Application Report
SPRAC02–September 2015

TPS544Bxx/TPS544Cxx Powering TCI6630K2L in Smart Reflex Class 0 TC Mode

ABSTRACT

This application report describes an application circuit example of the TPS544B/Cxx family of power management IC (PMIC) powering the Smart-Reflex digital core supply of the TCI6630K2L SoC. Smart-Reflex Class 0 Temperature Compensation (Class 0 TC) mode of operation of the TCI6630K2L device is emphasized. Assumption is that temperature compensation mode is enabled using the function provided in the Multi-Core Software Development Kit (MCSDK) software release - 3.1.0 or higher version.

In temperature compensated mode of operation, the TCI6630K2L SoC can achieve the best possible power consumption across all operating temperatures. This example power supply solution is also extendable to the 66AK2Lx family of SoC. as well.

Contents

1 Scope

This document is applicable to the following K2 devices: TCI6630K2L and 66AK2Lx.

1.1 Acronyms Used in This Document

Table 1. Acronyms

Acronym	Definition
TCI6630K2L	Keystone II architecture Device from Texas Instruments: http://www.ti.com/product/TCI6630K2L
66AK20Lx	Family of derivative ARM/DSP SoC based on the TCI6630K2L design http://www.ti.com/product/66ak2l06
PMIC	Power Management IC
SRSS	Smart Reflex Sub System on device
TC	Temperature Compensation
VID	SmartReflex VID Value Mapping KS2 Hardware Design Guide
R	Read Only Register
RW	Read Write Register
TPS544Cxx TPS544Bxx	PMBus compatible voltage regulator and digital controller PMIC from Texas Instruments.
MCSDK	Multi-Core Software Development Kit
CVDD	Smart-Reflex adjustable voltage supply that powers core digital logic on Keystone II devices

2 TCI6630K2L and TPS544BXX/TPS544CXX Connectivity for Smart-Reflex Class 0 Only Mode (non TC mode)

The core voltage supply generation for the TCI6630K2L device can be done with the TPS544Bxx or TPS544Cxx family of devices. These PMIC devices come in pin compatible packages. In a scenario where TCI6630K2L is intended to be used in Smart-Reflex Class 0 only mode (non TC mode), typical connectivity between these devices is depicted in the schematic for the TCI6630K2L EVM located at K2LEVM.

In the case of the Smart-Reflex Class 0 only mode (non TC mode), the TCI6630K2L device sends out a device-specific voltage value for its CVDD rail. After the device cpmpletes the power on reset sequence (after RESETSTATZ has gone high), the VID value is sent over the VCNTL pins. For details, see the *Hardware Design Guide for KeyStone II Devices* (SPRABV0). This is the device's voltage ID or VID value. The LM10011 device interprets this VID request sent over the VCNTL bus and generates the appropriate feedback current to inject into the TPS544BXX/TPS544CXX feedback loop. The lower the VID value the more current is injected such that the output voltage is negatively offset from its initial starting voltage value. Based on this feedback voltage,TPS544BXX/TPS544CXX generates stable voltage for the CVDD rail of TCI6630K2L. For details of implementation, see the *TCI6630K2L, TPS544BXX/TPS544CXX, LM10011 User's Guides* at http://www.ti.com/ww/en/analog/swift/products.html.

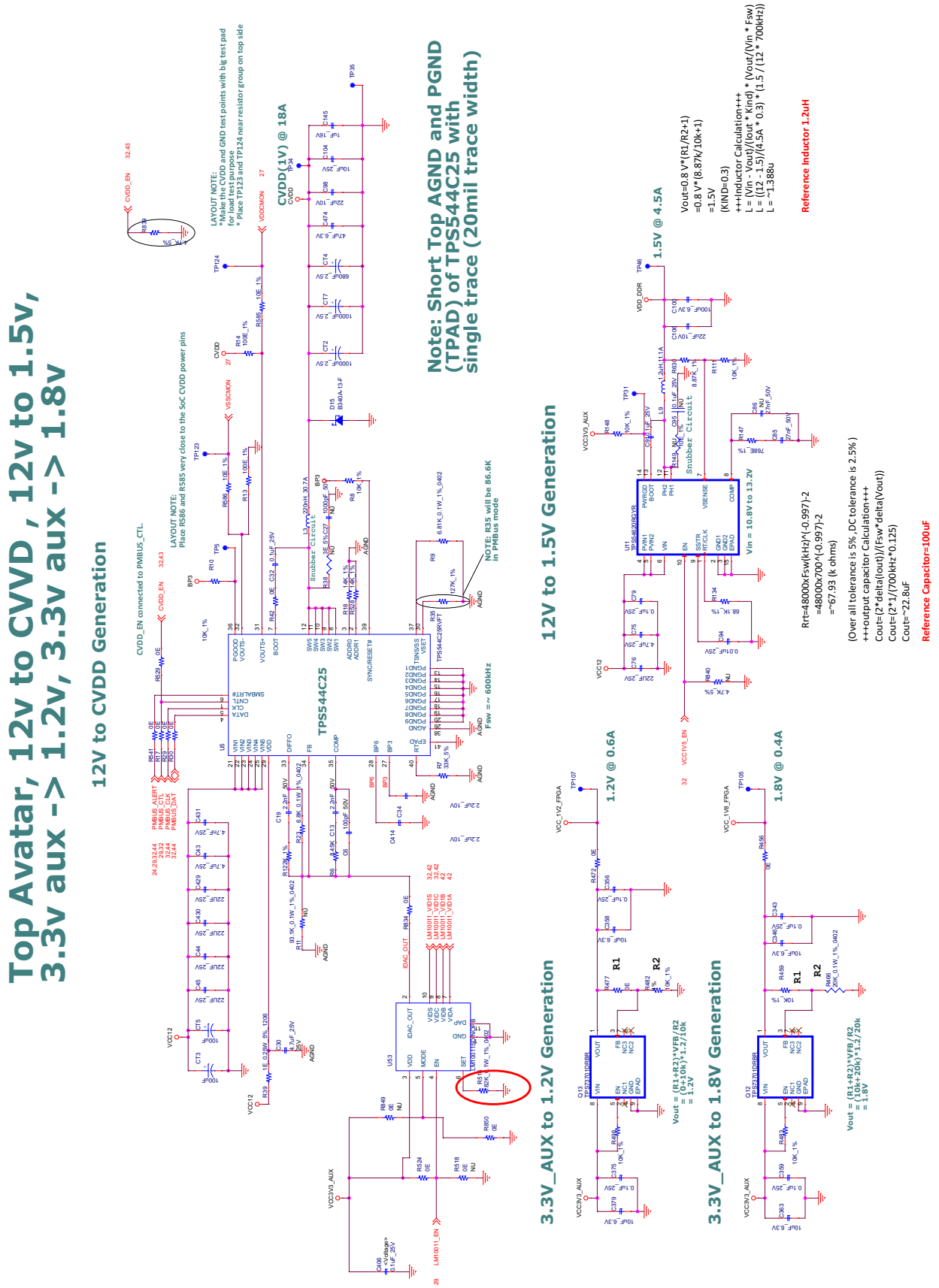

Figure 1. Schematic Excerpt Showing Implementation of TPS544C20 PMIC on the TCI6630K2L EVM

3 TCI6630K2L and TPS544BXX/TPS544CXX Connectivity for Smart-Reflex Class 0 TC Mode

To support Smart-Reflex Class 0 with Temperature Compensation, an I2C-based control solution of the TPS544B/C PMBUS is put in place of the LM10111/VCNTL solution described in Section 2.

3.1 Summary of Changes With Respect to Class 0 Non-TC Mode

In Smart Reflex Class 0 TC mode, the TCI6630K2L device sends out the temperature-specific VID of the CVDD rail. The TC mode software (running as a Linux service) is setup to use the I2C0 port of the K2L to communicate the VID value to the attached TPS544B/C device. Whenever the internal temperature of the TCI6630K2L exceeds pre-programmed temperature thresholds, the temperature monitoring software will trigger and send out an updated VID value over the I2C bus. An example schematic showing the necessary connectivity for the TC mode of operation is shown in Figure 2.

3.1.1 LM10011 Removed

When Smart Reflex Class 0 TC mode is enabled in TCI6630K2L, the CVDD voltage requests are conveyed straight to TPS544BXX/TPS544CXX over the I2C bus. Instead of using the feedback voltage from LM10011 to regulate the CVDD rails voltage, the TPS544BXX/TPS544CXX can regulate it based on the I2C requests. As such, the LM10011 is not utilized. It is worth noting that use of Smart Reflex Class 0 TC mode saves on component cost.

3.1.2 Default/Initial CVDD Voltage

Enabling of the Smart Reflex Class 0 TC mode in TCI6630K2L is done via software. Prior to enabling this mode on TCI6630K2L, the TPS544BXX/TPS544CXX sets a default voltage on the CVDD rail based on the VSET pin resistor value. In Figure 2, R_Vset (R25) is configured to provide 1 V on the CVDD rail of TCI6630K2L as a default CVDD value. TPS544BXX/TPS544CXX will maintain this CVDD rail value until a new output voltage is requested on the I2C bus.

3.1.3 Resistor Feedback Network

Use of the VSET pin to set the default voltage requires the VOUT_SCALE_LOOP term of TPS544BXX/TPS544CXX to be 1. This is achieved with a resistor network that provides feedback voltage to the FB pin of TPS544BXX/TPS544CXX. As shown in Figure 2, there is no Rbottom resistor between the FB pin and ground in this mode of operation.

For details on the resistor and VOUT_SCALE_LOOP, see the data sheets of the TPS544Cxx/ TPS544Bxx devices at SWIFT Point-of-Load DC/DC Converters.

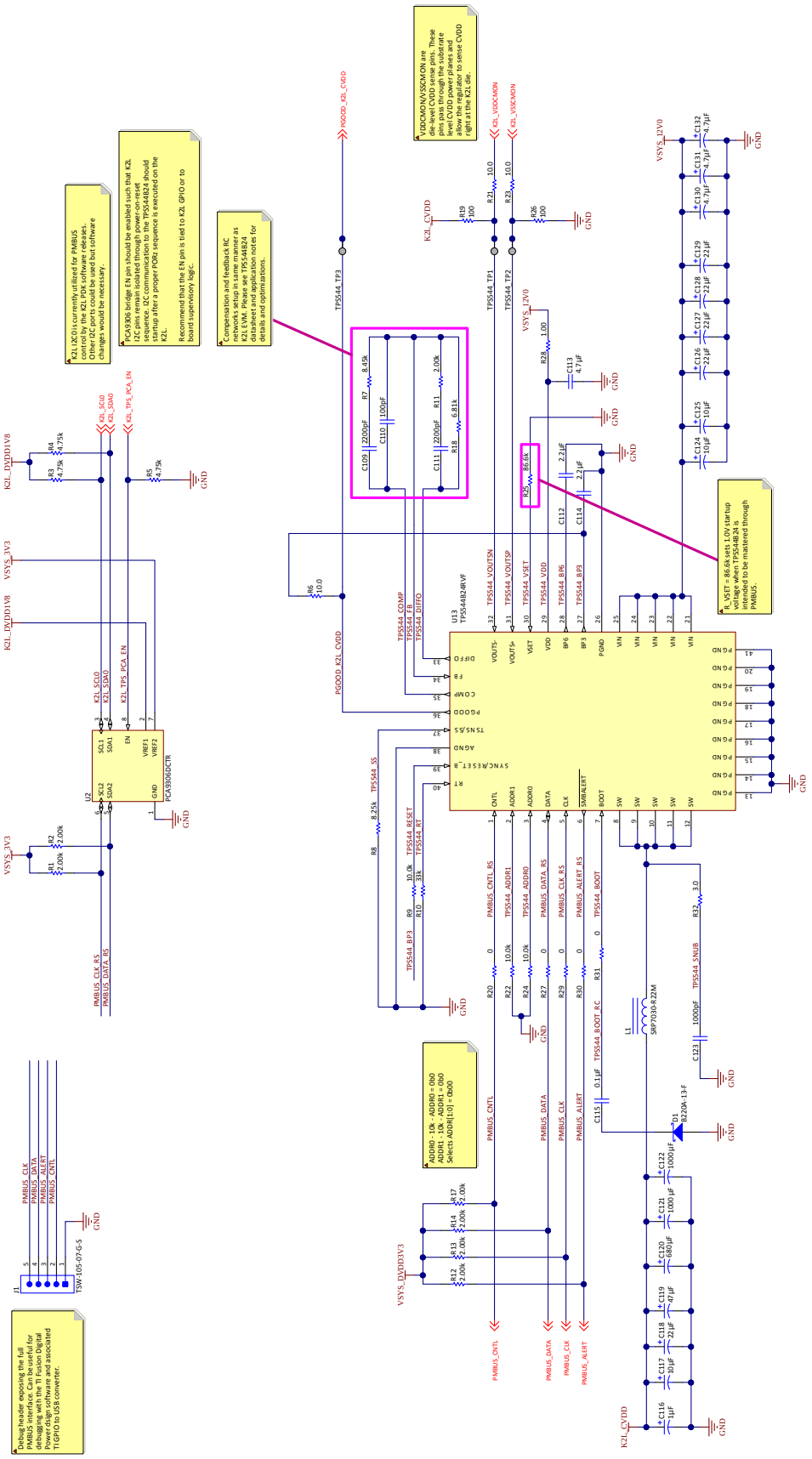

Figure 2. Schematic

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