

Common EOS pitfalls in board design

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ABSTRACT

As more and more features are integrated into the latest generation of processors, attention to detail is imperative in the design of the system hardware. The board design process is a critical phase where customers need to ensure that their design is compliant to the device-specific data sheet requirements. Errors in the data sheet compliance that are not caught in the board design phase can be very costly if the design is committed to hardware with errors.

This application report focuses on one such important system level integration detail that covers input/output (I/O) interfaces with fail-safe considerations and where non-compliance with the TI data sheet has shown to cause Electrical Over-Stress (EOS) issues in manufacturing and in the field. The following TI products are used as examples: AM335x, AM437x, AM57x family of Sitara™ processors.

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1 Introduction and Background

With ever increasing integration in the modern day system-on-chip (SoC), attention to details on system integration is very important. One such detail that is often overlooked is fail-safe considerations of I/O interfaces listed in device-specific data sheets. Robust system level design should ensure all I/O interfaces are fail-safe compliant during functional operation, supply power-up/down sequencing and low-power mode entry and exit.

Every SoC integrates I/O cells that interface with other system level components such as memory devices (NAND, NOR), serial ports, USB, DDR, Display, and so forth. These I/O cells in the SoC integrate ESD protection, output driver, input receiver functions to meet various interface requirements. A typical I/O cell is illustrated in [Figure 1](#).

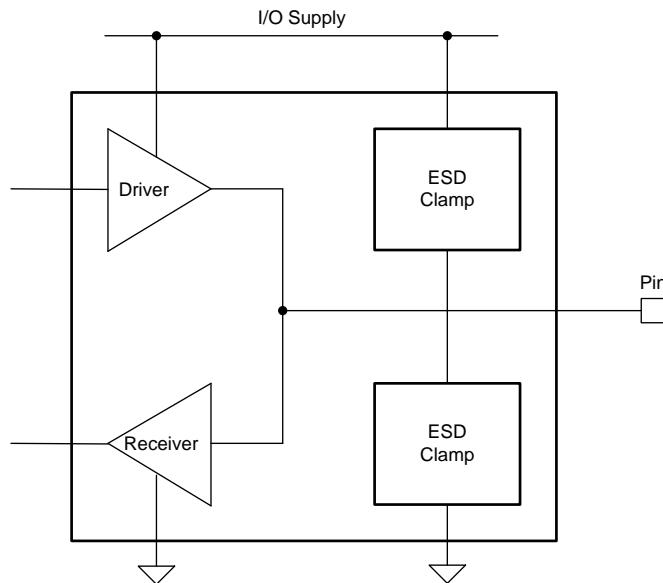


Figure 1. Typical I/O Block

The standard implementation of an ESD protection device in modern day SoC's consists of a dual-diode with a diode to supply and ground along with a supply ESD clamp to provide component level ESD protection such as Human Body Model (HBM) and Charge Device Model (CDM). This is illustrated in the [Figure 2](#).

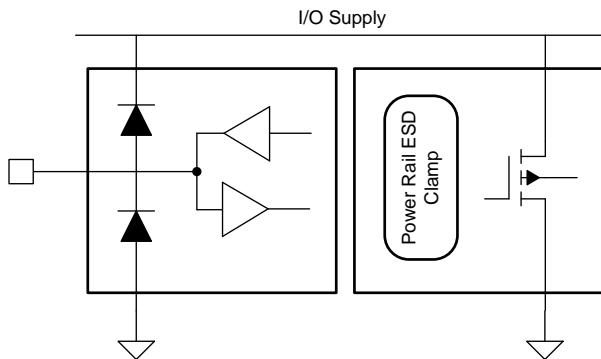


Figure 2. ESD Protection Scheme in I/O

As illustrated in [Figure 1](#) and [Figure 2](#), based on the supply connections of the I/O blocks for the SoC and the peripheral devices, the following definitions were established:

- **Fail safe I/O:** An interface between two or more devices, with each device having an independent power supply source that can survive the loss/failure of any power supply indefinitely without causing a reliability or functionality hazard in that device or in any of the still powered-up devices.
- **Non Fail safe I/O:** An interface between two or more devices, with each device having an independent power supply source that cannot survive the loss/failure of any power supply without causing a reliability or functionality hazard in that device or in any of the still powered-up devices.
- **<n>V Tolerant I/O:** The signal pins of any device whose power supply is within its specified operating range may be subjected to a maximum voltage of <n> V (<n> 1.8 V, 3.3 V, 5 V, and so forth) without causing a reliability or functionality hazard in that device or in any of the still powered-up devices.

Device-specific data sheets list I/O interfaces electrical specifications including the fail-safe tolerance. It is important to identify specific I/O pins and categorize them accordingly to the device capabilities for system level design and handling. Any violations to the fail-safe requirements can lead to permanent device damage. A device failure analysis identifying EOS damage due to fail-safe violations is listed in [Figure 3](#).

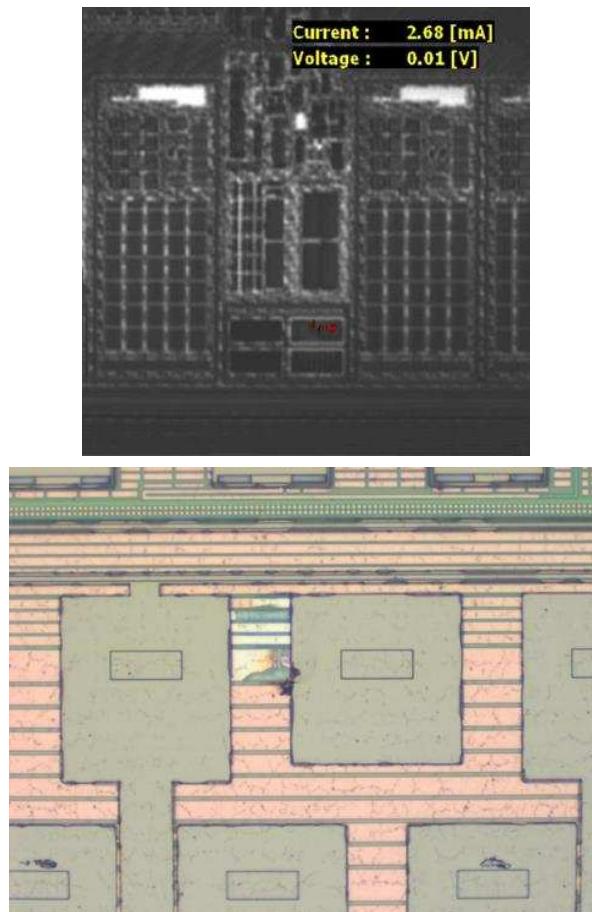


Figure 3. Device Damage Due to EOS

2 Common System Scenarios Leading to Fail-Safe Violations

This section covers a few system level design choices that can lead to Fail-safe violations of I/O interfaces and increased EOS risk levels.

A common and often ignored scenario causing fail-safe violations is power supply sequencing. [Figure 4](#) illustrates a common system design practice with split power rail system architecture for the SoC and the attached peripherals. In this system, a peripheral is powered by Source A, and SoC is powered by Source B. Even though source A and source B are of the same voltage levels, there is a possible fail-safe condition if source A and source B ramp up/down at different times as shown in [Figure 5](#). If any of the I/O pins connecting the peripheral to the SoC are driven/pulled high during the shaded region shown in [Figure 5](#), the I/O interface is subject to fail-safe condition. If the I/O interface is non fail-safe and subject to the fail-safe condition, there can be damage to the device over repeated exposure to the violation.

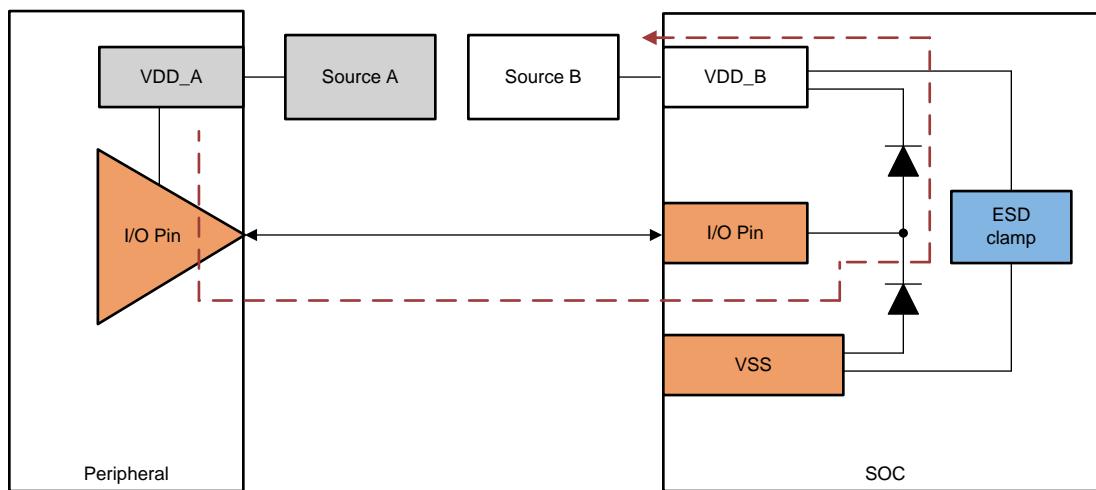


Figure 4. System With Split Rail Power Supply Design

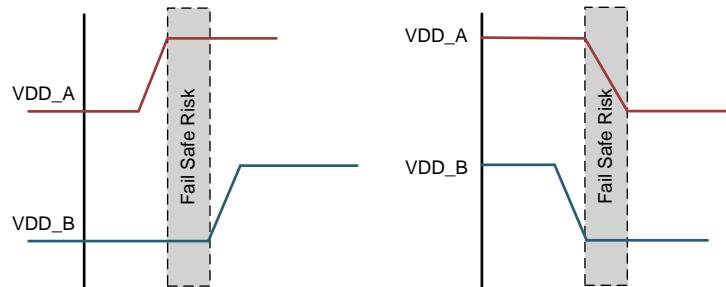


Figure 5. Staggered Power Supply Ramp-Up/Down

With a split power supply architecture, detailed and careful analysis of I/O interactions and default pin states during supply power-up and down sequencing is critical to avoid any fail-safe violations of both the SoC and the connected peripheral.

Low power consumption is an important consideration in most modern system design and especially a major concern for portable and battery powered systems. A common method employed to save system power is to turn off unused peripherals during system low power modes. [Figure 6](#) illustrates such a split power scheme where some of the peripheral power supplies are fully isolated from the SoC for shutting off during system low power modes. The system utilizes a Power Management IC (PMIC) that ensures the power up/down supply sequence does not create fail safe conditions and address fail safe risks with supply sequencing. However, the low power modes, where either the peripheral A or the SoC/Peripheral B power is shut off, presents a fail safe condition. Careful analysis of the interface pins and state of the interface pins during the low power modes should be assessed for any fail safe conditions. There can be permanent damage of the SoC and connected peripherals if the non fail safe I/O interface pins are subject to fail safe conditions for extended durations

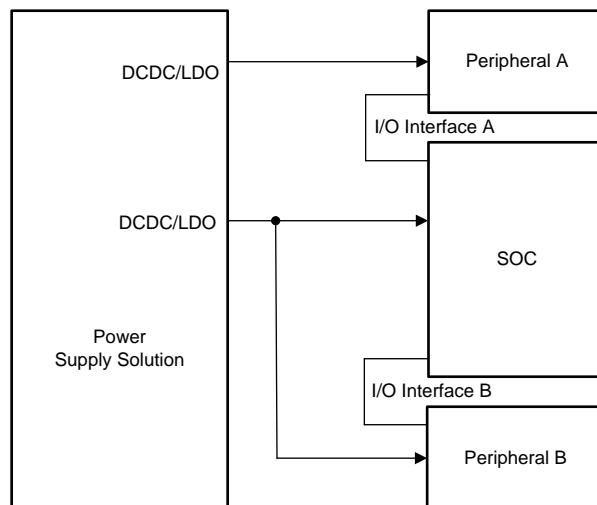


Figure 6. Low Power System Design With Split Power Rails

Design with fail safe considerations are also applicable for Analog pins and if the I/O pin is not designed to be fail safe, system design should avoid fail safe exposure to prevent device damage. The analog-to-digital converter (ADC) are used to monitor analog signals and a common use case is to monitor power supply rails. System level analysis should be performed to assess if the analog input pins of the ADC are subject to fail safe conditions when monitoring system and SoC power supply rails especially the rails that are turned ON before the ADC supply rail. Additional analysis should be performed to also review other system cases such as low power modes in addition to supply sequencing. An example of fail-safe condition exposure is illustrated in [Figure 7](#).

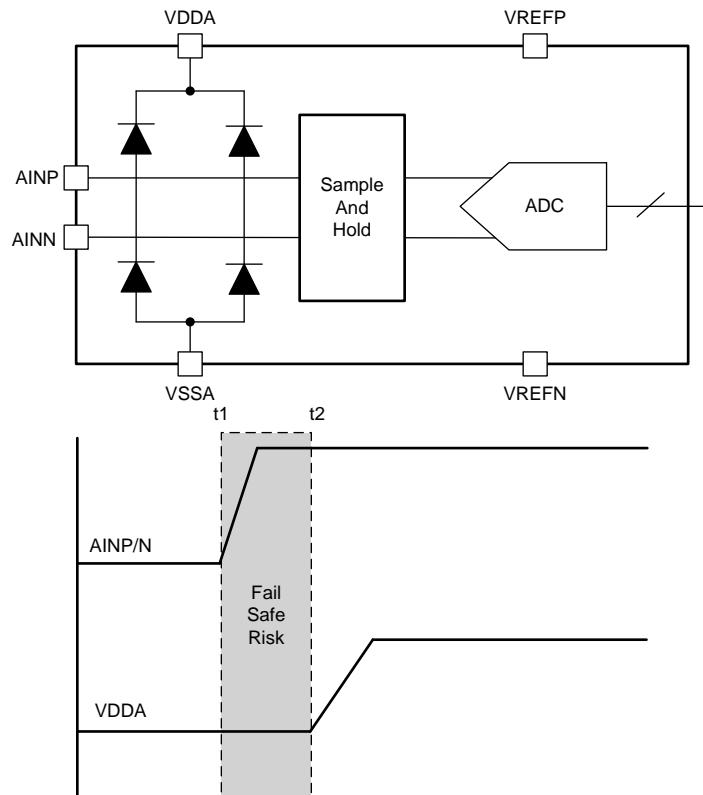


Figure 7. Analog Inputs of ADC

USB is another common Analog interface where fail safe considerations are important. When SoC operates as a USB device, it is possible that the SoC is connected to a USB host before the SoC power supplies are fully turned ON. This presents a fail safe exposure on the VBUS pin of the SoC where 5 V is applied on the VBUS pin of the SoC while the SoC power supply is not fully turned ON. If the VBUS pin of the SoC is not fail safe, extended exposure to this condition can cause permanent damage of the device. This is shown in [Figure 8](#).

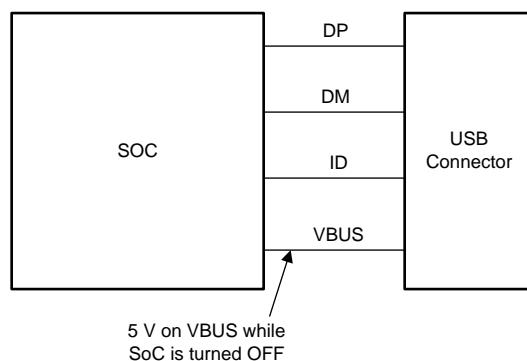


Figure 8. USB VBUS Fail Safe Considerations

Complex system designs often implement multi-board PCB approaches to ease the design process and also enhance reuse for a scalable platform based solution. Without proper fail safe considerations, the I/O interface between the different boards can be subject to fail safe considerations. All different system level aspects comprehending power supply ramp-up/down, low power modes should be assessed for fail safe exposure.

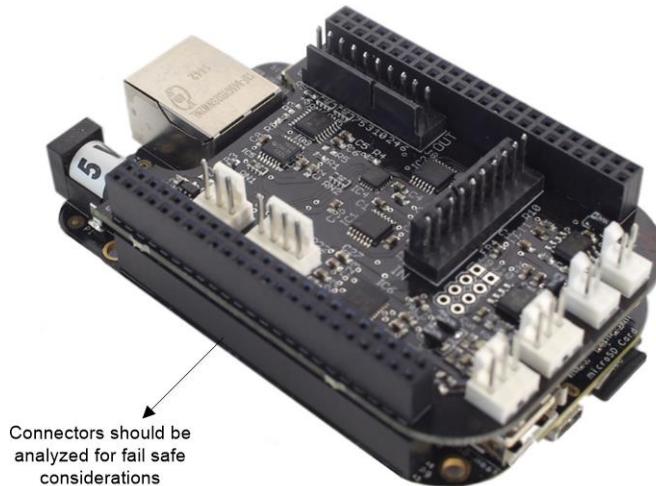


Figure 9. Multi PCB System Design

3 System Solutions for Fail-Safe Compliance

The first step for addressing fail safe compliance is to list different interfaces in the system along with their power supply associations. Analysis should be performed on the interfaces covering various system scenarios such as power supply ramp-up/down, low power entry/exit, hot plugging. If any I/O interface is subject to fail safe conditions, it should be reviewed for compliance with the device-specific data sheets and listed for special care and handling along with the condition causing the fail-safe condition.

If the I/O interface pins violate the device-specific data sheet fail safe requirements, several system level solutions exist to address the violations. A simple approach is to merge split power rails where possible, avoiding power supply sequencing race conditions causing fail safe violations. Other approaches to address fail safe violations may involve the usage of fail-safe buffers and level shifters when simpler fixes are not possible due to system considerations.

3.1 Definition of Terms

This section lists and describes some key terms used in this application report. The following definitions are specifically defined by TI and may or may not agree with other semiconductor vendor definitions.

3.2 EOS

EOS can be an over-current or over-voltage stress that occurs either randomly or systemically. This EOS has many possible sources as shown in Figure 10.

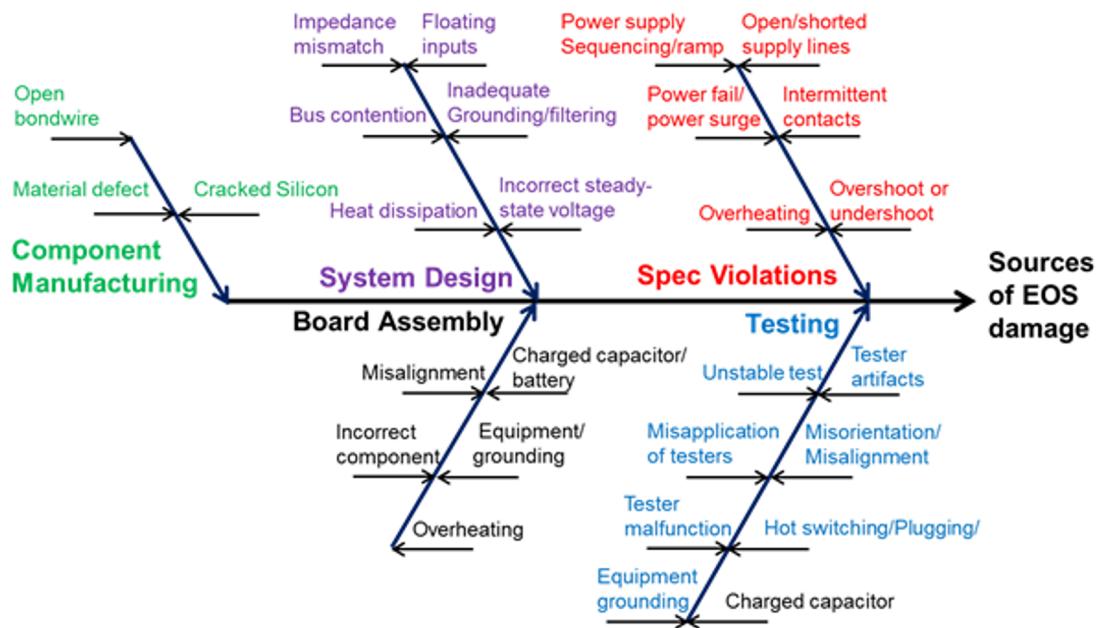


Figure 10. Ishikawa Diagram of Common Sources of EOS

3.3 Power Up/Down

A multi power rail device that demands a specific sequence of power rail ramp up and down in order to ensure reliable operation and functionality.

3.4 Low-Power Mode

A combination of clock and power controls in a device to dynamically turn off inactive portions of the device for reducing power consumption. Additionally, the device should still maintain proper state to enable quick resume to normal operation based on system activity.

3.5 Fail Safe

An interface between two or more devices, with each device having an independent power supply source, that can survive the loss/failure of any power supply indefinitely without causing a reliability or functionality hazard in that device or in any of the still powered-up devices.

4 References

- Texas Instruments: [AM335x Sitara™ processors data sheet](#)
- Texas Instruments: [AM335x and AMIC110 Sitara™ processors technical reference manual](#)
- Texas Instruments: [AM437x Sitara processors data manual](#)
- Texas Instruments: [AM437x and AMIC120 ARM® Cortex™-A9 processors technical reference manual](#)

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