Application Report
SPRACI9–October 2018

AM65x/DRA80x Schematic Checklist

ABSTRACT

This document shows examples and documents that specifically reference AM65x devices. Links for additional AM65x product pages and reference documents will be added as they become available.

Contents

Trademarks

1 Introduction

This article applies to the following devices:

- AM6548
- AM6546
- AM6528
- AM6527
- AM6526
- DRA804M
- DRA802M

Links to TI hardware designs based on AM65x:

- AM654x General Purpose EVM
- AM654x Industrial Development Kit EVM
- AM654x Silicon Errata

Check the relevant Sitara Processors Silicon Errata document when designing a board. This document contains important information on silicon issues which affect your board design.

Other useful links:

- High-Speed Interface Layout Guidelines
- AM654x/DRA80x PCB Escape Routing Guidelines
- TI PinMux Tool

2 Recommendations Specific to the AM65x/DRA80x

2.1 EVM versus Data Sheet

In case of any discrepancy between the TI EVMs and the device data sheet, always follow the data sheet. Despite the designer's best efforts, the EVMs may contain errors which may still function but are not completely aligned with the data sheet specification. Thus, the EVM designs should not be considered as reference designs to be blindly reused.

2.2 Power

- **Have you used the output of the power model and estimates from the rest of your design to determine the power solution needed?** The power needed for each rail of the AM65x/DRA80x SoC will vary based on the interfaces used and the environment in which it is operating. Power requirements must be determined using the power model.
- **Have you checked that the correct voltages are applied to the correct power pins on the device?** The AM65x/DRA80x SoC includes a number of power rails which must be powered with the correct voltage for proper operation.
- **Have you checked that all signals connected to each of these domains are operating at the expected voltage level?** The AM65x/DRA80x SoC includes twelve dual-voltage I/O domains configured for either 3.3 V or 1.8 V. All signals connected to these domains must match the voltage level provided to the associated VDDSHVx supply rail. The AM65x/DRA80x I/O buffers are not failsafe. The voltage for the VDDSHVx rail must be present before any voltage is applied to the associated I/Os.
- **Have you checked that the VDDS[2:0]_WKUP and VDDS[8:0] for all rails configured for 1.8 V are connected to the 1.8-V I/O power supply? Have you checked that the VDDS[2:0]_WKUP and VDDS[8:0] for all rails configured for 3.3 V are connected to the proper internal LDO?** To sequence correctly, VDDS[2:0]_WKUP and VDDS[8:0] must be supplied by either the 1.8-V I/O power supply or an internal I/O bias LDO, depending on the voltage of the rail.
- **Do you have the proper capacitor value connected to each output of the internal LDOs?** The AM65x/DRA80x SoC includes seventeen internal LDOs with the output of each connected to a pin on the device. The LDOs require an output capacitor connected to each of these pins.
- **Does your design meet the power sequencing requirement in the data manual?** Proper power supply sequencing in proper correlation with resets and clocks is required. Refer to the device-specific data sheet for the recommended power sequencing requirements.
- **Are the filters specified in the Technical Reference manual included for the VDDA_x supply pins?** AM65x/DRA80x devices contain multiple analog power pins that provide power to sensitive analog circuitry such as PLLs, DLLs, and SERDES buffers and terminations. These must be attached to filtered power sources.
- **Does your design include the correct termination for your selected DDR interface type?** The DDR3 and DDR4 interfaces both require a VTT termination at the end of the flyby chain for the DDR address, command and control. The VTT termination voltage is generated using a special push/pull termination regulator specifically designed to meet the VTT requirements.
- **Are the DDR_VREF0 and DDR_VREF_ZQ pins left unconnected with no external voltage applied?** The AM65x/DRA80x generates the DDR reference voltage internally. The DDR_VREF0 and DDR_VREF_ZQ pins are intended for observation only.
- **Has the PDN analysis been performed and are the proper values and number of bypass capacitors included in your design?** Use low ESL capacitors and mount them with short traces to keep the mounting inductance very low. This is required to meet the specified PDN impedance. See *Sitara Processor Power Distribution Networks: Implementation and Analysis* for more detail.
- **Does your design include properly implemented current measurement capabilities?** Zero ohm resistors in line with core and other power sections of the board are recommended for initial PCB prototype builds if the user wants to measure power. The user should then remove the resistor in production builds and connect the power planes with wide copper or multiple vias. Power measurement is the purpose of these resistors in the EVM designs. The implementation of these resistors adds inductance and resistance that can impair power supply and power distribution performance. Current measurement on a single part should never be substituted for the values provided by the Power Model spreadsheet.

2.3 Reset

- **If you are using the external MCU_PORz signal, do you have the MCU_BYP_POR pulled high?** The AM65x/DRA80x component supports the internal POK circuit, which eliminates the need for a reset signal generator. If MCU_BYP_POR is pulled high, an external reset pulse with the proper timing relative to the power sequencing must be generated and connected to the MCU_PORz and PORz pins.

- **If you are using the internal POK circuit, do you have the MCU_BYP_POR pulled low?** If the internal POK circuit is enabled, MCU_PORz and PORz are not needed and may be pulled high. If a reset signal is needed for an external device, the MCU_PORz_OUT or PORz_OUT can be used.
- **If you are using the internal POK circuit, do you have an external pull-up resistor on MCU_PORz?** MCU_PORz should be pulled high if the internal POK circuit is used.
- **Do you have a pull-down resistor on PORz_OUT and on MCU_PORz_OUT?** The MCU_PORz_OUT and PORz_OUT signals can be used to provide the reset to other devices on the board, but they must have individual pull-down resistors. The AM65x/DRA80x does not drive the PORz_OUT and MCU_PORz_OUT until the device has started to boot. A pull-down resistor keeps the PORz_OUT and MCU_PORz_OUT signals low during the initial power sequencing.
- **If you are using external MCU_PORz and PORz, do you have a reset circuit that generates the proper reset pulse?** If an external reset is used, it must meet the requirements for pulse length and must be held low during power sequencing.
- **Are all control pins held in the proper state until reset is released?** The pins used to configure the device must be held in the desired state until after the rising edge of the MCU_PORz. If the internal POK circuit is used, they must be held in the proper state until the rising edge of MCU_PORz_OUT. MCU_PORz_OUT and PORz_OUT must have a pull-down resistor to remain in the proper state until reset is released.

NOTE: The E3 version of the EVM does not have the pull-down resistors on MCU_PORz_OUT and PORz_OUT.

2.4 Boot Modes

- **Do all BOOTMODE and MCU_BOOTMODE pins have external pulling resistors or a circuit to drive the desired bootmode?** BOOTMODE and MCU_BOOTMODE pins do not have internal pull-up or pull-down resistors that are active during power up and reset. External pulling resistors can be used to set the bootmode. Alternatively, a buffer that is only driven when reset is active can be used to present the bootmode.
- **Is the expected bootmode present on the BOOTMODE and MCU_BOOTMODE pins when PORz or MCU_PORz are active?** If the bootmode pins are redefined for another purpose during operation, they must be released and set back to the proper levels to select the boot mode whenever the AM654x enters the cold reset state.

2.5 Unused Signals

Signals on unused interfaces can typically be left as no connect. Many of the I/Os have a Pad Configuration Register which gives control over the input capabilities of the I/O (INPUTENABLE field in each conf_<module>_<pin> register). See the Control Module chapter of the *AM65x Multicore ARM Keystone III SoC Technical Reference Manual* for more details. Software should disable the I/O receive buffers (that is, INPUTENABLE=0) which are not connected in the design as soon as possible during initialization. This INPUTENABLE field defaults to "input active" for most signals, which means there is a potential for some leakage during the power sequencing of the device if the input floats to a mid-supply level before the software can initialize the I/O. This should only be a concern when attempting to power up the design with minimum power consumption. Most designs should be able to tolerate this small amount of leakage in each floating I/O until the software has a chance to disable it. After disabling the receiver of the I/O, no leakage occurs.

NOTE: Refer to Section 4.5 Connections for Unused Pins in the Data Manual for specific guidance on certain unused pins.

NOTE: Refer to the Pad Configuration Registers section in the *AM65x Multicore ARM Keystone III SoC Technical Reference Manual* for specific guidance configuring I/Os.

2.6 Clocking

- **Do you have a clock source for WKUP_OSC0?** A clock source for WKUP_OSC0 is required for proper operation of the AM654x/DRA80x.
- **If OSC1 is not used, do you have it properly terminated?** The AM654x/DRA80x can operate with a single clock present on WKUP_OSC0. OSC1 can be used to provide a different clock for the MAIN domain or for use to generate audio clock frequencies.
- **Is the frequency for WKUP_OSC0 one of the acceptable frequencies?** The data manual includes a list of supported frequencies for WKUP_OSC0. The clock present must be one of the supported frequencies.
- **If used to clock the MAIN domain is OSC1 one of the acceptable frequencies?** The data manual includes a list of supported frequencies for OSC1. The clock present must be one of the supported frequencies unless it is only used for audio clock generation.
- **Does your design require a low frequency clock input?** The WKUP_LFOSC clock input is available to provide a 32.768-KHz clock for low power operation in deeper sleep modes. If your design does not support deeper sleep modes, this clock is not necessary.
- It is preferable to always have bias and dampening resistors that can help tune the crystal later in early version of the design. See Section 5.10.4 Clock Specifications in the device data sheet for more details.

2.7 System Issues

Pull-up Resistors

- **Are all pullups connected to the AM65x/DRA80x device pulled up to the correct I/O voltage?** Pulling a signal to the wrong I/O voltage can cause leakage between the I/O rails of the device. Each terminal has an associated supply voltage used to power its I/O cell. This can be found in the *AM654x Sitara™ Processors Data Manual*, in the Ball Characteristics table, and in the *DRA80xM Infotainment Applications Processor Silicon Revision 1.0*.

Peripheral clock outputs:

- Put 22-Ω series resistors (close to processor) on the output clocks of the following modules: MMC, GPMC, McASP (both clock and frame sync), SPI, QSPI, and VOUT.

General Debug:

- **Have you added visibility for the internal clocks?** Output clocks MCU_SYSCLKOUT0, MCU_OBSCLK0, and SYSCLKOUT0 are available on pins. If these pins/signals are not muxed in your design for other purposes, have test points on them to allow the monitoring of internal clocks in support of hardware and software debugging.
- **Have you added the ability to probe the MCU_PORz_OUT and PORz_OUT signals?** Accessible test points for MCU_PORz_OUT and PORz_OUT are useful for debug.

2.8 Low Power Considerations

If you are designing for low power, here are some tips to help you optimize your design for low power:

- On early prototype boards, TI recommends including small shunt resistors in the voltage rail paths of each of the following power rails of AM65x/DRA80x device: VDD_CORE, VDD_MCU, VDD_MPU0-1, VDDSHV0-2_WKUP, and VDDSHV1-11. These are listed in order of priority, so if you can't isolate all of these to measure power; the most important ones are the core rails VDD_CORE, VDD_MCU, VDD_MPU0-1, and so forth. Also, the VDDSHVx supplies may be broken into multiple segments and run at different voltages. This can help measure the power consumption of each rail and potentially pinpoint high power consumption during development. You may also want to add these shunt resistors for power supplies connected to other devices, to be able to measure power on those key devices. The AM654x/DRA80x EVMs have examples of these shunt resistors. For production, these shunt resistors must be removed from the design (that is, turned into a continuous plane) because these resistors restrict current flow and add inductance to the PDN.

2.9 DDR

- **Does your design have the proper connections for the type of DDR that you have selected?** The AM65x uses the same pins to support DDR3, DDR4, and LPDDR4, but these standards have different names for the signals connected to the memory device. Table 8-86 DDRSS0 AC Bus Mapping in the *AM65x Multicore ARM Keystone III SoC Technical Reference Manual* provides a mapping of the DDR pin names on the device to the appropriate signal name for each memory type.
- **Do you have notes in you schematic or guidelines to ensure that the DDR routing is done properly?** It is very important to follow the DDR routing guidelines in the AM65x device data sheet. These guidelines are very important to ensure a proper DDR operation. Failure to follow these guidelines will result in a nonfunctional DDR interface.
- **Does your design include the correct amount of decoupling for the DDR interface?** Always provide adequate decoupling capacitors on the DDR power rails both at the AM65x/DRA80x device and at the DDR SDRAM device. Proper distribution of these capacitors is mandatory when referencing fly-by signals to VDDS.
- **Have you connected the DDR RESET signal correctly for the type of device you have selected?** DDR RESET signal is treated differently from other control signals. Review the device data manual for proper operation. The addition of a pull-down resistor is also recommended.
- **Did you include the proper termination for the DDR memory device you have selected?** DDR3 and DDR4 have specific requirements for the termination of the flyby signals. Ensure that your signals are terminated correctly for the device selected. LPDDR4 does not use fly-by routing and it does not require VTT termination.
- **Did you include decoupling only for the DDR_VREF0 signal?** VREF can be obtained from the VTT termination regulator or from a resistor divider (2.2K-Ω 1% resistors) with capacitive decoupling to ground. It may be used for the VREF signals on the DDR memory devices, but should not be connected to the DDR_VREF0 signal on the AM65x/DRA80x. The VREF voltage for the AM65x/DRA80x device is generated internally. The DDR_VREF0 pin is used for external decoupling capacitors.
- **If your design supports ECC memory, does it have the correct component?** The AM65x/DRA80x supports 7 bits of ECC for x32-bit architectures and 6 bits of ECC for x16-bit architectures. Generally, the same device should be used for the ECC bits, even if some of the bits are unused.
- **Have you kept the signals associated with a byte lane in a group?** Data bit swapping within the data byte is allowed with the exception of the least significant bit, sometimes referred to as the prime bit. DDR D0, D8, D16, and D24 must be connected to the least significant bit for each byte on the memory device. The PHY is implemented such that this does not impact leveling. Bit swapping is not allowed for any other group of signals, including ADDR and CNTL.
- **Are you only using a single rank in your design?** The AM65x only supports single-rank operation. Signals for the second rank should not be used.
- **Have you terminated unused DDR signals correctly?** If a portion of the DDR interface is not used, then the applicable DDRx_DQSn and DDRx_DQSNn pins should be tied to the appropriate GND or power through a 1K-Ω resistor to keep the signals inactive as described in the *AM654x Sitara™ Processors Data Manual*. The same is also required if only a single byte lane is unused, such as the ECC byte lane. The address, command, control, clock, and data lines can all be left floating. The DDR supplies and VREF must be maintained at their rated levels per the *AM654x Sitara™ Processors Data Manual*.

2.10 MMC

- **Have you included a series resistor on the clock to dampen reflections?** Include a 22-Ω series resistor on MMCx_CLK (as close to the processor as possible). This signal is used as an input on read transactions, and the resistor eliminates possible signal reflections on the signal, which can cause false clock transitions.
- **Have you included pull-up resistors for SD-CARD signals to the proper I/O voltage rail?** Pull-up resistors are needed on all data and command signals. These pull-ups should be 10K Ω for SD-CARD implementations and 49.9K Ω for embedded device connections, such as eMMC memory devices. The pull-up resistors should be connected to the same supply used for the MMC I/O rail, VDDSHV6 for MMC0 or VDDSHV7 for MMC1.

- **Are you supporting UHS-I using the internal SDIO LDO?** The AM65x provides an internal SDIO LDO which has a switchable output to support either 3.3-V I/O or 1.8-V I/O. The switchable output must be connected to the proper I/O voltage rail and the bias voltage for the MMC interface used, VDDSHV6 and VDDS6 for MMC0 or VDDSHV7 and VDDS7 for MMC1. The proper capacitance value must also be included for proper operation of the LDO. In addition, a 270-Ω shunt resistor must be included between CAP_VDDSHV_SDIO and ground.
- **Have you connected the SD-CARD's VDD signal to a 3.3-V I/O supply?** While the I/O voltage for the SD-CARD interface can be either 1.8 V or 3.3 V, the SD card's VDD signal should be connected to a fixed 3.3-V rail. In other words, the card's VDD must remain at 3.3 V even for the UHS-I modes of operation. Only the signaling levels change in these modes, not VDD.

2.11 OSPI and QSPI

- **Is the MCU_OSPI[x]_LBCLKO signal connected correctly for the device you have selected?** The MCU_OSPI[x]_LBCLKO signal is used differently depending on what type of device you are using and if internal pad loopback is used.
- **Are the OSPI/QSPI data bits connected in the proper order?** D0 and D1 of the OSPI peripheral must be connected to D0 and D1 of the QSPI/OSPI memory to support legacy x1 commands. TI does not support bit swapping on the balance of the data bits, so these must also be connected in the correct order.

2.12 GPMC NAND

- **Does your design use the NAND R/B# signal?** Typically the R/B# signal from the NAND is open drain and connected to the GPMC0_WAIT0 signal. Include a 4.7K pullup to the appropriate voltage, depending if the NAND is 1.8 V or 3.3 V.

2.13 I2C

- **Do you have the I2C pull-ups connected to the correct voltage?** I2C interfaces require a pull-up resistor on both the data and the clock lines. 4.7K-Ω pull-up resistors must be attached on both I2C signals (x_SDA and x_SCL). Ensure the pull-up resistors connect to the correct I/O voltage rail. See the note on the Pull-up Resistors section above.
- **Are you using TI's software (Linux SDK) for PMIC control?** The TI software expects the WKUP_I2C0 to be connected to the PMIC.
- **Do you need a fully compliant I2C buffer?** The WKUP_I2C0 and MCU_I2C0 use true open-drain buffers that are fully compliant to the I2C specifications. These support 100-kHz and 400-kHz operation. The remaining I2C interfaces, I2C0-I2C2, use LVCMOS to emulate an open-drain buffer. These can support 3.4-Mbps I2C operations; however, these ports are not fully compliant with the I2C specification, in particular falling edges are too fast (< 2 ns). Any devices connected to these ports must be able to function properly with the faster fall time.

2.14 CPSW Ethernet

- **Have you correctly configured the initial configuration for your PHY?** Most PHYs use the signals normally driven by the PHY to capture the initial configuration, using pull-up and pull-down resistors. The TI PHY used on the AM65x/DRA80x EVM uses both to generate a mid-level voltage, allowing four separate configurations per pin. By default in the AM65x/DRA80x, both the receiver buffers and the internal pulling resistors are disabled at reset. The PHYs should be removed from reset, allowing the initial configuration to be captured before enabling either the receiver buffers or the internal pulling resistors.
- **Have you terminated your RGMII signals correctly?** For the RGMII interfaces, 22-Ω series termination resistors must be placed on all 12 interface signals as close to the transmitter as possible.
- **Have you used 1.8-V I/O voltage level for your RGMII interface?** Use 1.8 V for the RGMII I/O voltage level. The AM65x/DRA80x is not rated for RGMII operation at 3.3 V.

2.15 ICSSG

- **Have you selected the correct pins for your industrial application?** ICSSG pins allow muxing at the ICSSG IP level and at the SoC level using the PADCONFx registers. Carefully check that you have connected your schematic correctly for your application. In particular, review the differences between the RGMII connections and the MII connections for the TX pins.
- **Are you using an MII interface to an Ethernet PHY?** Some industrial protocols require the use of a 10/100-Mbit Ethernet. MII may be required to operate these protocols correctly. Check with your PHY manufacturer to determine if MII is needed.
- **Have you terminated your RGMII signals correctly?** For the RGMII interfaces, 22-Ω series termination resistors must be placed on all 12 interface signals as close to the transmitter as possible.
- **Have you used 1.8-V I/O voltage level for your RGMII interface?** Use 1.8 V for the RGMII I/O voltage level. The AM65x is not rated for RGMII operation at 3.3 V.

2.16 USB

- **Have you planned for the routing in the USB interface?** Refer to the *High-Speed Interface Layout Guidelines Application Report* for detailed recommendations on proper USB signal connection and routing. Add appropriate constraints or routing requirements to your schematic. This will vary from tool to tool.
- **Have you included the correct VBUS decoupling for your configuration?** USB device operation requires decoupling capacitance of less than 10 µF connected to the USB VBUS. USB host operation requires decoupling capacitance of greater than 120 µF connected to the USB VBUS. VBUS decoupling capacitance should be connected close to USB connector.
- **Have you connected the USBx_DP and USBx_DM signals directly to the connector?** USBx_DP and USBx_DM should never have any series resistors or capacitance on these signals. These signals should be routed with traces that do not include stubs or test points. These traces should be connected directly between the AM65x and the connector, unless EMI control is needed.
- **If you are including a USB device, have you connected the USB signals correctly?** USBx_DP and USBx_DM should be routed with traces that do not include stubs or test points. These traces should be connected directly between the AM65x and the connector unless EMI control is needed. The connector ID pin can be left unconnected. The USBx_DRVVBUS is not used and can be left unconnected.
- **If you are including a USB host, have you connected the USB signals correctly?** USBx_DP and USBx_DM should be routed with traces that do not include stubs or test points. These traces should be connected directly between the AM65x and the connector unless EMI control is needed. Connector ID should be grounded. The USBx_DRVVBUS should be connected to the enable of the 5-V VBUS power source. The VBUS pin on the USB connector should be connected to the output of the 5-V VBUS power from the power switch controlled by USBx_DRVVBUS
- **If you are including a USB hub, have you connected the USB signals correctly?** USBx_DP and USBx_DM should be connected directly to the USB hub upstream port. The hub then distributes these signals to the downstream ports as needed. The connector ID should be grounded to enable host mode. The USBx_DRVVBUS should be unconnected. The USBx_VBUS should be connected to the output of the 5-V VBUS power source. It is also connected to the VBUS detect on the hub, which then allows the hub to selectively enable or disable, typically through a power switch to each downstream port.
- **Do you need components for EMI and ESD protection?** Common-mode chokes may be needed for EMI/EMC control. These may reduce the signal amplitude and degrade performance. In addition, ESD suppression may also be required. If necessary, these components should be included in the design.

2.17 SERDES - USB3

- **Have you planned for the routing in the USB3 interface?** Refer to the *High-Speed Interface Layout Guidelines Application Report* for detailed recommendations for proper USB3 SERDES signal connection and routing. Add appropriate constraints or routing requirements to your schematic. This will vary from tool to tool.
- **Have you connected the correct SERDES pairs for USB3 operation?** The AM65x includes two SERDES transmit and receive pairs named SERDES0 and SERDES1. Each can support a number of

SERDES interfaces, but the correct SERDES interface must be used for some functions. USB3 is only supported using the SERDES0 transmit and receive signals.

- **Have you included DC-blocking capacitors in the correct location?** DC-blocking capacitors are required for USB3 transmit and receive pairs, but the capacitors should be placed closer to the USB3 transmitter. If a USB3 connector is used in the design, the receive pair will be connected directly to the connector. The DC-blocking caps for the receive pair are present on the device connected to the USB3 connector.
- **Have you connected the correct USB2 signals for the USB2 compatibility?** USB3 connectors include both the USB3 and USB2 connections for compatibility with older USB devices. The AM65x supports two USB2 interfaces, but the USB0_DM/P signals should be connected to a USB3 connector. USB1_DM/P is a USB2-only interface.

2.18 SERDES - PCIe

- **Have you planned for the routing in the PCIE interface?** Refer to the *High-Speed Interface Layout Guidelines Application Report* for detailed recommendations on proper PCIE SERDES signal connection and routing. Add appropriate constraints or routing requirements to your schematic. This will vary from tool to tool.
- **Have you connected the correct SERDES pairs for PCIE operation?** The AM65x includes two SERDES sets of transmit and receive pairs named SERDES0 and SERDES1. Each can support a number of SERDES interfaces, but the correct SERDES pairs must be used for the correct interface. SERDES0 and SERDES1 can each support two separate PCIE 1-lane connections, but if a PCIE 2-lane connection is needed, the pairs must be connected in the correct order. SERDES0 signals should be connected to the PERp0/n0 and PETp1/n1 pairs, and the SERDES1 signals should be connected to the PERp1/n1 and PETp1/n1 signals for a two-lane PCIE connection.
- **Have you included DC-blocking capacitors in the correct location?** DC-blocking capacitors are required for PCIE transmit and receive pairs, but the capacitors should be placed closer to the PCIE transmitter. If a PCIE connector is used in the design, the receive pair will be connected directly to the connector. The DC-blocking caps for the receive pair are present on the device connected to the PCIE connector.

2.19 JTAG and EMU

- **Have you included a JTAG connection?** If the JTAG and EMU interface is not used, all pins except TRSTn, TCK, and TMS can be left floating. TRSTn must be pulled low to ground through a 4.7k-Ω resistor. TCK and TMS must be pulled to VDDSHV3 through a 4.7k-Ω resistor. However, TI strongly recommends that all board designs contain at least a minimal JTAG port connection to test points or a header footprint to support early prototype debugging. The minimum connections are TCK, RTCK, TMS, TDI, TDO, and TRSTn. JTAG routes and component footprints (except the PD on TRSTn and the PU on TMS and TCK) can be deleted in the production version of the board, if desired.
- **Have you connected the RTCK signal correctly on your JTAG connector?** Emulators that support adaptive clocking must be implemented correctly using the RTCK output. If the pin-out of your emulation connector includes the RTCK signal, such as the CTI20 or the MIPI60, the TCK signal should be connected to a buffer for the AM65x and buffer for the RTCK pin. An example can be found in appendix B of the *Emulation and Trace Headers Technical Reference Manual*.
- **Are all of your JTAG signals using the same I/O voltage?** In the AM65x, the buffers for TDI, TDO, and TMS are powered by the VDDSHV0 domain. The buffers for TCK, TRSTz, EMU0, and EMU1 are powered by the VDDSHV0_WKUP domain. For proper operation of most emulators, these signals must be operating at the same voltage level. If this is a requirement for your emulator, ensure that VDDSHV0 and VDDSHV0_WKUP are both at either 1.8 V or 3.3 V.
- **Have you provided the proper buffering for robust JTAG operation?** Clock and signal buffering are required whenever the JTAG interface connects to more than one device. Clock buffering is strongly recommended even for single-device implementations. Verify series terminations are provided on each clock buffer output and ideally, that the clock output tracks are skew matched. EMU pins must not be buffered. EMU[1:0] can be bussed to multiple devices.
- **Are you connecting the TRC_x signals for trace operation?** If trace operation is needed, the TRC_x signals must be connected to the emulation connector. All TRC_x signals are pinmuxed with other signals. If the trace connections are needed, the connections for GPMC address and PRU2

interface may not be used. Routes for TRC_x signals used for trace must be short and skew matched. Trace signals are on a separate power domain and can be at a different voltage from the other JTAG signals. For more recommendations on TRC/EMU routing, refer to the *Emulation and Trace Headers Technical Reference Manual*l. A similar summary of this information is available at XDS Target Connection Guide.

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