Application Report
SPRACL9–May 2019

KeyStone™ Multicore Device Family Schematic Checklist

Catalog Processors

ABSTRACT

This application report highlights design topics that should be addressed by all board designers. It shows examples and documents that specifically reference KeyStone-I and KeyStone-II devices.

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1 Introduction

This article applies to the devices listed below. Product documentation is available on the product pages available at each link.

KeyStone-I DSPs

- TMS320C6652
- TMS320C6654
- TMS320C6655
- TMS320C6657
- TMS320C6670
- TMS320C6671
- TMS320C6672
- TMS320C6674
- TMS320C6678

KeyStone-II Devices

- 66AK2H14
- 66AK2H12
- 66AK2H06
- AM5K2E04
- AM5K2E02
- 66AK2E05
- 66AK2E02

2 Hardware Design Guide

For more details about design ideas and recommendations, the hardware design guide is referenced.

- For the KeyStone I hardware design guide, see the *Hardware design guide for KeyStone I devices*.
- For the KeyStone II hardware design guide, see the *Hardware design guide for KeyStone II devices*.

3 Device Comparison

Table 1 and Table 2 do not provide an all-encompassing feature list. It is intended to show differences between the devices in order to know which sections of this document apply to your specific device. Features common to all devices such as EMIF16, 1GbE Switch, general-purpose input/output (GPIO), inter-integrated circuit (I2C), serial peripheral interface (SPI), universal asynchronous receiver/transmitter (UART), and so forth are not shown. The chart is color coded to emphasize the groups of devices that are pin-for-pin compatible.

3.1 KeyStone II Devices

Table 1. KeyStone II Devices

Device	Arm Cortex-A15	C66x	PLL	DDR3	Hyperlink	PCIe	SRIO	TSIP	10-GbE	Coprocessor	USB 3.0	McBSP	UPP	AIF2	Package
66AK2H14	4	8	5	2x72 bit	2	1 x2	x4	NO	YES	1x NETCP (PA, SA)	1	NO	NO	NO	1517-ball FCBGA (AAW)
66AK2H12	4	8	5	2x72 bit	2	1 x2	x4	NO	NO	1x NETCP (PA, SA)	1	NO	NO	NO	
66AK2H06	2	4	5	2x72 bit	2	1 x2	x4	NO	NO	1x NETCP (PA, SA)	1	NO	NO	NO	
AM5K2E04	4	NO	3	1x72 bit	1	2 x2	NO	YES	NO	1x NETCP (PA2, SA2)	2	NO	NO	NO	1089-ball FCBGA (ABD)
AM5K2E02	2	NO	3	1x72 bit	1	2 x2	NO	SYE	NO	1x NETCP (PA2, SA2)	2	NO	NO	NO	
66AK2E05	4	1	3	1x72 bit	1	2 x2	NO	YES	NO	1x NETCP (PA2, SA2)	2	NO	NO	NO	
66AK2E02	1	1	3	1x72 bit	1	2 x2	NO	YES	NO	1x NETCP (PA2, SA2)	2	NO	NO	NO	

3.2 KeyStone I Devices

Table 2. KeyStone I Devices

Device	Arm Cortex-A15	C66x	PLL	DDR3	Hyperlink	PCIe	SRIO	TSIP	10-GbE	Coprocessor	USB 3.0	McBSP	UPP	AIF2	Package
TMS320C6654	NO	1	2	1x36 bit	NO	x2	NO	NO	NO	NO	NO	x2	YES	NO	625-ball FCBGA (CZH)
TMS320C6652	NO	1	2	1x36 bit	NO	NO	NO	NO	NO	NO	NO	x2	YES	NO	
TMS320C6655	NO	1	2	1x36 bit	1	x2	x4	NO	NO	TCP3d, 2x VCP2	NO	x2	YES	NO	
TMS320C6657	NO	2	2	1x36 bit	1	x2	x4	NO	NO	TCP3d, 2x VCP2	NO	x2	YES	NO	
TMS320C6671	NO	1	3	1x72 bit	1	x2	x4	x2	NO	NETCP	NO	NO	NO	NO	841-ball FCBGA (CYP)
TMS320C6672	NO	2	3	1x72 bit	1	x2	x4	x2	NO	NETCP	NO	NO	NO	NO	
TMS320C6674	NO	4	3	1x72 bit	1	x2	x4	x2	NO	NETCP	NO	NO	NO	NO	
TMS320C6678	NO	8	3	1x72 bit	1	x2	x4	x2	NO	NETCP	NO	NO	NO	NO	

4 Power Management Solutions

- For TT power management solutions, see the TI power management webpage. In addition, WEBBENCH designer tools provide a visual interfaces that deliver a complete power application in seconds.
- KS1: TIDEP0011/PMP8275
- KS2: TIDEP0042

5 Recommendations Specific to all KeyStone Devices

5.1 EVM vs Data Sheet

In case of any discrepancy between the TI EVMs and the device data sheet, always follow the data sheet. Despite the designer's best efforts, the EVMs may contain errors that still function but are not completely aligned with the data sheet specification. Therefore, the EVM designs should not be considered as reference designs to be blindly reused.

5.2 Critical Connections

5.2.1 Power

- Check that the correct voltages are applied to the correct power pins on the chip and that the required current can be supplied.
- Zero Ω resistors in line with core and other power sections of the board are recommended for initial PCB proto builds if you want to measure power. You can then remove the 0 Ω resistor in production builds.
- Proper power supplies sequencing is required in cooperation with resets and clocks. For the recommended power sequencing requirements, see the device-specific data sheet.
- TI SmartReflex™ solution is strictly recommended for CVDD rail of KeyStone devices. SmartReflex reduces device power consumption and ensures the proper operation across the temperature range. For better understanding of SmartReflex, see *SmartReflex™ power and performance management technologies*.
- The power supply solutions need to have remote sensing to compensate for resistive drop of the power path. For more information, see *Remote sensing for power supplies*.
- CVDD1 supply cannot be connected to the adaptive voltage scaling (AVS) supply used for CVDD and must be generated by the separate power circuit.
- The DDR3 interface requires a VTT termination at the end of the fly-by chain for the DDR3 address and control signals. The VTT termination voltage is generated using a special push/pull termination regulator specifically designed to meet the VTT requirements for DDR3.
- The VTT regulator provides voltage rail for DDR reference voltage also. If not, the voltage divider can be used. If a resistor divider is used, the VREFSSTL source voltage must be generated from the DVDD15.
- KeyStone devices contain multiple analog power pins that provide power to sensitive analog circuitry like PLLs, DLLs and serializer/deserializer (SerDes) buffers and terminations. These must be attached to filtered power sources. These filter solutions must match the recommendations in the device-specific Hardware Design Guide. For the link, see Section 2.
- For decoupling solutions, make sure that you are referring to the the device-specific Hardware Design Guide. For the link, see Section 2.

5.2.2 Clocking

- Many clock inputs are low jitter clock buffers (LJCBs). These input buffers accept LVDS and LVPECL signaling levels but must be AC coupled. The LJCBs do not support DC coupling to these interface standards.
- The LJCB input buffers include a 100 Ω parallel termination (P to N) and common mode biasing. Because the common mode biasing is included, the clock source must be AC coupled using a 0.1 µF ceramic capacitor (0402 size or smaller recommended).
- There are other clock inputs that are not LJCBs that must be conditioned differently for that specific device as discussed in the device-specific Hardware Design Guide. For the link, see Section 2.
- All clock inputs have jitter limitations. SerDes clock inputs have very stringent jitter limitations. For various interfaces on the jitter requirements, see the device-specific Hardware Design Guide. For the link, see Section 2.
- For the clocking design guide, see *Clocking Design Guide for KeyStone Devices*.

5.2.3 LJCB Differential Clock Inputs

- Many reference clock inputs are connected to a low-jitter clock buffers (LJCB) in the KeyStone devices. This buffer is designed to interface with LVDS, LVPECL, and HCSL clock input levels using AC coupling capacitors.
- The LJCB has internal termination and an internal common mode voltage generator so no external termination is needed between the AC coupling capacitors and the KeyStone device.
- The driver selected for your design may require termination on the output. You should review the device-specific data manual for the driver to determine what termination is necessary.

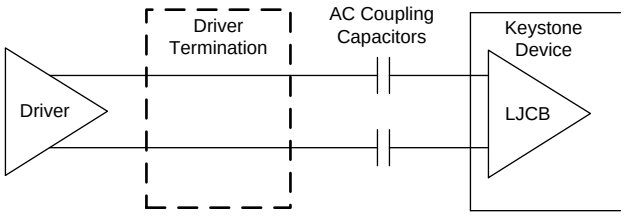

Figure 1. LJCB Differential Clock Inputs

5.2.4 Clock Termination

Most input clocks are presumed to be of the differential type and require proper terminations or coupling. Each differential pair must be AC-Coupled using a 0.1 µF ceramic capacitor (0402 size or smaller recommended). In some cases, depending on topology, a 1-µF capacitor can be used. All AC-coupling capacitors should be located at the destination end as close to the device as possible. For more information, see *AC-coupling between differential LVPECL, LVDS, HSTL, and CML*.

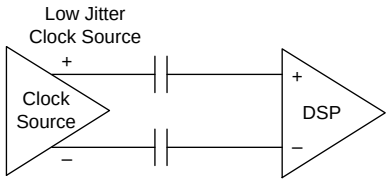

Figure 2. Clock Termination

5.2.5 Unused Clock Inputs

Any unused LJCB or LVDS differential clock inputs should be connected to the appropriate rails to establish a valid logic level. Unused clock inputs connected to the SerDes/CML in the KeyStone II device should be left unconnected. The recommended connections are shown in Figure 3 and Figure 4. The added 1kΩ resistor is designed to reduce power consumption. The positive terminal should be connected to the respective power rail. For more clarity, see *Hardware Design Guide for KeyStone™ I Devices* and the *Hardware Design Guide for KeyStone II Devices*.

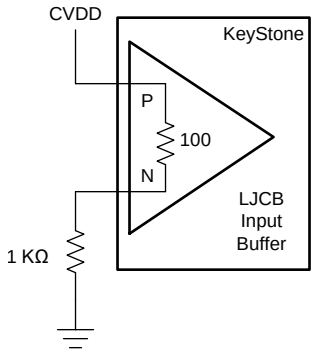

Figure 3. Unused LJCB Clock Input Connection

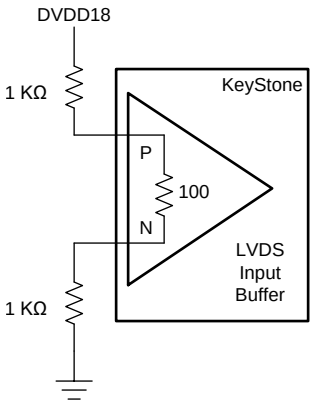

Figure 4. Unused LVDS Clock Input Connection

5.2.6 Reset

- Reset pins must be driven as defined in the device's Data Manual. This sequencing in relation to clocks and power supply ramping must be followed in all operating conditions, including boundary scan testing.
- The PORz pin has special properties such that it holds all output pins at high impedance when low. When controlled from logic derived from a Power Good indication, it can safely shut down the device if a power supply fault occurs.
- All control pins must show a means to be held in the proper operating state prior to the reset signal raising that releases the device from reset.
- RESETFULL and POR must be controlled separately.
- If the LRESET is not used, it is recommended that it be pulled high to DVDD18 with an external 4.7kΩ resistor to ensure that the CorePacs are not unintentionally reset.

5.2.7 GPIO/Boot Configuration

- The design must support the dual role of these pins. The pins need to return to the boot configuration levels whenever the boot configuration is latched. This is indicated by RESETSTATz low on most devices.
- Boot configuration can rely on the internal pull-up or pull-down resistors for most devices. However, if any track, even a test pad, is added to a pin, an external resistor must be added to maintain the rated noise immunity.
- Sometimes boot configuration inputs are multiplexed with other interfaces like timers, which are often overlooked. These pins must also revert to their boot-configuration level whenever it will be latched.
- Internal resistors can be as low as 8K Ω. This must be considered when connecting an external resistor to oppose it. Additionally, when multiple pins are bussed together, the combined leakage current of the internal resistors must be considered.

5.2.8 JTAG and EMU

- Clock and signal buffering are required whenever the JTAG interface connects to more than one device. Clock buffering is recommended even for single device implementations. It was verified that series terminations are provided on each clock buffer output and ideally that the clock output tracks are skew matched.
- EMU pins must not be buffered. EMU[1:0] can be bused to multiple devices. Other EMU pins connected for trace usage must be short and skew matched.
- For more recommendations on JTAG and EMU, see the *Emulation and trace headers technical reference manual*.
- For XDS target connection, see the *XDS Target Connection Guide*.
- Adaptive clocking must be implemented correctly for devices that have an RTCK output.
- If the JTAG and emulation interface is not used, all pins except TRST can be left floating. TRST must be pulled low to ground through a 4.7 kΩ resistor.
- In the event that the JTAG interface is used and the emulation (or a subset of the emulation pins) interface is not used, the unused emulation pins can be left floating.

6 Peripherals

6.1 DDR3 Interface

- Address, command, clock signals must be routed in fly by topology with VTT termination. Balanced T routing is not supported on DDR3 design for these devices.
- It is recommended to use dedicated ZQ resistor of 240 Ω 1% to be connected to each SDRAM ZQ pin (cannot share pins).
- Each respective address and command net should be end terminated using a resistor (in the range of 39 Ω to 49 Ω) and connected to VTT. The preferred resistor value is 39 Ω, 1%.
- The clock nets shall be terminated with a series 39 Ω, 1% resistor to a 0.1 µF capacitor to DVDD15 (VDDq).
- Each trace to the respective termination should be ≤ within 500 mils and the opposite side of the termination resistor should tie directly to the VTT rail.
- The reference voltage must be derived from the VDDQ supply using a resistor divider using 1% resistors (this reference voltage can also be derived from VTT power supply, such as TPS51200). It must be decoupled at the divider and each VREF input. Proper routing isolation is also needed for the VREF signal to prevent noise coupling. Additionally, the VREF input pins cannot be attached to the VTT termination supply rail.
- The DDRRESET is a LVCMOS signal using the VDDQ levels. This signal must have a pull down resistor.
- The DDRSLRATE signals are LVCMOS signals at the DVDD18 voltage.
- Follow the recommended length matching rules for address and command, control, clock and data lines.

- The routing rules must be followed for each routing group as given in the DDR3 design requirements. Similarly, recommended trace spacing is required to manage crosstalk.
- For Keystone-I devices, pay special attention to the sections that describe the impact of round trip delay and write leveling on routing.
- For more information, see *DDR3 design requirements for KeyStone devices*.
- For the KeyStone I hardware design guide, see the *Hardware design guide for KeyStone I devices*.
- For the KeyStone II hardware design guide, see the *Hardware design guide for KeyStone II devices*.

6.1.1 EMIF16

- Check that chip selects go to the proper memory for a correct memory map.
- Generally, series resistors can be used on the EMIF16 signals to reduce overshoot and undershoot. Acceptable values are 10 Ω, 22 Ω, or 33 Ω.
- The WAIT signals may have internal pull-down resistors. Be sure they are pulled-up sufficiently, if used.
- For address lines connection, see the *KeyStone architecture external memory interface (EMIF16) user's guide*
- Series termination resistors are recommended on all edge-latching signals like WE and CS.
- Series resistors are recommended on the bi-directional pins for long routes or when going off-board.

6.1.2 SerDes

- REFRES should be 3K 1% to ground.
- DC blocking caps are needed on the reference clock input.
- For layout requirements, see the *Serializer/Deserializer (SerDes) for KeyStone II Devices User Guide* and *SerDes Implementation Guidelines for KeyStone I Devices*, and so forth
- For unused pin connection, see the device-specific Hardware Design Guide. For the link, see Section 2.

6.1.3 HyperLink

- Series resistors should be implemented on the sideband signal clock outputs.
- DC blocking caps on the reference clock input - required for KS1 device family and implementation specific for KS2 device family.
- Keystone1 to Kesytone1 HyperLink SerDes data links can be DC coupled. All other HyperLink SerDes data links must be AC coupled.
- The HyperLink interface must be operated synchronously. A common clock source must be provided for both link partners.
- The P and N connections of a single pair can be swapped to simplify routing. RX pairs can be swapped with other RX pairs to simplify routing. Similarly, TX pairs can be swapped with other TX pairs to simplify routing.
- The SerDes pins (HYPLNK0TXNx and HYPLNK0TXPx) can be left unconnected, if unused.
- The HYPLNK0REFRES pin can be left unconnected if the hyperlink is not used.
- Routing must support 10 GBaud operation.
- Differential pairs must be length matched.
- DC blocking capacitors are required for data lanes and should be implemented on the RX end.
- The HyperLink differential TX and RX buffers contain on-chip termination resistors, so an external termination is not needed.
- If the HyperLink interface is not required, the HyperLink regulator power pin must still be connected to the correct supply rail with the appropriate decoupling capacitance applied.

6.1.4 PCIe

- DC blocking capacitors are required for data lanes and should be implemented on the TX end.
- Routing must support 5 GBaud operation.
- Differential pairs must be length matched.
- The PCIe differential TX and RX buffers contain on-chip termination resistors, so an external termination is not needed.
- If the PCIe interface is not required, the PCIe regulator power pin must still be connected to the correct supply rail with the appropriate decoupling capacitance applied.

6.1.5 SRIO

- Routing must support 5 GBaud operation.
- Differential pairs must be length matched.
- DC blocking capacitors are required for data lanes and should be implemented on the RX end.
- The SRIO differential TX and RX buffers contain on-chip termination resistors, so an external termination is not needed.
- If the SRIO interface is not required, the SRIO regulator power pin (VDDR4_SRIO) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied.

6.1.6 SGMII

- Routing must support 1.25 GBaud operation.
- Differential pairs must be length matched.
- DC blocking capacitors are required for data lanes and should be implemented on the RX end.
- The SerDes receiver includes a 100 Ω internal termination, so an external 100 Ω termination is not needed.
- If both of the SGMII interfaces are not used, the SGMII regulator power pin (VDDR3_SGMII) must still be connected to the correct supply rail with the appropriate decoupling capacitance applied.
- Both SRIO and SGMII interfaces must be unused in order to pull-up the unused clock signal (SRIOSGMIICLK) for devices that have these combined.

6.1.7 MDIO

- MDIO and MDC are 1.8V LVCMOS.
- MDIO requires a 1.5K pull up resistor.
- Clock buffering maybe required on MDC signal if routed with more than one load.
- Note that MDIO connections to PHYs may need level translation to 2.5 V or 3.3 V.

6.1.8 TSIP

- Series resistors should be used on clock sources because the TSIP clock inputs are edge-sensitive. These resistors need to be placed near the signal source.
- If any of the TSIP inputs are not used, they can be left floating because all TSIP pins have internal pull-down resistors.

6.1.9 I2C

- The KeyStone devices I2C pins are open drain IOs, and require pull-up resistors to DVDD18 rail. The recommended pull-up resistor is 4.7KΩ on SCL and SDA lines.
- If the I2C signals are not used, it is recommended that the SDA and SCL pins be pulled up to 1.8 V (DVDD18). These pins can be left floating, but this will result in a slight increase in power consumption due to increased leakage.
- The 1.8 V I2C pins are not tolerant to higher voltages. The PCA9306 dual bidirectional I2C level shifter is recommended when connecting to higher voltage I2C busses like 2.5 V or 3.3 V.

6.1.10 SPI

- Series termination resistor is recommended for clock output. Clock buffering may be needed if multiple devices are attached.
- The SPI interface is intended to operate at 1.8 V. Connection between the device SPI interface and peripheral must be at a 1.8-V level to assure functionality and avoid damage to either the external peripheral or KeyStone device.
- Make sure chip selects are properly allocated.

6.1.11 UART

- The UART interface is intended to operate at 1.8 V. UART interface and an external peripheral must be at a 1.8 V level.

6.1.12 I/O Buffers and Termination

- Series impedance is not always needed but is useful for some interfaces to avoid over-shoot and under-shoot problems. Check the recommendations in the peripherals sections or perform IBIS simulations on each interface.

7 Recommendations Specific to KeyStone II Devices

7.1 Peripherals

7.1.1 USB

- The USB reference clock must be AC coupled with 100 Ω termination between them.
- RESREF connection to ground through a 200 Ω, 1% resistor used for termination tuning and other internal analog references in the PHY.
- The connection diagram for USB3.0 host/device and USB2.0 host/device are shown in Figure 5 through Figure 8.
- VPP, VPPTX, VDDUSB, VPH pins should be connected to their respective power groups via recommended filtering circuit as outlined in the device-specific Hardware Design Guide. For the link, see Section 2.
- The input pin USBVBUS is only 5 V tolerant when the DVDD18 and DVDD33 supplies are valid. It is not 5 V tolerant prior to that time. A power switch in series between the VBUS pin on the USB connector and the USBVBUS pin can be disabled when the DVDD18 and DVDD33 supplies are not valid. The control for this switch should come from circuitry monitoring that these supplies are at valid levels.

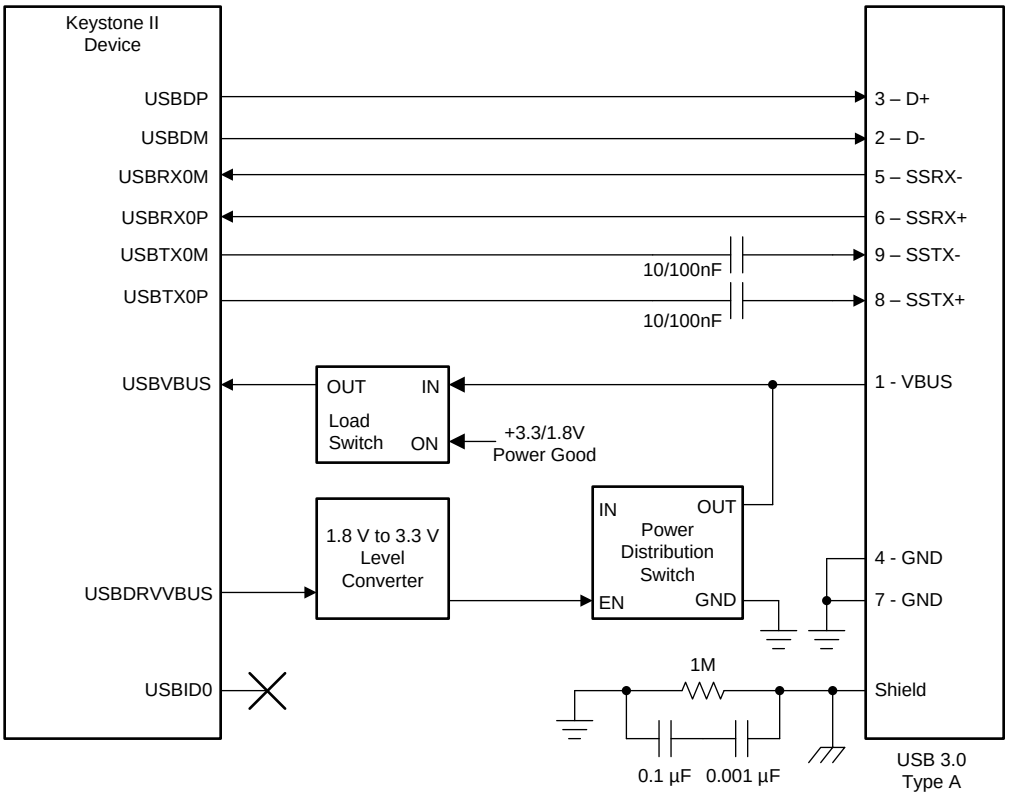

Figure 5. USB3.0 Host Connection

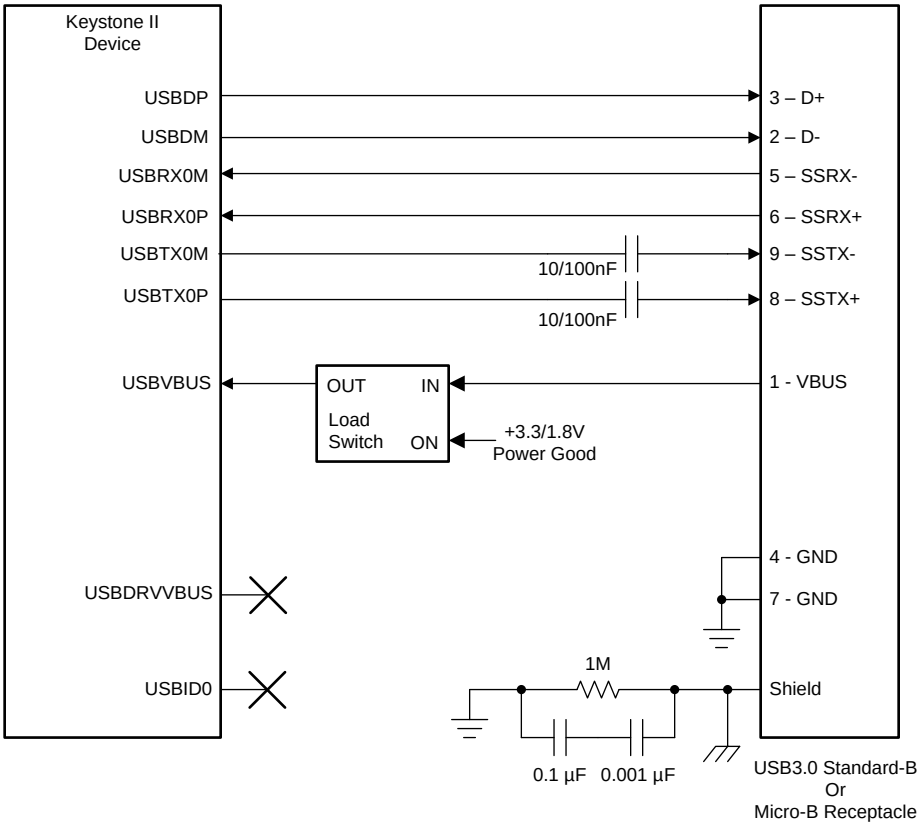

Figure 6. USB3.0 Device Connection

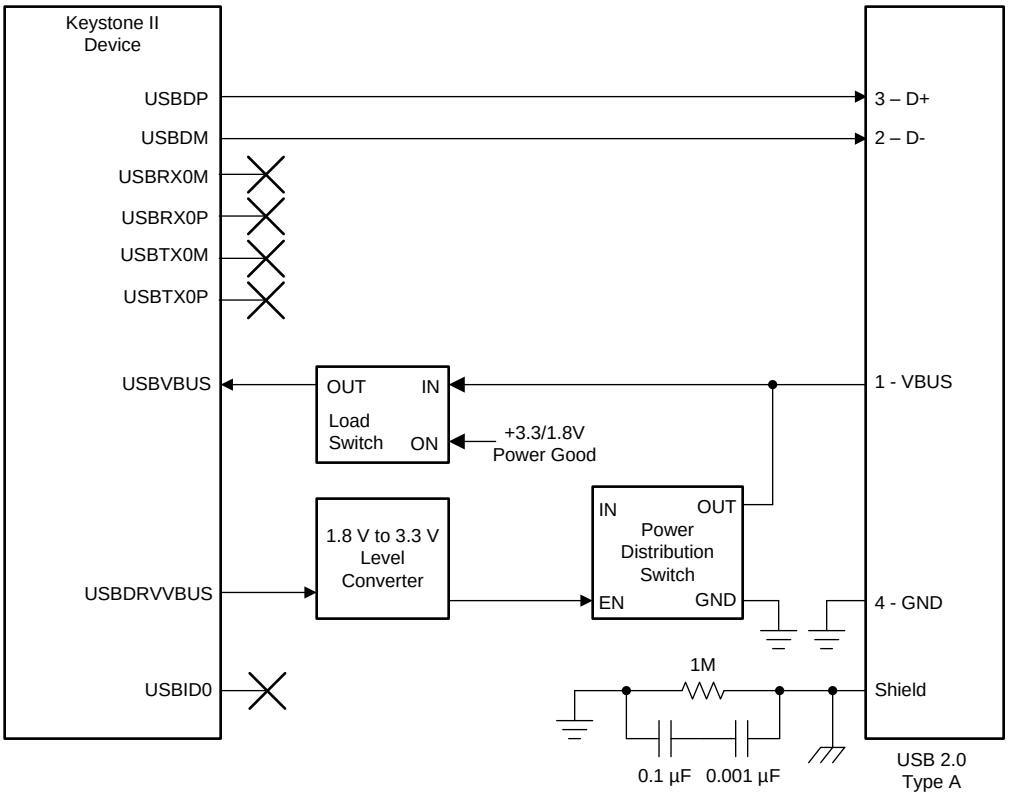

Figure 7. USB2.0 Host Connection

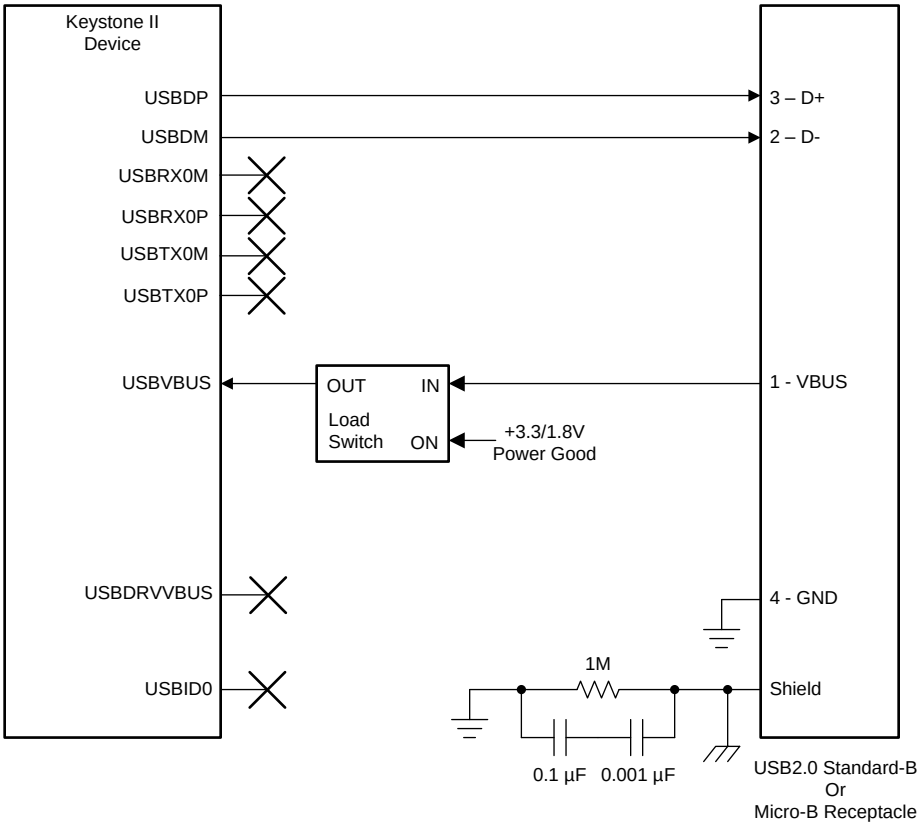

Figure 8. USB2.0 Device Connection

8 General Recommendations

As you are creating the schematics for your project here are a few things to consider.

8.1 Before You Begin

8.1.1 Documentation

Make sure you have the latest version of the documentation, especially the data sheet and silicon errata.

TIP: Try searching the documentation for words such as: "must", "require", "do not", "shall", "note:", and so forth. Important criteria for the device will typically contain one or more of these words. This is an easy way to make sure you have not missed anything important.

TIP: On each ti.com device product folder there is an "Alert me about changes to this product" button. Registration here enables proactive automatic notification of device errata.

8.1.2 Pinout

- Have you verified that your pin labels correspond to the correct pin numbers?
- Have you verified that the power pins are connected to the correct supply rails?
- Pullups/Pulldowns: If opposing an internal resistor use 1k resistor. To complement, use weaker value such as 4.7k resistor.

9 References

1. C6000 DSP + Arm Processors - Products
2. Other Sitara processors – Products
3. C6000 DSP - Products
4. ADVANTECH - EVMK2HX Evaluation Module
5. https://www.einfochips.com/
6. https://www.einfochips.com/partnerships-and-alliances/device-partnerships/texas-instruments/tms320c6657-evm/
7. ADVANTECH - TMDXEVM6678L Evaluation Module
8. K2E Clock Generation Reference Design - TIDEP0026
9. Power management
10. WEBENCH® Design Center
11. EETimes
12. Texas Instruments: *Hardware Design Guide for KeyStone I Devices*
13. Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
14. Texas Instruments: *DDR3 Design Requirements for KeyStone Devices*
15. Texas Instruments: *KeyStone Architecture External Memory Interface (EMIF16) User's Guide*
16. Texas Instruments: *SmartReflex™ Power and Performance Management Technologies*
17. Texas Instruments: *Remote Sensing for Power Supplies*
18. Texas Instruments: *AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML*
19. Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
20. Texas Instruments: *XDS Target Connection Guide*
21. *SerDes Implementation Guidelines for KeyStone I Devices*
22. *Serializer/Deserializer (SerDes) for KeyStone II Devices User's Guide*

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