Application Report
SPRACQ6–February 2020

AM65x/DRA80xM Silicon Revision 1.0 to 2.0 Migration Guide

ABSTRACT

This application report describes an overview of changes that should be considered when migrating AM65x/DRA80xM based designs from silicon revision 1.0 to silicon revision 2.0.

More information can be found in the AM65x/DRA80xM Processors Technical Reference Manual or respective data sheet located at:

- Silicon Revision 1.0: www.ti.com/lit/pdf/SPRSP08
- Silicon Revision 2.0: www.ti.com/lit/pdf/SPRSP52

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1 Hardware Design Changes

This section describes the hardware changes needed to migrate from silicon revision 1.0 to silicon revision 2.0.

1.1 Power Supply Voltage

The recommended operating condition values for VDD_CORE, VDD_MCU, VDD_MPU0, VDD_MPU1, VDD_WKUP0, VDD_WKUP1, VDD_DLL_MMC0, and VDD_DLL_MMC1 may change on silicon revision 2.0 devices. The values recommended for production products will not be available until the production data sheet is published. Meanwhile, TI recommends implementing adjustable output voltage power sources for these power rails when designing any product that migrates from silicon revision 1.0 to silicon revision 2.0. Fixed voltage power sources may be an option once the production data sheet has been published.

1.2 ADC0 Sample Rate Reduction

1.2.1 Problem Statement

The ADC0 and ADC1 design implemented in silicon revision 1.0 has high input leakage current that may impact ADC accuracy.

- ADC input leakage current may be higher than expected at worst-case Process/Voltage/Temperature (PVT) conditions, where process variation and operating temperature are the major contributors. Leakage current is larger for strong process devices operating at elevated temperatures.
- There is also a dependency on the potential applied to an ADC input. Leakage current flows out of the ADC when applying a potential equal to VSS, flows into the ADC when applying a potential equal to VDDA_ADC, and the direction change occurs at approximately 42% of VDDA_ADC. Magnitude of leakage current has a non-linear function to the applied potential, where it increases exponentially as the applied potential approached VSS or VDDA_ADC.

1.2.2 Design Considerations

Significant error can be introduced in ADC measurements when high impedance sources are connected to inputs with high leakage. This occurs because the input leakage current introduces a voltage drop across the source impedance. For example, the ADC would measure a potential of 1.45 volts when measuring a 1.5 volt source with 1K ohm output impedance connected to an ADC input with 50 uA of leakage flowing into the ADC input. The error of this measurement would be 50 millivolts, which is 3.3% lower than the expected value. Reducing the source impedance from 1K ohms to 100 ohms in this example would reduce the measurement error to 0.33%.

1.2.3 Minimizing Impact of Input Leakage on Silicon Revision 1.0

Use these design techniques to minimize the impact of input leakage.

- Reduce impedance of sources connected to ADC inputs. For example, it may be necessary to buffer outputs of high impedance sources with a voltage-follower operational amplifier.
- Design static DC sources to apply a nominal potential of approximately 42% of VDDA_ADC. For example, this approach can be used to minimize leakage when monitoring a DC power source through a resistor voltage divider.

1.2.4 Minimizing Impact of Input Leakage on Silicon Revision 2.0

ADC0 has been updated in silicon revision 2.0 to reduce input leakage.

- The largest contribution to input leakage is the size of each analog switch used to implement the 8:1 analog multiplexer that allows the ADC to be connected to one of eight inputs.
- Reducing the size of each analog switch is necessary to reduce input leakage. However, this increases the settling time of the applied signal, which reduces the maximum sample rate that can be achieved by the ADC.
- The maximum sample rate of ADC0 in silicon revision 2.0 has been reduced to 50k samples/sec, while

the maximum sample rate for ADC1 remains at 4M samples/sec.

- The worst case input leakage current for ADC0 is expected to be about 27 uA versus a worst case input leakage current of 572 uA for ADC1.

1.2.5 Summary of ADC0 Change on Silicon Revision 2.0

The ADC0 design implemented in silicon revision 2.0 has been updated to reduce input leakage current. However, this update reduces the maximum sample rate supported from 4M samples/sec to 50k samples/sec.

Products designed to use silicon revision 1.0 devices may require design updates when migrating to silicon revision 2.0. The following use cases are examples where product design changes need to be considered.

- ADC0 configured to operate at sample rates greater than 50k samples/sec.
- Product design could benefit from reduced input leakage current provided by ADC0.

1.3 I/O Power Supply Connections

1.3.1 Problem Statement

Internal I/O power supply connections of I/O cells associated with pins A23, B23, B24, and C24 were changed on silicon revision 2.0 devices.

- I/Os associated with pins A23 (MMC0_SDCD) and B23 (MMC0_SDWP) were originally connected to VDDSHV6, which is the MMC0 UHS-1 (8-bit) PHY I/O supply.
- I/Os associated with pins B24 (MMC1_SDCD) and C24 (MMC1_SDWP) were originally connected to VDDSHV7, which is the MMC1 UHS-1 (4-bit) PHY I/O supply.
- All four of these I/Os were disconnected from their previous supply rail and connected to VDDS_OSC1, which is the 1.8-V power supply for OSC1.

The original power supply rail connected to these I/O cells may need to change voltage dynamically for some applications. For example, in a use case where the respective MMCSD port is connected to a device that begins operation at 3.3 V and changes to 1.8 V when switching to a higher data transfer rate.

Internal power supply connections were changed because the I/O cells associated with these pins were not designed to support dynamic voltage change. VDDS_OSC1 was selected as the new power supply for these four I/O cells because it provided a fixed voltage supply while minimizing differences between silicon revisions.

1.3.2 Design Considerations

Pins associated with these four I/Os must only be used as inputs (their MMC0/MMC1 input functions or general purpose input functions) when OSC1 is being used with an external crystal. This restriction prevents any output buffer supply noise generated by the I/O cells from coupling into the oscillator supply. The output function of these pins can be used if OSC1 is connected to a 1.8-V LVCMOS reference clock source, or OSC1 is not used.

External circuits connected to pins associated with these four I/Os should be powered from the same power source to eliminate any risk of creating a non-fail-safe condition.

- A product designed to use silicon revision 1.0 should power all circuits connected to pins A23 and B23 from the same supply sourcing VDDSHV6, and power all circuits connected to pins B24 and C24 from the same supply sourcing VDDSHV7.

NOTE: Silicon revision 1.0 devices do not support dynamic voltage change of VDDSHV6 and VDDSHV7 because these four I/Os are powered from these power rails.

- A product designed to use silicon revision 2.0 should power all circuits connected to pins A23, B23, B24, and C24 from the same supply that is sourcing VDDS_OSC1. This allows dynamic voltage change to be supported on VDDSHV6 and VDDSHV7 power rails of silicon revision 2.0 devices.

1.3.3 Summary of I/O Power Supply Change on Silicon Revision 2.0

Products designed to use silicon revision 1.0 devices may require design updates when migrating to silicon revision 2.0. In most cases, a PCB could be designed with component installation options that allow external circuits to be powered from their respective VDDSHV6 or VDDSHV7 supply for silicon revision 1.0 devices or VDDS_OSC1 supply for silicon revision 2.0 devices.

1.4 ICSSG Pin Multiplexing Enhancements

1.4.1 Problem Statement

ICSSG0 and ICSSG1 implement pin multiplexing options for connecting a low latency 10/100 Mbps Ethernet PHY through the MII_RT interface, or a 10/100/1000 Mbps Ethernet PHY through the RGMII interface.

Five signal functions of each ICSSG MII_RT implemented in silicon revision 1.0 are assigned such that they did not match common Ethernet PHY signal function assignments which support similar pin multiplexing options for MII or RGMII. The original assignment of these five signal functions requires different connectivity between ICSSG and the PHY when operating in MII mode versus RGMII mode. This prevents a product from being designed with a common hardware connection topology for these signal functions.

There are use cases where a product could benefit from a common connection topology for these signal functions.

A common connection topology lets ICSSG be used with the Ethernet PHY MII interface or RGMII interface with minimum or no hardware changes. However, this requires ICSSG signal functions to be assigned to match the Ethernet PHY pin multiplexing assignments.

Silicon revision 2.0 is updated to provide additional pin multiplexing options for these five signal functions. This lets a product be designed with a common connection topology for Ethernet PHYs that support MII and RGMII interfaces with matching pin multiplexing options.

The original pin multiplexing options were retained and additional pin multiplexing options were implemented as described in Table 1 and Table 2.

Table 1. ICSSG0

Package Signal Name	Original MII_RT Assignment	Additional MII_RT Assignment[1]	RGMII Assignment
PRG0_PRU0GPO11	pr0_mii1_txd[0]	pr0_mii1_txen	pr0_rgmii1_tctl
PRG0_PRU0GPO12	pr0_mii1_txd[1]	pr0_mii1_txd[0]	pr0_rgmii1_td0
PRG0_PRU0GPO13	pr0_mii1_txd[2]	pr0_mii1_txd[1]	pr0_rgmii1_td1
PRG0_PRU0GPO14	pr0_mii1_txd[3]	pr0_mii1_txd[2]	pr0_rgmii1_td2
PRG0_PRU0GPO15	pr0_mii1_txen	pr0_mii1_txd[3]	pr0_rgmii1_td3
PRG0_PRU1GPO11	pr0_mii0_txd[0]	pr0_mii0_txen	pr0_rgmii0_tctl
PRG0_PRU1GPO12	pr0_mii0_txd[1]	pr0_mii0_txd[0]	pr0_rgmii0_td0
PRG0_PRU1GPO13	pr0_mii0_txd[2]	pr0_mii0_txd[1]	pr0_rgmii0_td1
PRG0_PRU1GPO14	pr0_mii0_txd[3]	pr0_mii0_txd[2]	pr0_rgmii0_td2
PRG0_PRU1GPO15	pr0_mii1_txen	pr0_mii0_txd[3]	pr0_rgmii0_td3

(1) Additional pin multiplexing options for each ICSSG0 MII_RT port are provided via Mux Mode 4.

Table 2. ICSSG1

Package Signal Name	Original MII_RT Assignment	Additional MII_RT Assignment[1]	RGMII Assignment
PRG1_PRU0GPO11	pr1_mii1_txd[0]	pr1_mii1_txen	pr1_rgmii1_tctl
PRG1_PRU0GPO12	Pr1_mii1_txd[1]	pr1_mii1_txd[0]	pr1_rgmii1_td0
PRG1_PRU0GPO13	pr1_mii1_txd[2]	pr1_mii1_txd[1]	pr1_rgmii1_td1
PRG1_PRU0GPO14	pr1_mii1_txd[3]	pr1_mii1_txd[2]	pr1_rgmii1_td2
PRG1_PRU0GPO15	pr1_mii1_txen	pr1_mii1_txd[3]	pr1_rgmii1_td3
PRG1_PRU1GPO11	pr1_mii0_txd[0]	pr1_mii0_txen	pr1_rgmii0_tctl
PRG1_PRU1GPO12	pr1_mii0_txd[1]	pr1_mii0_txd[0]	pr1_rgmii0_td0
PRG1_PRU1GPO13	pr1_mii0_txd[2]	pr1_mii0_txd[1]	pr1_rgmii0_td1
PRG1_PRU1GPO14	pr1_mii0_txd[3]	pr1_mii0_txd[2]	pr1_rgmii0_td2
PRG1_PRU1GPO15	pr1_mii1_txen	pr1_mii0_txd[3]	pr1_rgmii0_td3

(1) Additional pin multiplexing options for each ICSSG1 MII_RT port is provided via Mux Mode 5.

1.4.2 Design Considerations

The original pin multiplexing assignment of these five signal functions required using one of the following three options when connecting ICSSG to the Ethernet PHY.

The first option is designing a PCB with these ICSSG signal functions connected to the appropriate MII PHY pins or RGMII PHY pins, where a single mode of operation is supported and connectivity is based on a pre-determined mode of operation.

The second option is designing a PCB with 0-Ω resistor installation options, which connects ICSSG to MII PHY pins or RGMII PHY pins through a BOM change.

The third option is designing a PCB with dynamic switching logic, which connects ICSSG to MII PHY pins or RGMII PHY pins through a software change. However, the switching logic circuit must be designed to support signal integrity and insertion delay requirements of RGMII.

1.4.3 Summary of ICSSG Pin Multiplexing Enhancements on Silicon Revision 2.0

The additional pin multiplexing options provided in silicon revision 2.0 allows a common PCB design to be used when ICSSG is using MII_RT or RGMII.

NOTE: Some Ethernet PHYs do not multiplex the MII and RMII transmit clocks on a common pin. For example, DP83867 uses separate pins, whereas DP83869 uses a common pin. The hardware platform must address transmit clock connectivity differences when using an Ethernet PHY with separate transmit clock pins if the product is required to support MII mode and RGMII mode with a common hardware platform.

1.5 Series Termination on MMC0_CLK and MMC1_CLK

Pins associated with MMC0_CLK and MMC1_CLK on silicon revision 1.0 devices operate as an output while also operating as a retiming input to internal synchronization circuits.

The MMCSD host controller sources a clock to the pin which provides a reference clock to the attached device, but the clock is also looped back into the host controller. A series source termination resistor is required on silicon revision 1.0 devices to help eliminate potential glitches on the looped-back clock as the result of signal distortion that occurs on the source end of the PCB signal trace.

The looped-back clock has been removed from pins associated with MMC0_CLK and MMC1_CLK on silicon revision 2.0 devices. Therefore, the requirement of including a series source termination resistor on these pins has been eliminated for silicon revision 2.0 devices.

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