Application Note

AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Schematic Design and Review Checklist

ABSTRACT

This application note summarizes schematics design and review guidelines and recommendations to be followed by board designers using any of the AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 family of processors. The guidelines include possible processor configurations and care about for interfacing different processor peripherals to attached (external) devices.

Additionally, links are provided for processor product page, related collaterals, E2E FAQs and other commonly referenced documents that could help the board designers optimize the design efforts and schedule during custom board design.

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Trademarks

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1 Introduction

This application note applies to all the family of processors listed below. Product related documentation is available on the product pages on TI.com. Click the processor link below for accessing the product page.

1.1 AM62x Processor Family

1.1.1 AM625

- AM6254
- AM6252
- AM6251

1.1.2 AM623

- AM6234
- AM6232
- AM6231

1.1.3 AM625SIP

- AM6254

1.1.4 AM625-Q1

- AM6254
- AM6252

1.1.5 AM620-Q1

- AM6204
- AM6202
- AM6201

1.2 AM62Ax Processor Family

1.2.1 AM62A7

- AM62A74

1.2.2 AM62A7-Q1

- AM62A74

1.2.3 AM62A3

- AM62A34
- AM62A32
- AM62A31

1.2.4 AM62A3-Q1

- AM62A34
- AM62A32

1.3 AM62Px Processor Family

1.3.1 AM62P

- AM62P54
- AM62P52
- AM62P34
- AM62P32

1.3.2 AM62P-Q1

- AM62P54

2 Related Collaterals

2.1 Links to Commonly Available and Applicable Collaterals

A number of documents relevant to the selected processor are available on the processor product page on TI.com. It is strongly recommended to read through these documents before starting the custom board design.

The links below summarizes the collaterals that can be referred when starting the custom board design.

2.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

[FAQ] AM625 Custom board hardware design – Collaterals to Get started

[FAQ] AM623 Custom board hardware design – Collaterals to Get started

[FAQ] AM625SIP Custom board hardware design – Collaterals to Get started

[FAQ] AM625-Q1 / AM620-Q1 Custom board hardware design – Collaterals to Get started

2.1.2 AM62A7 / AM62A3

[FAQ] AM62A7 / AM62A7-Q1 Custom board hardware design – Collaterals to Get started

[FAQ] AM62A3 / AM62A3-Q1 Custom board hardware design – Collaterals to Get started

2.1.3 AM62P / AM62P-Q1

[FAQ] AM62P / AM62P-Q1 Custom board hardware design – Collaterals to Get started

2.2 Hardware Design Guide

It is recommended to read through the processor specific *Hardware Design Guide* before starting the custom board design for the recommended steps to be followed. Refer the device-specific (processor specific) *Hardware Design Guide* linked below:

2.2.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

Hardware Design Guide for AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Family of Processors.

2.2.2 AM62A7 / AM62A3

Hardware Design Guide for AM62A7 / AM62A3 Family of Processors.

2.2.3 AM62P / AM62P-Q1

Hardware Design Guide for AM62P / AM62P-Q1 Family of Processors.

3 Processor Selection

3.1 Data Sheet

Processor specific data sheet includes pin attributes (pin to function mapping), pin description, timing information and diagrams for all the applicable processor peripherals and recommended operating conditions for all the supply rail.

To get an overview of the processor architecture and for selecting the processor variant, features, package (ALW / AMC / AMK / AMB / AMH) and speed grade, refer the *Functional Block Diagram* and *Device Comparison* sections of the device-specific (processor specific) data sheet.

3.2 Peripheral Instance Naming Convention

For naming the peripherals and instances, the device-specific TRM tends to be generic and the device-specific data sheet is specific.

In the data sheet a suffix number is assigned even when there is only one peripheral instance, so any documents that reference the peripheral name will not need to change from processor to processor.

The suffix starts with “0”. For the CPSW3G port names, port “0” is the internal (CPPI host) port of the switch.

3.3 Device Ordering and Quality

For information related to ordering and quality for the selected family of processor, see the links below:

AM625-Ordering & quality

AM623-Ordering & quality

AM625SIP-Ordering & quality

AM625-Q1-Ordering & quality

AM620-Q1-Ordering & quality

AM62A7-Ordering & quality

AM62A7-Q1-Ordering & quality

AM62A3-Ordering & quality

AM62A3-Q1-Ordering & quality

AM62P-Ordering & quality

AM62P-Q1-Ordering & quality

4 Power Architecture

To get an overview of the power solutions available, see the TI Power management page.

Additionally, WEBBENCH circuit designer tool provides a visual interface that delivers required power application.

4.1 Generating Supply Rails

The required supply rails for the selected processor can be generated using integrated or discrete power architecture. Use of integrated power architecture (PMIC) simplifies design of processor specific power architecture (power supplies). The PMIC generates supplies commonly used to power the processor and the attached devices, allows supply power-up and power-down sequencing, supply ramp control and meeting all the processor specific power requirements. Along with the PMIC, additional DC/DC converters and LDOs can be used to generate additional on-board supplies based on use case.

Discrete power architecture provides flexibility in design and component selection. Board designer has to take care of the power device selection that can source the required load current, provide the required output voltage, support required load transient response, control supply ramp and supply sequencing.

Processor power supply rails have slew rate requirements specified. Follow the section *Power Supply Slew Rate* of device-specific data sheet for all the generated or switched supply rails.

Recommended family of devices and related collaterals for generating the on-board supplies using different power architectures are summarized below:

4.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

4.1.1.1 PMIC (Power Management IC)

Recommended PMIC for integrated power architecture includes TPS65219. The space, performance and BOM optimized power architecture is designed to power the processor and the attached devices.

TPS65219 has multiple variants and each of the variant has a fixed supply output configuration. Choose the required variant based on the design requirement. To choose the required variant, see the TPS65219 product page. *Schematic and Layout Checklist* is available that can be used during the custom board design.

For the full application note and operational details, refer below:

Powering the AM62x with the TPS65219 PMIC

Powering the AM625SIP with the TPS65219 PMIC

4.1.1.1.1 Additional Reference

For more information, see the below section of the device-specific data sheet.

Device Connection and Layout Fundamentals, Power Supply, Power Supply Designs

4.1.1.2 Discrete Power

A discrete power architecture could be used to generate the processor and the attached devices supply rails. Discrete power architecture is based on DC/DC converters and LDOs. The power sequence has to be implemented using the power good output and discrete logic.

For more information on the device selection and power architecture implementation, refer *Discrete Power Solution for AM62x*.

4.1.1.2.1 DC/DC Converter

DC/DC Converters such as TPS62826, LM61460-Q1 devices can be considered.

To get an overview of the DC/DC Converters available, see the TI Buck converters (integrated switch) page.

4.1.1.2.2 LDO

LDOs such as TPS74518, TLV7103318, TLV75518 devices can be considered.

To get an overview of the LDOs available, see the TI Linear & low-dropout (LDO) regulators page.

4.1.2 AM62A7 / AM62A3

4.1.2.1 PMIC

Recommended PMIC for integrated power architecture includes TPS6593-Q1. The space, performance and BOM optimized power architecture is designed to power the processor and the attached devices.

For implementation, refer the *Starter Kit SK-AM62A-LP* schematic.

Alternate PMIC recommendation includes TPS65224-Q1. For automotive functional safety use cases, connect MCU_I2C0 of the processor to PMIC (TPS65224/2) I2C1.

4.1.2.2 Discrete Power

A discrete power architecture could be used to generate the processor and the attached devices supply rails. Discrete power architecture is based on DC/DC converters and LDOs. The power sequence has to be implemented using the power good output and discrete logic.

Currently there is no discrete power architecture implementation available.

To get an overview of available solution, see the processor (AM62A7 / AM62A3) product page.

4.1.3 AM62P / AM62P-Q1

4.1.3.1 PMIC

Recommended PMIC for integrated power architecture includes TPS65224-Q1. The space, performance and BOM optimized power architecture is designed to power the processor and the attached devices.

For automotive functional safety use cases, connect MCU_I2C0 of the processor to PMIC (TPS65224/2) I2C1.

For implementation (without functional safety), refer the *Starter Kit SK-AM62P-LP* schematic.

4.1.3.2 Discrete Power

A discrete power architecture could be used to generate the processor and the attached devices supply rails. Discrete power architecture is based on DC/DC converters and LDOs. The power sequence has to be implemented using the power good output and discrete logic.

Currently there is no discrete power architecture implementation available.

To get an overview of available solution, see the processor (AM62P / AM62P-Q1) product page.

4.2 Power Control and Protection

4.2.1 Load Switch

Load switches could be used to turn on and off power to a specific peripheral or sub-system powered by the same supply level rail instead of using multiple DC/DC converters or LDOs to generate the supply. In some applications, there is a strict power-up and power-down sequence that must be followed. Load switches simplifies the implement power sequencing to meet the power-up and power-down requirements. The load switch enable could be controlled by the PMIC or DC/DC converter to comply with the processor power sequencing requirements.

Load switches such as TPS22965, TPS22918, TPS22902, TPS22946 devices can be considered.

To get an overview of the Load switches available, see the TI Load switches page.

4.2.2 eFuse

eFuses are integrated power path protection devices that are used to limit circuit current, voltages to safe levels during fault conditions. eFuses offer many benefits to the design and can include protection features that are often difficult to implement with discrete components. To get an overview of the eFuses available, see the TI eFuses & hot swap controllers page.

5 General Recommendations

Here are the recommendations and guidelines for board designers to be familiar while designing the custom board.

5.1 Processor Performance Evaluation Module (SK - Starter Kit)

Processor (hardware) performance evaluation modules/platforms (SKs) are not to be considered as a reference design. They are evaluation platforms and may not represent a proper or complete board or system implementation. In many cases, the SKs are partially or completely designed and released for fabrication much before the processor design is complete. This is done so that a hardware platform is available when first silicon arrives. It is possible to learn new processor requirements during processor bring-up and bench validation. If so, these new requirements may not be accounted for in the hardware evaluation platform. Therefore, TI expects customers to carefully review and follow all requirements defined in the device-specific data sheet, silicon errata, and TRM when designing the custom board.

Processor (hardware) performance evaluation platforms were not designed to be comprehensive of any board or system specific requirements, like EMI / EMC purpose (reduce radiated emissions), noise susceptibility, thermal management and so forth.

Refer below FAQ for design update note that customers could refer along with the SK schematics

[FAQ] AM625 / AM623 / AM62A Common design Errors / Recommendations for Custom board hardware design – SK Schematics Design Update Note.

5.2 Device-Specific (Processor-Specific, Processor-Family Specific) SK Versus Data Sheet

During evaluation or the custom board design, in case of any discrepancy between the device-specific SK and the data sheet, it is recommended to follow the data sheet. Despite the best efforts by the board designer, the SK may contain errors that still function but are not completely aligned with the data sheet specifications.

5.2.1 Notes About Component Selection

Selection of SK components may not be the most optimized. Review the BOM and optimize the component selection based on the data sheet recommendations, application requirements and board circuit design.

Design calculations, design review and performing board level tests and measurements as required is recommended before finalizing the components value and ratings (Voltage, Power).

5.2.1.1 Series Resistor

The recommended value for the series resistors are simply a starting point for board designers and should be verified on the board and adjusted accordingly (Step function that occurs on this pin is not near the mid-supply).

5.2.1.2 Parallel Pull Resistor

Provide provision for adding parallel pulls to the processor IOs. Parallel pull polarity and the values are dependent on the specific peripheral connectivity recommendations, recommendations for improved processor performance and relevant interface or standards requirements.

Device-specific SK pull values can be used as a starting point and board designers can choose the appropriate pull values based on the recommendations for the processor and attached device or specific board design implementation.

When a trace is connected to the processor pads and not being actively driven, a parallel pull is recommended (pull polarity is customer use case dependent). During power-up, processor IO buffers are off and the IOs are in high impedance state (effectively an antenna that will pick up noise). Without any termination, these signal are very high impedance. This makes it easy for noise to couple energy on these floating signal trace and develop a potential that could exceed our recommended operating conditions, which would create an Electrical Over-Stress (EOS) on the IOs. ESD protection circuits inside the processor were only designed to protect the device from handling before being installed on a PCB assembly.

5.2.1.3 Drive Strength Configuration

We do not support any other drive strength besides the nominal value for peripherals and LVCMOS buffers as that is the only one at which chip-level STA (Static Timing Analysis) has been closed. The nominal value corresponds to a 40 Ω driver. The IBIS model has been updated to contain only those drive strengths where the timing has been closed internally.

5.2.1.4 Data Sheet Recommendations

The board designers are responsible for implementing whatever precautions are necessary (required) to ensure their custom board design does not violate the requirements mentioned (specified) in the processor specific data sheet. Example processor requirement: I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics - Input Slew Rate.

When data sheet recommendations are not available, recommendations provided in this checklist or implementation in the SK schematics can be used as a starting point.

5.2.1.5 Processor IOs - External ESD Protection

An external ESD protection is recommended to any of the processor IOs connected directly to an external connector or exposed to external inputs, since internal ESD protection was not designed to handle the board (or system) level ESD requirements. To get an overview of the ESD protection devices and solutions available, see the TI ESD & surge protection ICs page.

5.2.1.6 Peripheral Clock Output Series Resistors

The series resistor on the clock output is required to resolve issues with signal distortion at the source of the clock signal because the clock output is also used for retiming. For MMCx interface an unbonded pad is used in

the AM62x, AM62Ax and AM62Px processor family, so the series resistor is not a requirement for loopback. In some cases a low value series resistor may be needed for EMI / EMC purpose (reduce radiated emissions). It is recommended to keep the series resistor as a place holder just in case it is needed for improving signal integrity.

5.2.2 Additional Information Regarding Reuse of SK Design

5.2.2.1 Design Notes Added on the SK Schematics

Based on the use case design, a number of *Design Update Notes* and *Schematics Design Review Notes* are added as guidelines that could support board designers during board optimization and final assembly BOM review. It is highly recommended that customers read these notes before the start of the design and during the board design.

5.2.2.2 SK Design Files Reuse

Based on the design process followed during the custom board design and project schedule, it is okay to reuse the SK design files as a starting point and make the required updates. It is recommended that customer verify the SK implementation and component selection.

The links below summarizes the considerations board designers are required to be familiar when reusing TI SK design files.

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design - Reusing TI SK (EVM) design files

[FAQ] AM62A7 / AM62A3 Custom board hardware design - Reusing TI SK (EVM) design files

[FAQ] AM62P / AM62P-Q1 Custom board hardware design - Reusing TI SK (EVM) design files

5.3 Before You Begin The Design

5.3.1 Documentation

During the entire custom board design cycle, it is recommended to always refer or use the latest version of the documentation, examples include the device-specific data sheet, silicon errata, TRM and other commonly referenced design collaterals. Verify the processor specific product page for the latest available documents or addition of new documents.

Tips for documentation search: Try searching the documentation for words such as: "recommended", "require", "do not", "note", "pin connectivity" and so forth. Important criteria for the processor typically contain one or more of these words. This is an easy way to make sure not missed anything important.

Tips to get updated information: On TI.com, processor product page, there is a "Notifications" button. Registering here enables automatic notification of processor documentation changes.

5.3.2 Processor Pin Attributes (Pinout) Verification

- Verify the processor pin label correspond to the correct pin numbers listed in the *Pin Attributes* section of the device-specific data sheet. Main the data sheet names in the symbol and change the net names as per the application use case.
- Verify the supply voltages connected to the processor power pins are within the *Recommended Operating Conditions*.
- All the processor pins (grouped into functions and having separate symbol blocks) including reserved pins are include and in the schematics to minimize tool related and functional errors.
- Many of the processor IOs TX and RX buffers and pulls are turned off by default. External pull resistors are recommended to hold inputs of any attached device in a valid logic state until software initializes the IOs. Use of pull resistor is depends on the attached device IO capabilities.
- For improved custom board performance, recommend implementing external monitoring of voltage, current or temperature.

5.3.3 Device Comparison and IOSET

Refer to the note regarding shared IO pins in *Device Comparison* section of the device-specific data sheet. IOSETs are a collation (grouping) of signals specific to an interface that are timed as a set. The processor

is timing closed using IOSETs. Any interface that has IOSETs must select all interface signals from the same IOSET. Some interface signals may be shared over multiple IOSETs. The valid pin combinations are detailed in the SysConfig-PinMux tool.

5.3.4 Note on PADCONFIG Registers

Many of the processor IOs support multiplexing of functions. The IO function can be chosen from multiple functions. The list of functions available for each pad is enumerated in *SIGNAL NAME* column in the *Pin Attributes* table of the device-specific data sheet.

The desired function is selected via the MUXMODE field of the associated pad configuration register. The PADCFG_CTRL0_CFG0_PADCONFIG0 to PADCFG_CTRL0_CFG0_PADCONFIG150 registers control the signal multiplexing of IOs in the processor Main Domain and MCU_PADCFG_CTRL0_CFG0_PADCONFIG0 to MCU_PADCFG_CTRL0_CFG0_PADCONFIG33 registers control the signal multiplexing of IOs in the processor MCU Domain.

The *Pad Configuration Ball Names* table in the *Pad Configuration Registers* section of the device-specific TRM summarizes the Bit Field Reset Values for all the PADCONFIG registers. Follow the notes listed at the end of the table while configuring the PADCONFIG registers. The RXACTIVE bit must never be set without a valid logic state being sourced to the pin associated with the respective PADCONFIG register. This is important since a floating input could damage the processor or affect reliability.

5.3.5 Processor IO (Signal) Isolation for Fail-Safe Operation

In case the processor and the attached devices or an additional host are powered by different power sources, signal isolation is recommended since most of the processor IOs are not fail-safe. It is recommended to route the signals through a FET bus switch circuit designed to automatically isolate the two devices anytime the IO power is not valid for both devices. The FET bus switch and control logic are recommended to be powered from an always on power supply and only enabled by an AND function of power good signals from different power sources.

5.3.6 Reference to Device-Specific SK

For implementation (when specific recommendations are not available in the device-specific data sheet) examples and values, see the device-specific SK, as applicable.

5.3.7 High-Speed Interface Design Guidelines

For detailed recommendations on USB2.0 and CSI-Rx signals connection and routing, see the *High-Speed Interface Layout Guidelines*. Include appropriate constraints or routing requirements to be followed during the custom board design.

For USB interface, a common-mode choke could be added for improving the custom board performance when operating in harsh industrial environment. Provide provision to bypass the common-mode choke using 0 Ω resistors. Consider adding external ESD protection based on the application requirement.

5.3.8 Recommended Current Source or Sink for LVCMOS (GPIO) Outputs

The DC current outputs sourced should remain less than the maximum I_{OH} and I_{OL} values defined to achieve the V_{OL} max and V_{OH} min values defined in the respective *Electrical Characteristics* table. It is not recommended to Source/Sink currents above the limits defined in the device-specific data sheet and it is preferred that the DC current Source/Sink is significantly less that these limits because it can contribute to thermal or other problems.

Example, switching these high current levels could create a lot of electrical noise that could couple to other circuits and require additional decoupling capacitors on the respective IO power rail.

5.3.9 Connection of Slow Ramp Inputs or Capacitors to LVCMOS IOs (Inputs or Outputs)

LVCMOS inputs have slew rate requirements specified. Connecting slow ramp signal directly to the LVCMOS inputs or capacitors at the LVCMOS inputs is not recommended. When slow ramp input is applied, CMOS input will have shoot-through current that flows from VDD through the partially turned on P-channel transistor and the partially turned on N-channel transistor to VSS when the input is at mid-supply. Accumulated exposure to slow ramps could result in performance or reliability concerns.

LVCMOS output buffers were not designed to drive large capacitive loads. For LVCMOS type IOs when configured as output and connected to capacitive load, follow the data sheet recommendations for the allowed capacitor value or add series resistor to limit the current or perform simulations.

5.3.10 Queries and Clarifications Related to Processor During Custom Board Design

For queries and clarifications related to processor selection, features and guidelines, TI recommends using the E2E forum. E2E can be used to ask new questions or refer to related questions that have been previously answered.

6 Processor Specific Recommendations

6.1 Common (Processor Start-Up) Connection

6.1.1 Power Supply

Follow the recommendations listed below:

- The power requirement for each of the supply rail varies based on the interfaces used and the operating environment.

- The current draw of processor supply rails can be estimated using the *PET (Power Estimation Tool)*. If the supply rail powers the other on-board attached (peripheral) devices, the maximum current draw of these devices needs to be included.
- Verify if the output current ratings of the selected power architecture (including PMIC, DC/DC converters and LDOs) meet the maximum current requirements of processor and all attached devices. It is recommended to add some additional margin for design variances.
- Verify if the recommended power supply sequence (Power-Up and Power-Down) is being followed. Proper power supply sequencing in correlation with resets and clocks is recommended. For the recommended power sequencing requirements, refer the *Power Supply Sequencing* section of device-specific data sheet.

6.1.1.1 Supply for Core and Peripherals

For proper operation, all power pins (balls) must be supplied with the supply voltages recommended in the *Recommended Operating Conditions* section of the device-specific data sheet. Power pins that have specific connectivity requirements are specified in the *Pin Connectivity Requirements* section of the device-specific data sheet.

Note

Powering the MCU Domain and the MAIN Domain independently is not an option. The processor does not have separate MCU and Main power domains. All power rails must be powered, and they must be sequenced as defined in the device-specific data sheet. The concept of MCU and Main only applies to internal device functions and processor domains.

6.1.1.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 and AM62A7 / AM62A3

Core supplies VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 (available on the AMC and AMB packages) are recommended to be powered by the same power source and can be operated at 0.75 V or 0.85 V (valid operating ranges defined in the Recommended Operating Conditions (ROC) table). When these supplies are operating at 0.75 V, it is recommended to ramp 0.75 V prior to all 0.85 V supplies. Setting the core supply to 0.8 V is not an allowed option and there is no range defined for a nominal operating voltage of 0.8 V.

VDDR_CORE is specified to operate only at 0.85 V. When VDD_CORE is operating at 0.85 V, VDD_CORE and VDDR_CORE are recommended to be powered by the same source (ramp together).

VDDS_OSC0 and VDDA_MCU supplies are recommended to be connected always.

The processor includes multiple analog supply pins that provide power to sensitive analog circuitry like VDDA_MCU, VDDA_PLLx [x=0..2 for AM62x and x=0..4 for AM62Ax], VDDA_1P8_CSIRX0, VDDA_1P8_OLDI0 (AM62x) and VDDA_1P8_USB. Filtered (ferrite) power supplies are recommended.

For more information, refer the *Recommended Operating Conditions* and *Power Sequencing* sections of the device-specific data sheet.

6.1.1.1.2 AM62P / AM62P-Q1

Core supplies VDD_CORE, VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB, and VDDA_DDR_PLL0 are recommended to be powered by the same power source and can be operated at 0.75 V or 0.85 V. (valid operating ranges defined in the ROC table). When these supplies are operating at 0.75 V, it is recommended to ramp 0.75 V prior to all 0.85 V supplies. Setting the core supply to 0.8 V is not an allowed option and there is no range defined for a nominal operating voltage of 0.8 V.

Core supplies VDD_MMC0 and VDDA_0P85_DLL_MMC0 are specified to operate at 0.85 V when MMC0 is used. It is recommended to connect VDD_MMC0 and VDD_0P85_DLL_MMC0 to the same power source as VDD_CORE when MMC0 is not used.

VDDR_CORE is specified to operate only at 0.85 V. When VDD_CORE is operating at 0.85 V, VDD_CORE and VDDR_CORE are recommended to be powered by the same source (ramp together).

VDDS_OSC0 and VDDA_MCU supplies are recommended to be connected always.

The processor includes multiple analog supply pins that provide power to sensitive analog circuitry like VDDA_MCU, VDDA_PLLx [x=0..4], VDDA_1P8_CSI_DSI and VDDA_1P8_OLDI0. Filtered (ferrite) power supplies are recommended.

For more information, refer the *Recommended Operating Conditions* and *Power Sequencing* sections of the device-specific data sheet.

6.1.1.1.3 Additional Information

For more information on processor power-sequencing requirements, see the below FAQ:

[FAQ] AM625 / AM623 Custom board hardware design – Processor power-sequencing requirements for power-up and power-down.

For more information on processor power supply rails filtering using ferrite, see the below FAQ:

[FAQ] AM625 / AM623 Custom board hardware design – Ferrite (power supply filter) recommendations for SoC supply rails.

These are generic FAQs and can also be used for AM625SIP / AM625-Q1 / AM620-Q1, AM62A7 / AM62A3 and AM62P / AM62P-Q1 family of processors.

6.1.1.2 Supply for IO Groups

6.1.1.2.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 and AM62A7 / AM62A3

The processor includes nine Dual-voltage IO domains (VDDSHVx [x = 0..6], VDDSHV_CANUART and VDDSHV_MCU), where each domain provides power supply to a fixed set of IOs. Each IO domain can be configured for 3.3 V or 1.8 V independently, which determines a common operating voltage for the entire set of IOs powered by the respective IO domain power supply.

Processor pads (pins) designated as CAP_VDDSx [x=0..6], CAP_VDDS_CANUART and CAP_VDDS_MCU are provided for connecting an external capacitor to the internal LDO. A 1-µF (to be connected between these pins and VSS, see the device-specific data sheet,) capacitor is recommended. Refer device-specific data sheet for the recommended capacitor voltage rating.

The capacitors are expected to be placed on the back side of the PCB in the array of the BGA to meet the loop inductance requirements. Choice of capacitor voltage rating could influence the capacitor package (size) selection.

Select a capacitor with ESR < 1 Ω. Ensure board trace connection loop inductance is < 2.5-nH.

The capacitor value recommended does not include variations in value considering DC bias and degradation over time. The capacitor value is independent of IO count and activity. It is required for stability of the LDO to generate BIAS supply. Any value beyond the recommended value could result in over voltage stress.

6.1.1.2.2 AM62P / AM62P-Q1

The processor includes eight Dual-voltage IO domains (VDDSHVx [x = 0..3, 5..6], VDDSHV_CANUART and VDDSHV_MCU), where each domain provides power supply to a fixed set of IOs. Each IO domain can be configured for 3.3 V or 1.8 V independently, which determines a common operating voltage for the entire set of IOs powered by the respective IO domain power supply.

Processor pads (pins) designated as CAP_VDDSx [x=x = 0..3, 5..6], CAP_VDDS_CANUART and CAP_VDDS_MCU are provided for connecting an external capacitor to the internal LDO. A 1-µF (to be connected between these pins and VSS, see the device-specific data sheet,) capacitor is recommended. Refer device-specific data sheet for the recommended capacitor voltage rating.

The capacitors are expected to be placed on the back side of the PCB in the array of the BGA to meet the loop inductance requirements. Choice of capacitor voltage rating could influence the capacitor package (size) selection.

Select a capacitor with ESR < 1 Ω. Ensure board trace connection loop inductance is < 2.5-nH.

The capacitor value recommended does not include variations in value considering DC bias and degradation over time. The capacitor value is independent of IO count and activity. It is required for stability of the LDO to generate BIAS supply. Any value beyond the recommended value could result in over voltage stress.

6.1.1.2.3 Additional Information

Most of the processor IOs are not fail-safe. For information on fail-safe IOs, see the device-specific data sheet. It is recommended to power IO supply of attached devices from the same power source as the respective processor Dual-voltage IO domains (VDDSHVx supply rail) to ensure the system never applies potential to an IO that is not powered. This is needed to protect the IOs of processor and attached devices.

For more information on power-sequencing requirements between processor and attached devices including signal isolation for fail-safe operation, see the below FAQ:

[FAQ] AM625 / AM623 Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices. This is a generic FAQ and can also be used for AM625SIP / AM625-Q1 / AM620-Q1, AM62A7 / AM62A3 and AM62P / AM62P-Q1 family of processors.

Note

A valid supply voltage for the VDDSHVx IO supplies must be present before any input is applied to the associated processor IOs or peripherals.

VDDSHVx IO supplies and the associated CAP_VDDSx capacitors must be connected irrespective of the usage of the processor IOs or peripherals.

6.1.1.3 Supply for VPP (eFuse ROM Programming)

It is important for the processor VPP (eFuse ROM programming supply) to remain within the ROC range during eFuse programming. An LDO powered from a higher input voltage supply (2.5 V or 3.3 V) is recommended for the LDO to be able to compensate for the voltage drop through its series pass transistor and maintain the correct operating voltage during high load current transients. Local bulk capacitors are recommended near the processor VPP pin to support the LDO transient response.

Using a Load switch or FET configured as a switch to power VPP from another supply rail that has a +/-5% variation could be problematic due to the high load current transient and the VPP power rail having the same supply range requirement. This topology doesn't account for the voltage drop going through the load switch. The load switch may be an option if the board designer uses power source with smaller variation, such that the supply variation combined with the voltage drop through the load switch never exceeds the VPP recommended operating range.

For more information, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application. This is a generic FAQ and can also be used for AM62A7 / AM62A3 and AM62P / AM62P-Q1 family of processors.

6.1.1.4 Supply Connection for Partial IO Mode (Low Power) Configuration

6.1.1.4.1 Partial IO Used

VDD_CANUART and VDDSHV_CANUART are recommended to be connected to always on power sources.

6.1.1.4.2 Partial IO Not Used

VDD_CANUART shall be connected to the same power source as VDD_CORE and VDDSHV_CANUART shall be connected to any valid IO power source.

6.1.1.4.3 Data Sheet Reference for Power Sequence

Refer to notes related to partial IO in the below sections of the processor specific data sheet:

Power-Up Sequencing

Power-Up Sequencing – Supply / Signal Assignments

Power-Down Sequencing

Power-Down Sequencing – Supply / Signal Assignments

Also, refer *Partial IO Power Sequencing* section of the processor specific data sheet.

6.1.1.5 Additional Information

Placement of 0 Ω resistors (shunt) or a jumper in line with the core supply and other supply rails are recommended for initial PCB prototype builds. This helps during board bring-up and debug to isolate the supply or for current measurement. Current measurement is the purpose of these resistors in the SK.

Verify the effect of adding these provisions on the custom board performance.

6.1.2 Capacitors for Supply Rails

6.1.2.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

Ensure PDN analysis has been performed, and the required number of decoupling and bulk capacitors are provided for all the power supply rails including the Dual-voltage IO supply rails.

Place the decoupling capacitors as close as possible to the supply pins. Larger bulk capacitors can be placed further away.

Use low ESL capacitors and mount them with shortest possible traces to keep the mounting inductance low. For more information, refer the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

The bulk and decoupling capacitors values from the SK can be used as a reference when PDN analysis is not performed or results are not available. For filtered (ferrite) power supplies implementation, follow the device-specific SK.

6.1.2.2 AM62A7 / AM62A3 and AM62P / AM62P-Q1

Feedthrough (3-terminal) capacitors can be considered (used on the SK-AM62A-LP and SK-AM62P-LP SK) to optimize the number of capacitors used. Use of 3-terminal capacitors minimizes the loop inductance and helps optimize processor performance mainly the DDR performance.

6.1.2.3 Additional Information

6.1.2.3.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 and AM62A7 / AM62A3

When the processor peripherals (Camera Serial interface (CSIRX0), DDR Subsystem (DDRSS0) and USB2.0 (USB0 and USB1)) are not used, the supplies (core, analog) associated with these peripherals have specific connectivity requirements. For more information, refer the *Pin Connectivity Requirements* section of the device-specific data sheet. The power supply filter (ferrite) and the capacitors (bulk) used can be optimized.

6.1.2.3.2 AM62P / AM62P-Q1

When the processor peripherals (CSI-2 (Camera Serial interface 2) and DSI (Display Serial interface) instance CSIRX0 and DSITX0), DDR Subsystem (DDRSS0) and USB2.0 (USB0 and USB1)) are not used, the supplies (core, analog) associated with these peripherals have specific connectivity requirements. For more information, refer the *Pin Connectivity Requirements* section of the device-specific data sheet. The power supply filter (ferrite) and the capacitors (bulk) used can be optimized.

6.1.3 Processor Clock

6.1.3.1 Clock Inputs

6.1.3.1.1 High Frequency Oscillator (MCU_OSC0_XI/ MCU_OSC0_XO)

For the operation of the processor, select a crystal as clock source or 1.8 V LVCMOS square-wave digital clock source.

A 25 MHz external crystal connected to the internal high frequency oscillator (MCU_HFOSC0), is the default clock source for internal reference clock HFOSC0_CLKOUT.

Discrete components used to implement the oscillator circuit are recommended to be placed as close as possible to the MCU_OSC0_XI and MCU_OSC0_XO pins. For the crystal, follow the *MCU_OSC0 Crystal Circuit Requirements* table of the device-specific data sheet when choosing the load capacitors.

When a 1.8 V LVCMOS square-wave digital clock source is used, connect the processor XO pin as per the device-specific data sheet recommendation.

For information on clock selection, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding Crystal selection. This is a generic FAQ and can also be used for AM62A7 / AM62A3 and AM62P / AM62P-Q1 family of processors.

Note

25 MHz is the only crystal frequency that is currently supported. Refer device-specific data sheet for more details on the crystal parameters.

6.1.3.1.2 Low Frequency Oscillator (WKUP_LFOSC0_XI/ WKUP_LFOSC0_XO)

WKUP_LFOSC0 has limited use case and is optional. Based on the use case, select a 32.768 kHz crystal as clock source or 1.8 V LVCMOS square-wave digital clock source.

For more information, see the [FAQ] AM625: LFOSC usage in the device. This is a generic FAQ and can also be used for AM623 / AM625SIP / AM625-Q1 / AM620-Q1, AM62A7 / AM62A3 and AM62P / AM62P-Q1 family of processors.

All discrete components used to implement the oscillator circuit must be placed as close as possible to the WKUP_LFOSC0_XI and WKUP_LFOSC0_XO pins. For the crystal, the load capacitance selected is required to be in the range recommended in the *WKUP_LFOSC0 Crystal Electrical Characteristics* table of the device-specific data sheet.

If WKUP_LFOSC0_XI/ XO is not used:

- It is recommended to connect the XI directly to VSS
- It is recommended to leave XO unconnected

For more information on connecting the unused WKUP_LFOSC0, see the *WKUP_LFOSC0 Not Used* section of the device-specific data sheet.

6.1.3.1.3 EXT_REFCLK1 (External Clock Input to Main Domain)

EXT_REFCLK1 pin is routed to clock muxes as one of the selectable input clock source to the Timer modules (DMTIMER/WDT), DMTIMER in Security Subsystem (SMS), MCAN and CPTS (Time Stamping Module). If an application requires a specific clock frequency to be fed to these modules using the EXT_REFCLK1 is an option (example: time synchronization or for clock quality reasons).

6.1.3.1.4 Additional Information

MCU_OSC0_XI/ MCU_OSC0_XO has specific routing guidelines. Refer *Clock Routing Guidelines* section of device-specific data sheet. The clock routing guidelines are the same for the AM62x processor family.

6.1.3.2 Clock Outputs

Processor pins named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for the attached devices (external peripherals).

WKUP_CLKOUT0 is a buffered output of the high frequency oscillator HFOSC0 available during power-up as default output for AM62x processor family.

WKUP_CLKOUT0 is driven low during power-up for AM62Ax and AM62Px processor family.

6.1.4 Processor Reset

6.1.4.1 External Reset Inputs

MCU_PORz is the external MCU and Main Domain cold reset input to the processor. It is recommended to keep the MCU_PORz pulled low during the supply ramp and oscillator start-up. Follow the recommended MCU_PORz timing in the *Power-Up Sequencing* diagram of the device-specific data sheet.

For MCU_PORz (3.3 V tolerant, fail-safe input), a 3.3 V input can be applied. The input thresholds are a function of the 1.8 V IO supply voltage (VDDS_OSC0).

Usage note for MCU_RESETz:

Refer silicon errata advisory i2407- RESET: MCU_RESETSTATz unreliable when MCU_RESETz is asserted low

Connect external warm reset inputs MCU_RESETz and RESET_REQz as per the *Pin Connectivity Requirements* section of the device-specific data sheet. Warm reset inputs (LVCMOS inputs) have input slew rate requirements. Connecting a capacitor directly at the input is not recommended due to the slow input ramp. A schmitt trigger based debouncing circuit is recommended. For implementing the debouncing logic, see the device-specific SK schematics.

6.1.4.2 External Reset Status Outputs

PORz_OUT is the Main Domain POR (cold reset) status output, RESETSTATz is the Main Domain warm reset status output and MCU_RESETSTATz is the MCU Domain warm reset status output.

RESETSTATz can be used to reset on-board memories or peripherals with reset functionality (eMMC, OSPI, EPHY) or SD Card power switch. The PORz_OUT can also be used to latch the hardware strap configurations during power-up including latching the Ethernet PHY pin strap configurations.

Pulldown resistors are recommended for PORz_OUT and RESETSTATz outputs to assert the reset (hold the attached devices in reset) to the attached devices during power-up.

It is recommended to connect the reset status outputs to a test point for testing or future enhancements when not used. Optionally a pulldown can be provided and can be a DNI.

Note

MCU_RESETz and MCU_RESETSTATz have specific use case recommendation. Refer advisory i2407 of the device-specific silicon errata.

6.1.4.3 Additional Information

The BOOTMODExx inputs that are used to configure the processor boot must be held in a known state to select the appropriate boot mode configuration as defined in the device-specific TRM, until the boot mode configuration is latched during the rising edge of the PORz_OUT.

6.1.5 Configuration of Boot Modes (for Processor)

Boot mode inputs do not have internal pullup or pulldown resistors that are active during processor power-up or reset. It is recommended to connect external pullup or pulldown resistors to set the required boot mode.

When dip switches are used, it is recommended to use a resistor divider ratio of 470 Ω (pullup) and 47 kΩ (pulldown) for improved noise performance.

When the bootmode is configured using only resistors, a standard resistor (same value for pullup or pulldown) value Example: 10 kΩ or similar is recommended since either the pullup or pulldown resistor will be used.

It is recommended to connect pullup or pulldown resistor to boot mode pins marked as Reserved or not used.

BOOTMODE 14 and BOOTMODE 15 pins are Reserved for AM62x family of processors.

BOOTMODE 14 and BOOTMODE 15 pins are Reserved for AM62Ax family of processors.

BOOTMODE 14 pin is Reserved and BOOTMODE 15 pin is POST (Hardware Power-on-Self-test) functionality for AM62Px family of processors. It is recommended to add provision for pullup and pulldown resistors for BOOTMODE 15 pin.

It is highly recommended to add provision for pullup and pulldown resistors for all the boot mode pins that have configuration capability for debugging, design flexibility and future enhancement. Populate either pullup or pulldown for each boot mode pins. Direct connection of boot mode pins to ground or IO supply rail is not recommended or allowed since these IOs have alternate configuration and could intentionally or unintentionally be configured as output by the software.

Boot mode input pins are not fail-safe and this needs to be considered when boot mode configurations are being driven from an external input or a base board.

Based on the application requirement, a buffer that is driven only when reset (MCU_PORz) is asserted (low) can be used to present the boot configuration to the processor.

If the bootmode pins are configured as an output during normal operation, a series resistor (~1 kΩ) is recommended at the output of the buffers. For more information, see the device-specific SK for implementation.

6.1.5.1 Processor Boot Mode Inputs Isolation Buffers Use Case and Optimization

In the SK, the boot mode pins BOOTMODE [15:00] are asserted through two buffers (isolation buffers). The buffers ensure that SYSBOOT pulls (boot mode configured using resistors) are controlling the level of the signals when the boot mode signals are being latched (around the PORz_OUT rising edge) by the processor. Since boot mode signals are often used for other functions after processor power-up and are connected to attached devices or peripherals, boot mode configuration resistors need to be isolated from other connected peripherals so that those peripherals do not conflict with the intended boot mode configuration (signal levels).

The buffers are enabled when PORz_OUT is driven low by the processor. After PORz_OUT goes high, the buffer outputs are Hi-Z so the signals are not pulled or influenced by the boot mode resistors.

For optimizing the design (including BOM), these buffers can be optimized or deleted depending on the use case. The boot mode pull resistors value can be selected so that they do not affect the operation of attach devices.

6.1.5.2 Bootmode Selection

For configuring the processor bootmode, refer the *ROM Code Boot Modes* table in the *Initialization* chapter of the device-specific TRM.

6.1.5.2.1 Notes for USB Boot Mode

USB0 interface supports boot. When the USB0 is configured for DFU boot mode, 3.3 V supply (permanent or switched) is not recommended to be connected to the USB0_VBUS pin. No permanent supply (equivalent to the divider value) is allowed to be connected to the USB0_VBUS pin.

A 5 V supply from the host (switched) connected through the USB connector is recommended to be connected to the processor USB0_VBUS pin through the resistor voltage divider as per the device-specific data sheet recommendations. The Zener diode could be deleted and the two resistors can be combined to a 20 kΩ resistor for the *USB VBUS Detect Voltage Divider / Clamp Circuit* if the custom board design will never apply a VBUS potential greater than 5.5 V and the supply is on-board.

6.1.5.3 Additional Information

When the boot mode configuration are being driven by external inputs, the boot mode configuration inputs are recommended to be stable during the processor POR (cold reset).

When using Ethernet Boot and RGMII, the design must implement a EPHY that enables RGMII_ID mode on the EPHY RX data path and disables RGMII_ID mode on the TX data path by default (the processor implements RGMII_ID on the TX output). The processor ROM is EPHY agnostic and will not programmatically enable/disable RGMII_ID mode on attached EPHYs. Typically, this is accomplished via pin strapping on the EPHY.

Select a EPHY with capability to set the RGMII internal TX delay through pin strap, see the device-specific SK. For more information, see the advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS)* of the device-specific silicon errata.

6.2 Board Debug Using JTAG and EMU

JTAG and EMU used

Recommend to connect the JTAG (TDI, TCK, TMS and TRSTn) and EMU (EMU0 and EMU1) signals as per the *Pin Connectivity Requirements* section of the device-specific data sheet.

It is recommended to connect a series resistor (22 Ω) for the TDO (close to processor) signal. It is recommended to add external ESD protection for all JTAG and EMU signals when the signals interface to external connector. EMU 0/1 signals support boot sequence debug after cold reset (MCU_PORz).

TDO pullup is optional and depends on the target used.

Refer *On-Chip Debug* chapter of the device specific TRM.

JTAG and EMU not used

For connecting the JTAG and EMU signals, refer the *Pin Connectivity Requirements* section of the device-specific data sheet.

During custom board design, TI recommends provisioning at least a minimal JTAG port including EMU0/1 connected to test points or a header footprint to support early prototype debugging. JTAG components can be DNI in the production version of the board, if desired. Also provide provision to add recommended pulls as per *Pin Connectivity Requirements* section and external ESD protection.

6.2.1 Additional Information

Buffering of clock and signals are recommended whenever the JTAG interface connects to more than one device. Buffering of clock is recommended even for single device implementations. For implementation, see the device-specific SK.

If trace operation is used, connect TRC_x signals directly to the emulation connector. All TRC_x signals are pin-muxed with other signals. Either trace functionality or GPMC interface can be used. Connections (Board trace) for TRC_x signals used for trace functionality must be short and skew matched. The trace signals are on VDDSHV3 Dual-voltage IO domain, and can be at a different supply voltage from the other JTAG signals. For additional recommendations on TRC/EMU design and layout, see the *Emulation and Trace Headers Technical Reference Manual*. A summary of this information is available in the *XDS Target Connection Guide*.

If boundary scan is used, connect EMU0 and EMU1 pins directly to the JTAG connector.

For proper implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual* and the *XDS Target Connection Guide*.

7 Processor Peripherals

7.1 Supply Connections for IO Groups

7.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 and AM62A7 / AM62A3

Each Dual-voltage IO domain (VDDSHVx [x=0..6], VDDSHV_MCU and VDDSHV_CANUART) provides power supply to a fixed set of IOs (peripherals). 3.3 V or 1.8 V supply voltage can be connected to each of the Dual-voltage IO domains.

VDDSHV4, VDDSHV5 and VDDSHV6 have been designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

Note the output buffer type available for the processor IOs (SDIO or LVCMOS) connected to the IO supply rails.

7.1.2 AM62P / AM62P-Q1

Each Dual-voltage IO domain (VDDSHVx [x = 0..3, 5..6], VDDSHV_MCU and VDDSHV_CANUART) provides power supply to a fixed set of IOs (peripherals). 3.3 V or 1.8 V supply voltage can be connected to each of the Dual-voltage IO domains.

VDDSHV5 and VDDSHV6 have been designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails. This capability is required to support UHS-I SD Cards.

Note the output buffer type available for the processor IOs (SDIO or LVCMOS) connected to the IO supply rails.

7.2 Memory Interface (DDRSS (DDR4 / LPDDR4), MMCSD (eMMC / SD / SDIO), OSPI / QSPI and GPMC)

7.2.1 DDR Subsystem (DDRSS)

Refer below FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDR4 / LPDDR4 MEMORY Interface.

7.2.1.1 DDR4 SDRAM (Double Data Rate 4 Synchronous Dynamic Random-Access Memory)

7.2.1.1.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

For implementation guidelines and routing topologies, refer the *AM62x DDR Board Design and Layout Guidelines*.

7.2.1.1.1.1 Interface Configuration

The allowed memory configurations are 1 X 16-bit or 2 X 8-bit.

1 X 8-bit memory configuration is not a valid configuration.

Verify connection of DDRSS Bank Groups (DDR0_BG0, DDR0_BG1) based on the selected memory size. Refer *DDR4 Implementation Using 8-Bit SDRAM Devices* section of *AM62x DDR Board Design and Layout Guidelines*.

Verify connection of DDRSS Chip Selects (DDR0_CS0_n, DDR0_CS1_n) based on memory selection (Single-Rank or Dual-Rank).

7.2.1.1.1.2 Routing Topology and Terminations

When a single memory (DDR4) device (1 X 16-bit) is used, Point-to-Point topology could be considered.

Summary of point-to-point topology implementation:

- External terminations (VTT) for address and control signals are not required.
- For differential clock (DDR0_CK0, DDR0_CK0_n), AC (differential) termination (2 X R in series (value = Zo - Single-ended impedance) and a filter capacitor (0.01-µF or value recommended by the memory manufacturer) connected to the center of two resistors and VDDS_DDR (DDR PHY IO supply)) is recommended. For Single-ended impedance value and DDR4 point-to-point connections, see the *AM62x DDR Board Design and Layout Guidelines* and device-specific SK.
- VREFCA (VDDS_DDR/2) is the reference voltage used for control, command and address inputs to the memory (DDR4) devices. VREFCA can be derived from VDDS_DDR using a resistor divider (2 resistors (recommended resistor value is 1 kΩ, 1%) connected to VDDS_DDR and VSS) with filter capacitor (recommended value is 0.1-µF) connected in parallel to both the resistors. An additional decoupling capacitor is connected to the VREFCA pin (close to memory (DDR4) device).

Alternatively, adding VTT terminations for a single memory (DDR4) device on the address and control signals, and using an Sink/Source DDR Termination Regulator to generate the VTT supply is an acceptable approach.

When two memory (DDR4) devices (2 X 8-bit) are used, it is recommended to follow the Fly-by topology.

Summary of Fly-by topology implementation:

- External terminations (VTT) for address, control and clock signals are recommended.
- Sink/Source DDR Termination Regulator is recommended to generate the VTT supply.
- The Sink/Source DDR Termination Regulator generates the reference voltage VREFCA (VDDS_DDR/2).
- Add decoupling capacitors for the reference voltage.

7.2.1.1.1.3 Resistors for Control and Calibration

Connect pulldown resistors for DDR0_RESET0_n (DDR_RESET#), DDR0_CKE0 (DDR_CKE (optional)) and pullup resistor for DDR0_ALERT_n (DDR_ALERTn) close to memory (DDR4) device. Provide pulldown resistor for DDR4 device TEN (test enable) close to memory (DDR4) device. For implementation and resistor value, see the device-specific SK.

Connect recommended resistors for DDR0_CAL0 (close to processor) and ZQn (n=0..1, close to memory (DDR4) device). For recommended connection, resistor value and tolerance, see the device-specific data sheet and *AM62x DDR Board Design and Layout Guidelines*.

7.2.1.1.1.4 Capacitors for the Power Supply Rails

Verify if adequate bulk and decoupling capacitors are provided for the processor DDR supply rails and memory (DDR4) device supply rails.

Follow the device-specific SK implementation whenever recommendations are not available.

7.2.1.1.1.5 Data Bit or Byte Swapping

During custom board design in case bit swapping is required, bit swaps within a data byte, and swapping of byte 0/1 are allowed with some restrictions. The DM and DQS bits must not be swapped with any other signals. Bit swapping of the address or control bits is not allowed.

For more information, refer the *Bit Swapping* section in the *DDR4 Board Design and Layout Guidance* chapter of the *AM62x DDR Board Design and Layout Guidelines*.

It is recommended to update the schematics with the bit swapping changes for future reference or reuse.

7.2.1.1.1.6 VTT Termination Schematics Reference

When two memory (DDR4) devices (2 X 8-bit) are used, each device would be connected to each data byte. The address/control signals would be connected in Fly-by topology with VTT termination.

Refer *AM64x evaluation module for Sitara processors* for implementing VTT termination.

It is recommended to perform board level simulations to ensure proper signal integrity.

7.2.1.1.2 AM625SIP

Not Applicable. The DDRSS0 pins have been reassigned due to integrated LPDDR4 and have connection recommendations recommended in the *Pin Attributes and Signal Descriptions* section of the device-specific data sheet (AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM).

7.2.1.1.3 AM62A7 / AM62A3

Currently Not Supported.

7.2.1.1.4 AM62P / AM62P-Q1

Currently Not Supported.

7.2.1.2 LPDDR4 SDRAM (Low-Power Double Data Rate 4 Synchronous Dynamic Random-Access Memory)

7.2.1.2.1 AM625 / AM623 / AM625-Q1 / AM620-Q1

For implementation guidelines and routing topology, refer the *AM62x DDR Board Design and Layout Guidelines*.

7.2.1.2.1.1 Interface Configuration

The allowed memory configuration is 1 X 16-bit.

7.2.1.2.1.2 Routing Topology and Terminations

Follow point-to-point topology for clock (CK), address, control (ADDR_CTRL) and data signals.

VTT termination does not apply for LPDDR4. Terminations required for address/control signals are handled internally (on-die).

7.2.1.2.1.3 Resistors for Control and Calibration

Connect a pulldown resistor for DDR0_RESET0_n (LPDDR4_RESET_N) close to memory (LPDDR4) device. For implementation and resistor value, see the device-specific SK.

Connect recommended resistors for DDR0_CAL0 (close to processor), ODT_CA_A (close to memory (LPDDR4) device) and ZQ (close to memory (LPDDR4) device). For recommended connection, resistor value and tolerance, see the device-specific data sheet, SK schematic and *AM62x DDR Board Design and Layout Guidelines*.

7.2.1.2.1.4 Capacitors for the Power Supply Rails

Verify if adequate bulk and decoupling capacitors are provided for the processor DDR supply rails and memory (LPDDR4) device supply rails.

Follow the device-specific SK implementation whenever recommendations are not available.

7.2.1.2.1.5 Data Bit or Byte Swapping

During custom board design in case bit swapping is required, bit swaps within a data byte, and swapping of byte 0/1 are allowed. Address bit swapping is not allowed.

It is recommended to update the schematics with the bit swapping changes for future reference or reuse.

7.2.1.2.2 AM625SIP

LPDDR4 memory is integrated (internal) within the AM625SIP processor. The DDSSS0 pins have been reassigned to provided the required power supplies and external calibration resistor (DDR_ZQ).

For connecting the power supplies and the calibration resistor including the value, tolerance and resistor supply connection, see the device-specific data sheet (AM625SIP – AM6254 Sitara Processor with Integrated LPDDR4 SDRAM).

7.2.1.2.3 AM62A7 / AM62A3 and AM62P / AM62P-Q1

For implementation guidelines and routing topology, refer the *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines*.

7.2.1.2.3.1 Interface Configuration

The allowed memory configurations are 1 X 32-bit or 1 X 16-bit.

1 X 8-bit memory configuration is not a valid configuration.

7.2.1.2.3.2 Routing Topology and Terminations

When a 32-bit, Single-Rank/Dual-Rank LPDDR4 is used, follow Balanced ‘T’ Topology for Address, CKE and CK signals routing.

When a 16-bit, Single-Rank LPDDR4 is used, follow the point-to-point topology. Connect the unused Data strobe pins (DDR0_DQS2..3 and DQS2..3_n) as per the *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines* recommendation.

The data signal connection topology is point-to-point for LPDDR4, and is categorized into different byte lanes.

VTT termination does not apply for LPDDR4. Terminations required for address/control signals are handled internally (on-die).

7.2.1.2.3.3 Resistors for Control and Calibration

Connect a pulldown resistor for DDR0_RESET0_n (LPDDR4_RESET_N) close to memory (LPDDR4) device. For recommended connection and resistor value, see the device-specific SK schematics and *AM62Ax / AM62Px DDR Board Design and Layout Guidelines*.

Connect recommended resistors for DDR0_CAL0 (close to processor), ODT_CA_A..B (close to memory (LPDDR4) device) and ZQn (n=0..1, close to memory (LPDDR4) device). For recommended connection, resistor value and tolerance, see the device-specific data sheet, SK schematics and *AM62Ax / AM62Px DDR Board Design and Layout Guidelines*.

7.2.1.2.3.4 Capacitors for the Power Supply Rails

Verify if adequate bulk and decoupling capacitors are provided for the processor DDR supply rails and memory (LPDDR4) device supply rails.

Follow the device-specific SK implementation whenever recommendations are not available.

7.2.1.2.3.5 Data Bit or Byte Swapping

During custom board design in case bit swapping is required, bit swaps within a data byte, and swapping across bytes is allowed with some restrictions. Address and control bit swapping is not supported.

For more information, refer the *Channel, Byte, and Bit Swapping* section of *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines*.

It is recommended to update the schematics with the bit swapping changes for future reference or reuse.

7.2.2 Multi-Media Card/Secure Digital (MMCSD)

The processor supports three MMCSD instances. The MMCSD Host Controller provides an interface to 1 X eMMC (8-bit) and 2 X SD/SDIO (4-bit) instances.

7.2.2.1 MMC0 - eMMC (Embedded Multi-Media Card) Interface

Refer below FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface

7.2.2.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 and AM62A7 / AM62A3

For more information, refer the *MMC0 - eMMC/SD/SDIO Interface* section of the device-specific data sheet.

7.2.2.1.1.1 IO Power Supply

The processor IOs used for MMC0 interface are powered by VDDSHV4 (Dual-voltage IO) supply rail (IO supply for IO group 4).

VDDSHV4 is designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails.

It is recommended to connect VDDSHV4 and IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.2.2.1.1.2 eMMC (Attached Device) Reset

It is recommended to implement the device reset using a dual input AND gate logic. One of the AND gate input is connected to the processor general purpose input/output (GPIO) pin. The AND gate input has provision for pullup and 0 Ω to isolate the GPIO for testing or debug. The other AND gate input is the Main Domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.

7.2.2.1.1.3 Signals Termination

Provide the following:

- Connect a series resistor (0 Ω) for MMC0_CLK signal (close to processor) and external pulldown resistor for MMC0_CLK signal (close to eMMC device).
- Connect external pullup resistor for the data line (MMC0_DAT0) (close to eMMC device). eMMC device (as long as the eMMC device is compliant to the eMMC standard) has the pullups enabled for data signals MMC0_DAT1..7 by default. The eMMC device will turn off its MMC0_DAT1..3 pulls when entering 4-bit mode and MMC0_DAT1..7 pulls when entering 8-bit mode. The eMMC host software should turn on the respective DAT pulls when it changes the mode.
- Connect pullup resistor for MMC0_CMD signal and pulldown with TP (optional) for DS signal (close to eMMC device).

7.2.2.1.1.4 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV4 (Dual-voltage IO) supply rail and the attached device (Core and IO supplies).

Follow the device-specific SK implementation whenever recommendations are not available.

7.2.2.1.2 AM62P / AM62P-Q1

For more information, refer the *MMC0 - eMMC Interface* section of the device-specific data sheet.

7.2.2.1.2.1 MMC0 Used

7.2.2.1.2.1.1 IO Power Supply

The MMC0 interface of the processor is powered by the VDD_MMC0 (0.85 V), VDD_0P85_DLL_MMC0 (0.85 V) and VDDS_MMC0 (1.8 V) supplies.

It is recommended to connect VDDS_MMC0 and IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.2.2.1.2.1.2 eMMC (Attached Device) Reset

It is recommended to implement the device reset using a dual input AND gate logic. One of the AND gate input is connected to the processor general purpose input/output (GPIO) pin. The AND gate input has provision for pullup and 0 Ω to isolate the GPIO for testing or debug. The other AND gate input is the Main Domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.

7.2.2.1.2.1.3 Signals Termination

Provide the following:

- Connect a series resistor (0 Ω) for MMC0_CLK signal (close to processor)
- Connect a resistor between MMC0_CALPAD (close to processor) and VSS. Refer device-specific data sheet for recommended resistor value and tolerance.

Note

No external pull resistors are required for MMC0 since the PHY includes and dynamically controls the internal pull resistors as required for an eMMC.

Pullups for DAT0..7 and CMD are internally enabled during reset and after reset by the processor eMMC PHY. Pulldown is enabled for the DS and the clock output (CLK) is driven low during reset and by the SS (The subsystem selected with MUXMODE determines the output buffer state) after reset.

There are no PADCONFIG registers associated with the MMC0 pins. The internal pulls associated with the MMC0 pins are dynamically controlled by the MMC0 host and PHY.

Provision for External pulls are not a requirement for the eMMC data, CMD, DS and the CLK signals.

7.2.2.1.2.1.4 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for MMC0 supply rails and the attached device (Core and IO supplies).

Follow the device-specific SK implementation whenever recommendations are not available.

7.2.2.1.2.2 MMC0 Not Used

MMC0 interface signals do not have alternate function. When MMC0 is not used, the interface signals and the MMC0 supplies have specific connectivity requirements.

For connecting the interface signals and MMC0 supply rails, refer the *Pin Connectivity Requirements* section of the device-specific data sheet.

7.2.2.1.3 Additional Information on eMMC PHY

See the notes in the *Signal Descriptions, MMC, MAIN Domain* section of the device-specific data sheet.

Note

There could be implementation difference in the eMMC Controller and PHY IPs used on different processors families. Pay attention on the interface including terminations recommended when migrating to a different processor family.

It is recommended to review the device-specific data sheet, TRM, and following the connection recommendations for the device-specific processor family and attached device.

Device-specific SK implementation can be followed as required.

7.2.2.2 MMC0 – SD (Secure Digital) Card Interface

The CD (Card Detect) and WP (Write Protect) pins are not available on MMC0 interface. This can be used to interfaces with fixed SDIO devices (on-board). Fore more information, refer the *MMC0 - eMMC/SD/SDIO Interface* section of the device-specific data sheet (AM62x and AM62Ax).

7.2.2.3 MMC1 / MMC2 – SD (Secure Digital) Card Interface

For more information, refer the *MMC1/MMC2 - SD/SDIO Interface* section of the device-specific data sheet.

7.2.2.3.1 IO Power Supply

The processor MMC1 (CMD, CLK and Data) interface IOs are powered by VDDSHV5 (Dual-voltage IO) supply rail (IO supply for IO group 5) and MMC2 (CMD, CLK, Data, CD and WP) interface IOs are powered by VDDSHV6 (Dual-voltage IO) supply rail (IO supply for IO group 6).

VDDSHV5 and VDDSHV6 have been designed to support power-up, power-down, or dynamic voltage change without any dependency on other power rails.

VDDSHV5 and VDDSHV6 supplies must always default to 3.3 V and allow changing to 1.8 V when software is ready to change the supply voltage.

It is recommended to use separate supply sources (LDO or similar) for VDDSHV5 and VDDSHV6 supply rails when configured as SD Card interface.

Processor MMC1 SD Card Detect (CD) and Write Protect (WP) signals are powered by VDDSHV0 (Dual-voltage IO) supply rail (IO supply for IO group 0). It is recommended to connect the pullups for MMC1_SDCD, MMC1_SDWP from SD Card to the same supply rail VDDSHV0.

7.2.2.3.2 SD Card Supply Reset and Boot Configuration

It is recommended to provision for a software enabled (controlled) power switch (load switch) that sources the SD Card power supply (VDD). A fixed 3.3 V supply (IO supply connected to the processor) is connected as an input to the power switch.

Use of power switch allows power cycling of the SD Card (since this is the only way to reset the SD Card) and resetting the SD Card back into its default state.

It is recommended to implement the SD Card power switch enable reset logic using a three input AND gate. One of the AND gate input is connected to the processor general purpose input/output (GPIO) pin. The AND gate input has provision for pullup and 0 Ω to isolate the GPIO for testing or debug. The other two AND gate inputs are connected to the Main Domain POR (cold reset) status output (PORz_OUT) and Main Domain warm reset status output (RESETSTATz) Signals.

If SD Card is configured as a boot device ensure that the external power switch sourcing the SD Card power supply defaults to ON (powered state).

For the implementation details, see the device-specific SK.

7.2.2.3.3 Signals Termination

Provide the following:

- Connect a series resistor (0 Ω) for MMC1_CLK and MMC2_CLK (close to processor) and external pulldown resistor for MMC1_CLK and MMC2_CLK (close to device or SD Card socket).
- Add external pullup resistors for the data lines (MMC1_DAT0..3 and MMC2_DAT0..3) and CMD signal (MMC1_CMD and MMC2_CMD) connected to the respective Dual-voltage IO (MMC1 = VDDSHV5, MMC2 = VDDSHV6) supply rails (close to device or SD Card socket).
- Add external pullup resistors for the MMC1_SDCD and MMC1_SDWP signals connected to the VDDSHV0 (Dual-voltage IO) supply rail (close to device or SD Card socket).
- Add external pullup resistors for the MMC2_SDCD and MMC2_SDWP signals connected to the VDDSHV6 (Dual-voltage IO) supply rail (close to device or SD Card socket).

7.2.2.3.4 ESD Protection

External ESD protection is recommended for data, clock, and control signals (Internal ESD protection was not designed to handle the board or system level ESD requirements).

7.2.2.3.5 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV5 and VDDSHV6 (Dual-voltage IO) supply rails and attached device.

Follow the device-specific SK implementation whenever recommendations are not available.

Note

Follow the device-specific connection recommendations for data and control signals. It is recommended to place the series resistor for the clock output close to processor pin.

7.2.2.4 Additional Information

See the notes in the *Signal Descriptions, MMC, MAIN Domain* section of the device-specific data sheet.

7.2.3 Octal Serial Peripheral Interface (OSPI) and Quad Serial Peripheral Interface (QSPI)

For more information, refer the *OSPI/QSPI/SPI Board Design and Layout Guidelines* section of the device-specific data sheet.

Refer below FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface

7.2.3.1 IO Power Supply

The processor IOs used for OSPI / QSPI interface are powered by VDDSHV1 (Dual-voltage IO) supply rail (IO supply for IO group 1).

It is recommended to connect VDDSHV1 and IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.2.3.2 OSPI / QSPI Reset

It is recommended to implement the device reset using a dual input AND gate logic. One of the AND gate input is connected to the processor general purpose input/output (GPIO) pin. The AND gate input has provision for pullup and 0 Ω to isolate the GPIO for testing or debug. The other AND gate input is the Main Domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.

7.2.3.3 Signals Termination

Provide the following:

- Provision for a series resistor (0 Ω) for OSPI0_CLK and OSPI0_LBCLKO (close to processor) and external pulldown resistor for OSPI0_CLK (close to attached device).
- Provision for external pullup resistors for CS pin and INT# pin (close to attached device).
- Provision for external pullup resistors for the data lines (DAT0:7) (close to processor). Depending on the availability of pulls internal to the attach device, populate the external pulls.

7.2.3.4 Loopback Clock

Verify the required loopback clock configuration. Different configuration of clock loopback can be made using OSPI0_LBCLKO (OSPI Loopback Clock Output) and OSPI0_DQS (OSPI Data Strobe or Loopback Clock Input). For the following loopback configurations, refer the device-specific data sheet:

- *No Loopback, Internal PHY Loopback, and Internal Pad Loopback*

External Board Level Loopback

Processor DQS or Loopback Clock is used along with the DS data strobe of attached memory device

If DS (Read Data Strobe) pin is available on the device, connect the DS pin of the device to the OSPI0_DQS pin of the processor. It is recommended to leave the OSPI0_LBCLKO pin unconnected.

If DS pin is not being currently used, to configure the external loopback connect the OSPI0_LBCLKO output pin of the processor to the OSPI0_DQS input pin of the processor.

If External Loopback is not used, it is recommended to leave the OSPI0_LBCLKO and OSPI0_DQS pins unconnected.

Note

D0 and D1 of the processor OSPI interface pins must be connected to D0 and D1 of the QSPI / OSPI memory device pins to support legacy x1 commands.

Data bit swapping is not allowed.

7.2.3.5 Interface to Multiple Devices

Connecting OSPI interface to multiple memory devices is currently not supported. It is recommended to connect the OSPI (processor) to a single memory device. In case the OSPI is interfaced to multiple memory devices, the interface would create a split data bus which could severely degrade signal integrity at high speeds. For accessing OSPI at high speeds, a point-to-point data bus is recommended.

7.2.3.6 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV1 (Dual-voltage IO) supply rail and the attached device (Core and IO supplies).

Follow the device-specific SK implementation whenever recommendations are not available.

7.2.4 General-Purpose Memory Controller (GPMC)

7.2.4.1 IO Power Supply

The processor IOs used for GPMC interface are powered by VDDSHV3 (Dual-voltage IO) supply rail (IO supply for IO group 1).

It is recommended to connect VDDSHV3 and IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.2.4.2 GPMC Interface

Verify the number of devices connected to the GPMC interface.

It is recommended to connect the GPMC interface to a single device in synchronous mode. Using multiple devices (i.e., using multiple CSn) would require splitting the GPMC clock (and other interface signals) on board, which could cause signal integrity issues.

A detailed timing analysis is recommended when interfacing multiple devices (not recommended) in asynchronous mode. When interfacing multiple devices in asynchronous mode, the control signals would have to be routed to multiple devices. The split routing and loading (trace length and number of devices) issues will have an affect on custom board performance.

7.2.4.3 Memory (Attached Device) Reset

When using NAND / NOR flash with GPMC, many of the memories interfaced over GPMC may not have the reset pin.

In case reset pin is available, review the reset requirements and connect the reset pin to the relevant reset source.

7.2.4.4 Signals Termination

Provide series resistor (0 Ω) for GPMC0_CLK (close to processor).

It is recommended to provision for external pullup resistors on GPMC0_CSn0..3 (depending on the configuration) to hold the signal high when processor is held in reset, or after reset, before software has configured the PADCONFIG registers to enable the Tx buffer.

7.2.4.4.1 GPMC NAND

The active high ready / active low busy (R/B#) output from the NAND flash is open-drain and is connected to the GPMC0_WAIT0 and GPMC0_WAIT1 signals (depending on the configuration). It is recommended to provide pullup resistor (recommended value is 4.7 kΩ) (close to device).

7.2.4.5 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV3 (Dual-voltage IO) supply rail and the attached device (Core and IO voltage).

Follow the device-specific SK implementation whenever recommendations are not available.

7.3 External Communication Interface (Ethernet (CPSW3G), USB2.0, PRUSS, UART and CAN)

7.3.1 Ethernet Interface Using CPSW3G (Common Platform Ethernet Switch 3-Port Gigabit)

CPSW3G supports the below interfaces:

RGMII (10/100/1000)

RMII (10/100)

7.3.1.1 IO Power Supply

The processor Gigabit Ethernet Media Access Controller (GEMAC) IOs (used for Ethernet interface) are powered by VDDSHV2 (Dual-voltage IO) supply rail (IO supply for IO group 2).

It is recommended to connect VDDSHV2 and IO supply rail of the attached device to the same supply source.

VDD (core voltage) of the attached device can be powered from an independent supply source.

7.3.1.2 Ethernet PHY Reset

It is recommended to implement the device reset using a three input AND gate logic. One of the AND gate input is connected to the processor general purpose input/output (GPIO) pin. The AND gate input has provision for pullup and 0 Ω to isolate the GPIO for testing or debug. The other AND gate input can be the Main Domain POR (cold reset) status output (PORz_OUT) and Main Domain warm reset status output (RESETSTATz) Signals.

If a dual input AND gate is used, PORz_OUT or RESETSTATz can be connected as one of the inputs along with the processor GPIO input as the second input based on the use case. When more than one EPHY is used, it is recommended to provide provision to reset the EPHYs individually.

A pullup or pulldown at the output of the ANDing logic is recommended based on the EPHY reset pin configuration. The board designer needs to make sure the EPHYs are held in reset for a specified minimum reset hold time after the respective clocks are valid.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.

7.3.1.3 Ethernet PHY Pin Strapping

Many of the TI EPHYs configure their outputs as inputs during reset and captures the configuration (Pin strapping is done through resistors) information on these inputs when the processor is released from reset. It may be necessary to apply appropriate pullup or pulldown resistors on these inputs (IOs) which also connect to processor IOs. TI EPHYs used on the device-specific SK use a combination of pullup and pulldown resistors allowing multiple configuration modes to be configured using each pin. By default, the processor input buffers and internal pullup or pulldown resistors are disabled, which minimizes any concern of a mid-supply potential being applied to the processor input buffer by the EPHY. The EPHYs are required to be configured to normal state from reset state to ensure the EPHY is driving a valid logic state before enabling any of the associated processor input buffers.

7.3.1.4 Ethernet PHY (and MAC) Operation and Media Independent Interface (MII) Clock

Verify the clock input option used for Ethernet PHY and MAC based on the interface.

7.3.1.4.1 Crystal

If a crystal is used as the clock source for the EPHY, it is recommended to match crystal (clock) specifications with the processor crystal (clock) specifications to optimize performance.

7.3.1.4.2 Oscillator

When an external clock (LVCMOS) oscillator is used as the clock source for the processor and the EPHY, a single oscillator is recommended for the processor and the EPHY. It is recommended to use two-output phase aligned buffer for the processor and the EPHY. Be sure to connect XO of the processor as per the device-specific data sheet recommendations. Refer device-specific SK for implementation.

Additionally, verify if the crystal XO of the EPHY has connection recommendations to be followed.

7.3.1.4.3 Processor Clock Output (CLKOUT0)

For optimizing the design, the processor clock output (CLKOUT0) can be used as clock input to the EPHY. Clock output is buffered internally and is intended to used for a point-to-point clock topology. A series resistor is recommended at the source side of the CLKOUT0 to minimize reflections.

RGMII EPHYs require a 25 MHz clock input that is not synchronous to any other signals. So, this signal will not have any timing requirements, but it is important the EPHY does not receive any non-monotonic transitions on its clock input.

RMII EPHY clocking option changes with the EPHY controller (master) or device (slave) configuration.

When configured as controller, RMII EPHYs (most) require a 25 MHz input clock that is not synchronous to any other signals. The 25 MHz clock signal does not have any timing requirements relative the processor, but it is important to make sure the EPHY does not receive any non-monotonic transitions on its clock input.

The RMII EPHY provides the 50 MHz clock output to the MAC. For this use case, the 50 MHz data transfer clock is delayed to the MAC relative to the EPHY. This shifts clock to data timing relationship which may erode the timing margin. This could be problematic for some designs if this delay is too large.

When configured as device, the MAC and the EPHY uses a 50 MHz common clock that is synchronous to both transmit and receive data. The 50 MHz clock is defined in the RMII specification as a common data transfer clock signal that is used by both the MAC and the EPHY, where transitions are expected to arrive simultaneously at the MAC and EPHY device pins. This provides better timing margin for both transmit and receive data transfers. It is also important that the MAC and EPHY do not receive any non-monotonic transitions on their clock inputs. To ensure the clock signal integrity, it is highly recommended this clock signal is routed through a two-output phase aligned buffer. Recommend using equal length signal traces that are ½ the length of the data signals for connecting the clock buffer outputs, where one clock output connects to the MAC and the other connects to the EPHY.

For RMII interface, the recommended configuration is *RMII Interface Typical Application (External Clock Source)* explained in the device-specific TRM. If *RMII Interface Typical Application (Internal Clock Source)* configuration explained in the device-specific TRM is used, the performance has to be validated on a board or system level. Provision for an external clock for initial performance testing and comparison is recommended. The Ethernet performance (RGMII) has been validated on the processor and the EPHY with 25 MHz clock.

The CLKOUT0 signal function can be used to source a 25 MHz or a 50 MHz clock input to the EPHY. However, this would require the software to configure the clock output. This configuration cannot be used if the board design needs to support Ethernet boot. This clock is likely to glitch anytime the configuration is changed.

Based on the selected processor, the processor automatically begins sourcing the device reference clock (MCU_OSC0, enabled by default) to the WKUP_CLKOUT0 pin as soon as the device is released from reset (MCU_PORz 0 -> 1). The processor clock output does not glitch after it begins to toggle. However, the first high or low pulse could be short since reset is released asynchronous to the HFOSC0 clock.

The board designer needs to make sure the EPHYs are held in reset for a specified minimum reset hold time after the respective clocks are valid.

TI does not define performance of the processor clock outputs because clock performance is influenced by many variables unique to each custom board design. The board designer will have to validate timing of all peripherals by using their actual PCB delays, min/max output delay characteristics, and minimum setup/hold requirements of each device to confirm there is enough timing margin.

7.3.1.5 MAC (Data, Control and Clock) Interface Signals Termination

Series resistors (22 Ω) are recommended for the Ethernet MAC interface signals. Use smallest possible package (0402 or smaller) and place as close to source. To start with place series resistor (22 Ω) for the TX signals near to the processor pins. For the RX signals the EPHYs internal series resistors can be used. Providing provision for external series resistors (0 Ω) are recommended on the RX signals.

The interrupt output of the EPHY can be connected to the processor EXTINTn (interrupt) pin. It is recommended to connect a pullup resistor for the EXTINTn close to processor. When a PCB trace is connected and not being driven actively by an external input, it is recommended to connect the external pullup resistor. EXTINTn is an open-drain output type buffer, fail-safe IO.

7.3.1.6 MAC (Media Access Controller) to MAC Interface

For applications requiring EPHY-less (MAC-to-MAC) connection, using the RGMII interface is recommended (check with TI if this is officially supported) since the clocks are source synchronous.

7.3.1.7 MDIO (Management Data Input/Output) Interface

The processor IOs used for MDIO interface are powered by VDDSHV2 (Dual-voltage IO) supply rail (IO supply for IO group 2).

It is recommended to connect an external pullup resistor (close to device) for the MDIO0_MDIO signal.

Before configuring the MDIO interface, refer the advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS)* of the device-specific silicon errata.

7.3.1.8 Ethernet MDI (Medium Dependent Interface) Including Magnetics

In case the EPHY and MDI interface including the magnetics and the RJ45 connector are implemented on the processor board, follow the device-specific SK for MDI interface, magnetics recommendation, external ESD protection and connection of RJ45 connector shield.

7.3.1.9 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV2 (Dual-voltage IO) supply rail and the attached device (core and IO supplies).

Follow the device-specific SK implementation whenever recommendations are not available.

7.3.2 Universal Serial Bus (USB2.0)

The processor provides 2 X USB2.0 interfaces that can be configured as host or device or DRD (Dual-Role Device).

USBn_VBUS (n=0..1) is recommended to be connected in accordance with the *USB Design Guidelines* section of the device-specific data sheet. The supply voltage range for the USBn_VBUS pins is defined in the *Recommended Operating Conditions* section of the device-specific data sheet. The nominal voltage value applied is equal to the resistor divider output when VBUS supply voltage level is 5 V.

USBn_ID functionality is supported via any of the processor GPIO.

Note

USBn_VBUS are fail-safe inputs. The fail-safe input is valid only if the VBUS supply is connected through recommended *USB VBUS Detect Voltage Divider / Clamp Circuit*.

7.3.2.1 USBn (0..1) Used

It is recommended to connect the USB supplies VDDA_CORE_USB (USB0 and USB1 core supply), VDDA_1P8_USB (USB0 and USB1 1.8 V analog supply), and VDDA_3P3_USB (USB0 and USB1 3.3 V analog supply) to the recommended power supply rails in the device-specific data sheet.

Connect USBn_DM (n=0..1) and USBn_DP (n=0..1) signals directly (without any series resistors or capacitors). Route these signals with traces that does not include any stubs or test points.

Connect a resistor between USBn_RCALIB (n=0..1) (close to processor) and VSS. Refer device-specific data sheet for recommended resistor value and tolerance.

7.3.2.1.1 USB Host Interface

It is recommended to provide a power switch to control the VBUS supply to externally connected device and protect power switch input supply from being overloaded.

The power switch output connects to the USB type A connector. It is recommended to connect a capacitor (>120-µF) to the VBUS supply close to the connector.

The USBn_DRVVBUS (n=0..1) signals with an internal pulldown is used to enable the VBUS power switch. An external pulldown near to the power switch enable (EN) pin is recommended. Connection of USBn_VBUS (VBUS supply input including Voltage Divider / Clamp) is optional.

If the power switch used has an OC (over current) indication output, pullup the OC indication output and connect to a processor IO (input).

7.3.2.1.2 USB Device Interface

The VBUS power is sourced by an external host. USB standard for device operation recommends connecting < 10 µF capacitor to the VBUS close to the USB type B connector.

Follow the *USB VBUS Design Guidelines* section of the device-specific data sheet to scale the USB VBUS voltage (supply near the USB interface connector) before connecting to USBn_VBUS pins.

Based on the use case, the zener diode can be deleted if one is absolutely sure that the board will never experience a VBUS signal potential greater than 5.5 V (sourced on-board).

7.3.2.1.3 USB Dual-Role-Device Interface

If the custom board design uses USB Micro-AB connector, the USBn_ID signal from the connector can be routed to a processor GPIO pin. This can be connected to any available GPIO pin. The GPIO pin is specified in the board device tree file, including the pinmux setting of the GPIO pin.

Note

Full compliant USB On-The-Go (OTG) feature is not supported. The ID pin is not bonded out.

7.3.2.1.4 USB Type-C

If the custom board design uses USB Type-C connector, the USBn_ID signals are not required to be connected. The DRD mode switching is controlled by the USB Type-C companion device.

DRP (Dual Role Port) requires a controller, primarily to switch power based on the negotiated role. In a Device Mode only, USB2.0 only, Type-C implementations where the device is not powered by the Type-C connector, no Type-C controller is required.

- The CC pins at the connector should be independently grounded via 5.1 kΩ resistors.
- The USB DP and USB DM connector pins should be shorted on the PCB (DM=B7:A7, DP=B6:A6). This allows for USB2.0 connectivity regardless of cable orientation. Try to keep resulting stubs as short as possible.

Also ensure you follow the USBn_VBUS input scaling recommendations. Refer the section *USB VBUS Design Guidelines* of the device-specific data sheet for more details.

The AM62 SK USB0 interface design can be used as a reference for implementation of USB Type-C interface.

7.3.2.2 USBn (0..1) Not Used

When USB0 and USB1 are not used or USB0 or USB1 is not used, the interface signals and the USB supplies have specific connectivity requirements.

For connecting the interface signals and USB supply pins, refer the *Pin Connectivity Requirements* section of the device-specific data sheet.

It is recommended to connect the USB supplies (VDDA_CORE_USB, VDDA_1P8_USB, and VDDA_3P3_USB) to VSS through separate 0 Ω resistors.

In case USB0 or USB1 are used for future expansion, connect the signals (USBn_DM, USBn_DP, USBn_RCALIB and USBn_VBUS) with the shortest possible traces and connect at test points or connectors. Additionally, it is recommended to provide provision to connect the required USB supplies.

7.3.2.3 Additional Information

Connect USBn_DM and USBn_DP signals directly from the processor to the USB hub upstream port. The hub then distributes these signals to the downstream ports as needed. As each hub has different implementation requirements, it is recommended to follow the hub manufacturer recommendations.

For more information on USB2.0 interface, see the [FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – USB2.0 interface. This is a generic FAQ and can also be used for AM62A7 / AM62A3 and AM62P / AM62P-Q1 family of processors.

7.3.3 Programmable Real-Time Unit Subsystem (PRUSS)

7.3.3.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

For availability of the PRUSS features and supported functionalities, refer the *Device Comparison* section of the device-specific data sheet.

The programmable nature of the PRU cores, along with their access to pins, events and all processor resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the device.

The PRUSS has a large number of IO signals available. Most of these IOs are multiplexed with other functional signals at the processor level. PRUSS pins allow muxing using the PADCONFIGx registers.

Review the interface connection supports the required functionalities during schematic design.

To understand the PRUSS supported functionalities, refer the device-specific data sheet and TRM.

7.3.3.2 AM62A7 / AM62A3 and AM62P / AM62P-Q1

Not Supported

7.3.4 Universal Asynchronous Receiver/Transmitter (UART)

Verify the UART interface application requirements (external interface or debug) and configuration (2-wire or 4-wire with flow control). For the number of UART instances supported, see the device-specific data sheet.

When an external transceiver is used, make sure the external interface signal levels matches the Dual-voltage IO supply voltage level.

Recommend provisioning for series resistors on the interface signals (close to source) for isolation or debug. It is recommended to add pullup resistor on the UART Receive pins (UART0..6_RXD, MCU_UART0..1_RXD).

External ESD protection is recommended in case the interface signals from the processor are directly connected to an external connector.

UART interface is frequently hooked up incorrectly. Make sure signals are connected as follows:

- TX ---> RX
- RX ---> TX

If additional interface signals are used, verify the connections.

7.3.5 Controller Area Network (CAN)

For the number of CAN instances supported, see the device-specific data sheet. The CAN interface to the processor includes external CAN transceiver.

When an external transceiver is used, make sure the external interface signal levels matches the Dual-voltage IO supply voltage level.

Ensure the required terminations at the CAN transceiver are provided.

Recommend provisioning for series resistors on the interface signals (close to source) for isolation or debug.

7.4 On-Board Synchronous Communication Interface (MCSPI, MCASP and I2C)

7.4.1 Multichannel Serial Peripheral Interface (MCSPI) and Multichannel Audio Serial Ports (MCASP)

Provide series resistors (22 Ω) for clock outputs SPI0..2_CLK (MCSPI 0..2) and MCU_SPI0..1_CLK (MCU_MCSPI 0..1) (close to processor).

Provide series resistors (22 Ω) for transmit clock outputs MCASP0..2_ACLKX and Transmit Frame Sync signals MCASP0..2_AFSX (close to processor).

Provide series resistors (22 Ω) for receiver clock outputs MCASP0..2_ACLKR and Receive Frame Sync signals MCASP0..2_AFSR (close to attached device).

Processor IO buffers are disabled during power-up. Verify if external parallel pulls are provided for Chip Select signals SPI0..2_CS0..3 (MCSPI 0..2) & MCU_SPI0..1_CS0..3 (MCU MCSPI 0..1) (close to attached device). Pulls for device clock and data inputs are use case dependent and needs to be verified when selecting the attached device.

7.4.2 Inter-Integrated Circuit (I2C)

Verify if the application requires a fully compliant I2C interface. The MCU_I2C0 and WKUP_I2C0 are fail-safe, true open-drain output type buffer and fully compliant to the I2C specifications. These can support 3.4-Mbps I2C operations (when the IO buffers (interface) are operating at 1.8 V).

Note

For I2C interfaces with open-drain output type buffer (MCU_I2C0 and WKUP_I2C0), an external pullup is recommended irrespective of peripheral usage and IO configuration.

Refer the *Pin Connectivity Requirements* section of the device-specific data sheet. A pullup of 4.7 kΩ or similar is recommended.

When these open-drain output type buffer I2C interfaces are pulled to 3.3 V supply, the inputs have slew rate limit specified. An RC could be used to limit the slew rate. Refer *Starter Kit SK-AM62P-LP* for implementation.

For more information, refer the *Connecting Supply Rails to Pullups* section of this checklist document.

In case additional I2C interfaces are required, I2C0..3 interfaces could be used.

I2C0..3 interface uses LVCMOS to emulate an open-drain output type buffer and are not fully compliant with the I2C specification, in particular falling edges are fast (< 2 ns). Any devices connected to these ports must be able to function properly with the faster fall time. These support 100-kHz and 400-kHz operation. Pullup resistors are recommended for these I2C signals. Location of the pullups is not critical but connection is important. It is recommended to connect the pullups with the shortest possible stub.

Series resistor (0 Ω) for the I2C interface signals is good to have. For I2C0..3 interface, series resistors could be used to control the falling edge slew rate. The value depends on the custom board design and could be finalized after testing.

For more information, refer below FAQs:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – I2C interface

[FAQ] AM62A7 / AM62A3 Custom board hardware design – I2C interface

[FAQ] AM62P / AM62P-Q1 Custom board hardware design – I2C interface

[FAQ] AM62A7-Q1: Internal pull configuration registers for MCU_I2C0 and WKUP_I2C0

If the plan is to use TI provided software, be sure to connect recommended processor I2C (I2C0 for AM62x - TPS65219) interface to the PMIC, as this is the I2C interface used for PMIC control.

Note

When I2C3 interface is used, refer the I2C3 note (can be multiplexed to more than one pin) in the *Timing and Switching Characteristics, Peripherals, I2C* section of the device-specific data sheet.

Note

Refer *Exceptions* in section *Timing and Switching Characteristics, I2C* of device-specific data sheet during the custom board design.

7.5 User Interface (CSIRX0, DPI, OLDI, DSI), GPIO and Hardware Diagnostics

7.5.1 Camera Serial Interface (CSI-Rx (CSI-2 port, CSIRX0 Instance))

Refer device-specific data sheet for supported data rate.

7.5.1.1 CSIRX0 Used

The processor CSIRX0 interface is powered by CSIRX0 (CSIRX0 and DSITX0 for AM62Px) core supply VDDA_CORE_CSIRX0 (VDDA_CORE_CSI_DSI and VDDA_CORE_DSI_CLK for AM62Px) and CSIRX0 (CSIRX0 and DSITX0 for AM62Px) 1.8 V analog supply VDDA_1P8_CSIRX0 (VDDA_1P8_CSI_DSI for AM62Px).

Connect a resistor between CSI0_RXRCALIB (close to processor) and VSS. Refer device-specific data sheet for recommended resistor value and tolerance.

7.5.1.2 CSIRX0 Not Used

CSIRX0 when not used has specific connection requirements for interface signals and power supplies.

For connecting the interface signals, power supplies (core and analog), refer the *Pin Connectivity Requirements* section of the device-specific data sheet.

When boundary scan function is used, CSIRX0 (CSIRX0 and DSITX0 for AM62Px) supplies ((VDDA_CORE_CSIRX0 and VDDA_1P8_CSIRX0), (VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_CSI_DSI for AM62Px)) are required to be connected to the recommended supply rails. Decoupling capacitors on the supply pins are recommended. Bulk capacitors and ferrites are optional.

When boundary scan function is not used (and DSITX0 for AM62P), it is recommended to connect CSIRX0 (CSIRX0 and DSITX0 for AM62Px) supplies ((VDDA_CORE_CSIRX0 and VDDA_1P8_CSIRX0), (VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_CSI_DSI for AM62Px)) to VSS through separate 0 Ω resistors. Decoupling capacitors, bulk capacitors and ferrites are not recommended to be populated.

7.5.2 Display Subsystem

7.5.2.1 Display Parallel Interface (DPI)

7.5.2.1.1 AM625 / AM623 / AM625SIP / AM625-Q1 and AM62A7 / AM62A3 and AM62P / AM62P-Q1

7.5.2.1.1.1 IO Power Supply

The processor DPI interface is powered by VDDSHV3 (Dual-voltage IO) supply rail (IO supply for IO group 3).

7.5.2.1.1.2 DPI (Attached Device) Reset

It is recommended to implement the device reset using a dual input AND gate logic. One of the AND gate input is connected to the processor general purpose input/output (GPIO) pin. The AND gate input has provision for pullup and 0 Ω to isolate the GPIO for testing or debug. The other AND gate input is the Main Domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.

7.5.2.1.1.3 Connection

Verify display (RGB) connections.

Interface support includes 12-, 16-, 18-, and 24-bit RGB active matrix displays. When connecting only 16-bit data to an 18-bit panel (BGR565 to BGR666), connect D0-D4 to B1-B5 on LCD, D5-D10 to G0-G5 on the LCD, and D11-D15 to R1-R5 on LCD. On the 18-bit panel, connect B0->B5, R0->R5.

7.5.2.1.1.4 Signals Termination

Provide provision for connecting a series resistor (0 Ω) for VOUT0_PCLK (Pixel Clock Output) (close to processor). If space is not a constraint, recommend adding series resistors (0 Ω) for all other control and data pins.

7.5.2.1.1.5 Capacitors for the Power Supply Rails

Verify if bulk and decoupling capacitors are provided for VDDSHV3 (Dual-voltage IO) supply rail and the attached device.

Follow the device-specific SK implementation whenever recommendations are not available.

7.5.2.1.2 AM620-Q1

Not Supported.

7.5.2.2 Open LVDS Display Interface (OLDI)

Refer device-specific data sheet for supported display resolution.

7.5.2.2.1 AM625 / AM623 / AM625SIP / AM625-Q1 and AM62P / AM62P-Q1

7.5.2.2.1.1 OLDI0 Used

7.5.2.2.1.1.1 IO Power Supply

The processor OLDI interface is powered by VDDA_1P8_OLDI0 (OLDI0 1.8 V analog supply rail).

7.5.2.2.1.1.2 OLDI (Attached Device) Reset

It is recommended to implement the device reset using a dual input AND gate logic. One of the AND gate input is connected to the processor general purpose input/output (GPIO) pin. The AND gate input has provision for pullup and 0 Ω to isolate the GPIO for testing or debug. The other AND gate input is the Main Domain warm reset status output (RESETSTATz) signal.

In case an ANDing logic is not used and the processor Main Domain warm reset status output (RESETSTATz) is used to reset the attached device, ensure the IO voltage level of the attached device matches the RESETSTATz IO voltage level. A level translator is recommended to match the IO voltage level.

7.5.2.2.1.1.3 OLDI Interface Compatibility

For verifying the voltage level compatibility, refer the *OLDI LVDS (OLDI) Electrical Characteristics* section of the device-specific data sheet.

7.5.2.2.1.1.4 Capacitors for the Power Supply Rails

Verify if required bulk and decoupling capacitors are provided for VDDA_1P8_OLDI0 supply rail.

Follow the device-specific SK implementation whenever recommendations are not available.

7.5.2.2.1.2 OLDI0 Not Used

OLDI0 when not used has specific connection requirements for interface signals. For connecting the interface signals, refer the *Pin Connectivity Requirements* section of the device-specific data sheet.

The OLDI0 1.8 V analog supply rail (VDDA_1P8_OLDI0) is recommended to be powered by a valid 1.8 V source. Ferrite and bulk capacitor are optional.

7.5.2.2.1.3 Additional Information

The signals are recommended to be connected as a point-to-point interface from the processor to a connector (display). Ensure there are no stubs.

Ensure any board-level implementation complies with the physical layer definition of *IEEE1596.3* standard and *ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) interface Circuits)*.

7.5.2.2.2 AM620-Q1 and AM62A7 / AM62A3

Not Supported.

7.5.2.3 Display Serial Interface (DSI)

Refer device-specific data sheet for supported display resolution.

7.5.2.3.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 and AM62A7 / AM62A3

Not supported

7.5.2.3.2 AM62P / AM62P-Q1

7.5.2.3.2.1 DSITX0 Used

The processor DSITX0 interface is powered by CSIRX0 and DSITX0 core supplies VDDA_CORE_CSI_DSI and VDDA_CORE_DSI_CLK and CSIRX0 and DSITX0 1.8 V analog supply VDDA_1P8_CSI_DSI.

Connect a resistor between DSI0_TXRCALIB (close to processor) and VSS. Refer device-specific data sheet for recommended resistor value and tolerance.

7.5.2.3.2.2 DSITX0 Not Used

DSITX0 when not used has specific connection requirements for interface signals and power supplies.

For connecting the interface signals, power supplies (core and analog), refer the *Pin Connectivity Requirements* section of the device-specific data sheet.

When boundary scan function is used, CSIRX0 and DSITX0 supplies (VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_CSI_DSI) are required to be connected to the recommended supply rails. Decoupling capacitors on the supply pins are recommended. Bulk capacitors and ferrites are optional.

When boundary scan function and CSIRX0 are not used, it is recommended to connect CSIRX0 and DSITX0 supplies (VDDA_CORE_CSI_DSI, VDDA_CORE_DSI_CLK and VDDA_1P8_CSI_DSI) to VSS through separate 0 Ω resistors. Decoupling capacitors, bulk capacitors and ferrites are not recommended to be populated.

7.5.3 General Purpose Input/Output (GPIO)

7.5.3.1 CLKOUT Available on GPIO

A buffered MCU_OSC0_XO is available by default on the WKUP_CLKOUT0 for AM62x family of processors. MCU_OSC0_XO can be configured as WKUP_CLKOUT0 for AM62Ax and AM62Px family of processors.

7.5.3.2 Connection and External Buffering

Recommend adding series resistor (Value TBD, use case dependent) to limit the current. It is recommended to externally buffer the GPIO outputs when higher (above the data sheet specified value) current sourcing is required.

7.5.3.3 Additional Information

Pins or Pads on unused interfaces can typically be left unconnected, unless otherwise stated. Many of the IOs have a *Pad Configuration Register* that provides control over the input capabilities of the IO (RXENABLE field in each conf_<module>_<pin> register). For more details, refer the *Control Module* chapter of the device-specific TRM. Software can disable the IO receive buffers (that is, RXENABLE=0) that are not connected in the design as soon as possible during initialization. Software needs to be ensure that it does not accidentally enable the receiver of an IO (by setting the RXENABLE bit) when the associated pin is floating.

Note

For specific guidance on configuring certain unused pins, refer the *Pin Connectivity requirements* section of the device-specific data sheet.

Note

For specific guidance on configuring IOs, refer the *Pad Configuration Registers* chapter of the device-specific TRM.

7.5.4 On-board Hardware Diagnostics

7.5.4.1 Monitoring of On-Board Supply Voltages Using Processor

Voltage monitor pins can be used to monitor the external supply rails. The VMON_1P8_SOC and VMON_3P3_SOC can be directly connected to 1.8 V or 3.3 V. The VMON_VSYS is connected through an external voltage divider and provides flexibility to monitor any of the supply rail.

7.5.4.1.1 Voltage Monitor Pins Used

It is recommended to connect the main voltage powering the board (such as 3.3 V, 5 V or other voltage levels) to the VMON_VSYS pin through an external resistor voltage divider (0.45 V ± 3 %) for early supply failure indication. It is recommend to implement a noise filter (capacitor) across the resistor voltage divider output since VMON_VSYS has minimum hysteresis and a high-bandwidth response to transients as described in the *System Power Supply Monitor Design Guidelines* section of the device-specific data sheet.

Connect VMON_1P8_SOC and VMON_3P3_SOC pins directly to their respective supplies. Refer *Recommended Operating Conditions* section of the device-specific data sheet for the allowed supply voltage range.

Note

For VMON_VSYS, fail-safe condition is valid when the recommendations in section *System Power Supply Monitor Design Guidelines* of device-specific data sheet are followed.

For VMON_1P8_SOC and VMON_3P3_SOC pins, the fail-safe condition is valid when the supply voltage connected is within the *Recommended Operating Conditions* or *Absolute Maximum Ratings* sections of device-specific data sheet.

7.5.4.1.2 Voltage Monitor Pins Not Used

It is recommended to use VMON_VSYS for early supply failure indication. When not used, connect VMON_VSYS and VMON_3P3_SOC pins to VSS through separate 0 Ω resistors and add test point for future expansion.

It is recommended to connect the VMON_1P8_SOC pin to respective supply. Grounding this pin would short internal 1.8 V supply and this is not allowed.

7.5.4.2 Internal Temperature Monitoring

The temperature monitors (sensors) are placed near the anticipated hot spots of the processor. You could read the on-die temperature sensors in Linux and perform thermal management. Refer E2E thread.

The Voltage and Thermal Manager (VTM) module on the processor supports voltage and thermal management of the processor by providing control of on-chip temperature sensors.

The processor supports a single VTM module, VTM0, which is located in the WKUP domain. VTM0 has two associated temperature monitors, Temp_Sensor_Main_0, and Temp_Sensor_Main_1, each of which are located near hot-spots of the processor die.

TI does not spec or guarantee any accuracy for the VTM module with regard to temperature measurements. A ± 7°C accuracy is provided to give an indication and internal characterization performed to confirm the measurements are within specified range.

7.5.4.3 Connection of Error Signal Output (MCU_ERRORn)

It is recommended to connect the MCU_ERRORn signal as per the *Pin Connectivity Requirements* section of the device-specific data sheet for testing or when using the signal for other board level functions.

7.5.4.4 High Frequency Oscillator (MCU_OSC0) Clock Loss Detection

The processor supports HFOSC0 clock loss detection circuitry to detect HFOSC0_CLK malfunction (stops). Dedicated hardware logic monitors HFOSC0 clock using CLK_12M_RC clock. When HFOSC0_CLK stops toggling for 9 CLK_12M_RC clock periods, a HFOSC0 clock stop loss condition is detected. If CTRLMMR_MCU_PLL_CLKSEL [8] CLKLOSS_SWTCH_EN is set, the reference clock is switched from HFOSC0_CLKOUT to CLK_12M_RC to allow the processor to operate with a slower clock.

During clock-loss condition, the processor reports the error to the external device through MCU_ERRORn pin by driving the pin low. The recovery mechanism is up to the external device (such as a PMIC to take action).

Example, doing a full board power cycle to see if the board recovers. If the board does not recover then the processor has to indicate user to take alternate actions or perform board level tests such as checking on-board system clocks, external crystal or supply rails.

7.6 Verifying Board Level Design Issues

7.6.1 Processor Pin Configuration Using Pinmux Tool

Recommend verifying the processor peripheral and IO configuration using the TI *SysConfig-PinMux* tool to ensure valid IOSETs have been configured.

For more information, refer the PinmuxConfigSummary.csv file provided by the SysConfig-PinMux tool.

7.6.2 Schematics Configurations

Verify if all the circuit options provided for alternate functionality or testing that are not required for the normal functioning of the board or could affect or influence custom board performance are marked as DNI.

7.6.3 Connecting Supply Rails to Pullups

Connecting a signal pullup to the wrong IO supply rail could cause leakage between the IO rails of the processor and affect the custom board performance/processor reliability. Each signal has an associated IO supply rail (Ex: VDDSHVx [x=0..6]). For more information, refer the *Pin Attributes* table in the device-specific data sheet.

Example, if you want to pullup SPI0_CLK signal in any mux mode (EHRPWM1_A, GPIO1_17, and so forth), pullup the signal supply rail connected to VDDSHV0.

7.6.4 Peripheral (Sub System) Clock Outputs

For any of the processor peripheral that has a clock output, configure the RXACTIVE bit of the appropriate CTRLMMR_MCU_PADCONFIGx / CTRLMMR_PADCONFIGy registers. This bit configuration is required for the clock output to work properly.

7.6.5 General Debug

7.6.5.1 Clock Output for Board Bring-Up, Test or Debug

The below clock outputs are available on the processor for test and debug purposes only.

- OBSCLK0, MCU_OBSCLK0 (recommended): Observation clock outputs

  OBSCLK0, MCU_OBSCLK0 are observation clock outputs for test and debug purposes only. OBSCLK pins can be used to select one of the several different clocks as output. We do not expect this signal to be used as a clock source for any external device. As stated in the data sheet, this signal is provided for test and debug purposes only.
- SYSCLKOUT0 (optional): SYSCLK0 is divided by 4 and then sent out of the processor as a LVCMOS clock signal (SYSCLKOUT0)
- MCU_SYSCLKOUT0 (optional): MCU_SYSCLK0 is divided by 4 and then sent out of the processor as a LVCMOS clock signal (MCU_SYSCLKOUT0)

In case the processor pins designated OBSCLK0 (available on two pins in AM62x), OBSCLK0..1 (in AM62Ax and AM62Px), MCU_OBSCLK0, SYSCLKOUT0, MCU_SYSCLKOUT0 are not used, provide a test point for test or debug. Recommend adding pull resistors to these pads.

In case these pins are used, a test point can be inserted on the trace and provision to isolated these signals from the attached devices can be provided for test or debug.

System clock output pins (MCU_SYSCLKOUT0 and SYSCLKOUT0) are hardwired to dedicated clock resources.

7.6.5.2 Additional Information

It is recommended to provide test points for MCU_RESETSTATz, RESETSTATz and PORz_OUT for testing or debug when not used.

For other on-board devices (DC/DC Converter or LDO or Sensor) that have an alert output, over current indication output or PG (power good) output that is not used, provide a pullup and test point for testing or future enhancements.

8 Layout Notes (Added on the Schematic)

Recommend adding the required design notes for the processor peripherals (Example: USB2.0 interface, Ethernet interface, Camera interface, Display (OLDI0) interface (AM625 / AM623 / AM625SIP / AM625-Q1 / AM62P / AM62P-Q1), Display (DSITX0) interface (AM62P / AM62P-Q1), eMMC, SD, and other available processor peripherals). Notes added could include Board Boot mode configurations, placement of series and parallel resistors, placement of decoupling and bulk capacitors.

Consider adding the required or applicable design notes to the processor attached devices and on-board devices. This helps understand the implementation rationale.

Mark all differential signals, critical signals and specify the target impedance (as required). See below examples:

- Refer to the *AM62Ax / AM62Px DDR Board Design and Layout Guidelines* for the recommended target impedance for the LPDDR4 clock, address and control signals.
- The differential impedance for the USB2.0 data lines must be within the specified tolerance for a nominal value of 90 Ω.
- The differential impedance for the CSI-Rx, DSITX and OLDI signals must be within the specified tolerance for a nominal value of 100 Ω.

9 Custom Board Design Simulation

The baseline drive impedance and ODT settings for memory (DDR4 / LPDDR4) derived from the Signal Integrity (SI) simulations performed on the SK.

It is recommended to perform simulation for the custom design as the configuration values could be different.

To get an overview of the basic system-level board extraction, simulation, and analysis methodologies for high speed LPDDR4 interfaces, refer *LPDDR4 Board Design Simulations* chapter of the *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines* application note.

The drive strength is adjustable using the DDR Register Configuration Tool on SysConfig.

For more information, see the [FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration. This is a generic FAQ and can also be used for AM625 / AM623 / AM625-Q1 / AM620-Q1 and AM62P / AM62P-Q1 family of processors.

10 Additional References

Additional references include FAQs and *Hardware Design Guide* for processor. Schematics for attached devices including PMIC and EPHY.

10.1 FAQ Covering AM6xx Processor Family

The below FAQ summarizes key collaterals that could be referenced during custom board design:

[FAQ] AM64x, AM62x, AM62Ax, AM62Px Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

Note

While reviewing the SK PDF schematics, look for the FAQ links that can be clicked for more information.

10.2 FAQs - Processor Product Family Wise

Based on customer interactions, queries and learning, FAQs have been created to support customers during custom board design. Refer below list of FAQs created that could be referred during custom board design along with other available design collaterals including the *Hardware Design Guide* and the *Schematic Design and Review Checklist*.

[FAQ] AM625, AM623, AM625SIP, AM625-Q1, AM620-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

Refer below FAQ that lists all the available FAQs including software related FAQs:

[FAQ] AM62x , AM62Ax & AM62P Frequently Asked Questions List

10.3 Processor Attached Devices

TPS65219 Schematic, Layout Checklist

TPS65931211-Q1 PMIC User Guide for AM62A

Ethernet PHY PCB Design Layout Checklist

11 Summary

This *Schematic Design and Review Checklist* is provided as a guide for use during the schematic design and review. The recommendations provided in this document could help simplify the design, reduce errors, reduce debug time and could possibly minimize future re-spins of the board.

12 References

12.1 AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1

- Texas Instruments: *AM62x Sitara™ Processors Data Sheet*
- Texas Instruments: *AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM*
- Texas Instruments: *AM62x Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM62x Silicon Errata*
- Texas Instruments: *Hardware Design Guide for AM62x Family of Processors*
- Texas Instruments: *Starter Kit SK-AM62B-P1*
- Texas Instruments: *Starter Kit SK-AM62-LP*
- Texas Instruments: *Starter Kit SK-AM62-SIP*
- Texas Instruments: *AM62x Power Consumption*
- Texas Instruments: *AM62x Maximum Current Ratings*
- Texas Instruments: *AM62x Power Estimation Tool*
- Texas Instruments: *Powering the AM62x With the TPS65219 PMIC*
- Texas Instruments: *Powering the AM625SIP With the TPS65219 PMIC*
- Texas Instruments: *Discrete Power Solution for AM62x*
- Texas Instruments: *AM625 / AM623 (ALW) Escape Routing PCB Design*
- Texas Instruments: *AM625-Q1 / AM620-Q1 (AMC) Escape Routing for PCB Design*
- Texas Instruments: *AM625SIP (AMK) Escape Routing for PCB Design*
- Texas Instruments: *AM625 / AM623 / AM625-Q1 / AM620-Q1 DDR Board Design and Layout Guidelines*
- Texas Instruments: *PRU-ICSS Feature Comparison*
- Texas Instruments: *How the AM625SIP Processor Accelerates Development by Integrating LPDDR4*

12.2 AM62A7 / AM62A3 / AM62A7-Q1 / AM62A3-Q1

- Texas Instruments: *AM62Ax Sitara™ Processors Data Sheet*
- Texas Instruments: *AM62Ax Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM62Ax Silicon Errata*
- Texas Instruments: *Starter Kit SK-AM62A-LP*
- Texas Instruments: *Hardware Design Guide for AM62A7 / AM62A3 Family of Processors*
- Texas Instruments: *AM62Ax Maximum Current Ratings*
- Texas Instruments: *AM62Ax Power Estimation Tool*
- Texas Instruments: *PMIC Solution for AM62Ax*
- Texas Instruments: *AM62Ax Escape Routing PCB Design*
- Texas Instruments: *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines*

12.3 AM62P / AM62P-Q1

- Texas Instruments: *AM62Px Sitara™ Processors Data Sheet*
- Texas Instruments: *AM62Px Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM62Px Silicon Errata*
- Texas Instruments: *Starter Kit SK-AM62P-LP*
- Texas Instruments: *Hardware Design Guide for AM62P / AM62P-Q1 Family of Processors*
- Texas Instruments: *AM62Px Escape Routing for PCB Design*
- Texas Instruments: *AM62Ax / AM62Px LPDDR4 Board Design and Layout Guidelines*

12.4 Common for all Family of Processors

- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*

- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *High-Speed Layout Guidelines*
- Texas Instruments: *Jacinto 7 High-Speed Interface Layout Guidelines*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *XDS Target Connection Guide*
- *IEEE1596.3*
- *ANSI/TIA/EIA644-A standard (Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*
- Texas Instruments: *General Hardware Design/BGA PCB Design/BGA Decoupling*
- Texas Instruments: *MSL Ratings and Reflow Profiles*
- Texas Instruments: *Moisture sensitivity level search*
- Texas Instruments: *Clocking Design Guide for KeyStone Devices*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments: *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design*
- Texas Instruments: *Jacinto™ 7 DDRSS Register Configuration Tool*
- Texas Instruments: *Using IBIS Models for Timing Analysis*

12.5 Master List of Available FAQs - Processor Family Wise

A master list of the FAQs are available that can be used to quickly view the available list of FAQs for the selected processor or family of processors.

[FAQ] AM625, AM623, AM625SIP, AM625-Q1, AM620-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM62A7, AM62A7-Q1, AM62A3, AM62A3-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

[FAQ] AM62P, AM62P-Q1 Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and Starter kit

12.6 FAQs Including Software Related FAQs

[FAQ] AM62x , AM62Ax & AM62P Frequently Asked Questions List

12.7 FAQs for Attached Devices

[FAQ] TPS65219: Benefits of a PMIC vs discrete solution to power Sitara AM62x MPU

[FAQ] DP83869-EP: Ethernet compliance Testing failure

13 Terminology

BOM – Bill of Materials

CAN – Controller Area Network

CPPI – Communications Port Programming Interface

CPSW3G – Common Platform Ethernet Switch 3-port Gigabit

CSIRX – Camera Streaming Interface Receiver

DFU – Device Firmware Upgrade

DNI – Do Not Install

DPI – Display Parallel Interface

DRD – Dual-Role Device

DSI – Display Serial Interface

E2E – Engineer to Engineer

ECC – Error-Correcting Code

EMC – Electromagnetic Compatibility

EMI – Electromagnetic Interference

eMMC – embedded Multi-Media Card

EMU – Emulation Control

EOS – Electrical Over-Stress

ESD – Electrostatic discharge

ESL – Effective Series Inductance

ESR – Effective Series Resistance

FAQ – Frequently Asked Question

FET – Field-Effect Transistor

GEMAC – Gigabit Ethernet Media Access Controller

GPIO – General Purpose Input/Output

GPMC – General-Purpose Memory Controller

HS-RTDX – High Speed Real Time Data eXchange

I2C – Inter-Integrated Circuit

IBIS – Input/Output Buffer Information Specification

IEP – Industrial Ethernet Peripheral

JTAG – Joint Test Action Group

LDO – Low Dropout

LVCMOS – Low Voltage Complementary Metal Oxide Semiconductor

LVDS – Low Voltage Differential Signaling

MAC – Media Access Controller

MCASP – Multichannel Audio Serial Ports

MCSPI – Multichannel Serial Peripheral Interface

MCU – Micro Controller Unit

MDI – Medium Dependent Interface

MDIO – Management Data Input/Output

MMC – Multi-Media Card

MMCSD – Multi-Media Card/Secure Digital

ODT – On-die Termination

OLDI – Open LVDS Display Interface

OSPI – Octal Serial Peripheral Interface

PCB – Printed Circuit Board

PDN – Power Distribution Network

PET – Power Estimation Tool

PMIC – Power Management Integrated Circuit

POR – Power-on Reset

PRUSS – Programmable Real-Time Unit Subsystem

QSPI – Quad Serial Peripheral Interface

RGMII – Reduced Gigabit Media Independent Interface

RMII – Reduced Media Independent Interface

ROC – Recommended Operating Condition

SD – Secure Digital

SDIO – Secure Digital Input Output

SPI – Serial Peripheral Interface

TCK – Test Clock Input

TDI – Test Data Input

TDO – Test Data Output

TEN – Test Enable

TMS – Test Mode Select Input

TRM – Technical Reference Manual

TRSTn – Reset

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

WKUP – Wake-up

XDS – eXtended Development System

14 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 1, 2024 to February 29, 2024 (from Revision D (January 2024) to Revision E (February 2024)) **Page**

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