Application Note

Hardware Design Guide for AM62A7/AM62A3 Devices

ABSTRACT

This hardware design guide gives an overview of the design considerations to be followed by the board designers using AM62A7/AM62A3 family of processors. This application note is intended to be used at different stages of board design as a guide by the designers. The hardware design guide additionally references to collaterals (device-specific and common) that could help the designers to optimize the efforts during the board design.

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1 Introduction

The Hardware Design Guide for AM62A7/AM62A3 family of Devices Application Report provides a starting point for the engineers designing with AM62A7/AM62A3 processors. It provides an overview of the flow, design efforts and highlights important areas that must be addressed. Note that this document does not contain all of the information needed to complete the board design. In many cases, it refers to the device-specific data manual or to various other user's guides as sources for specific information.

The document is organized in a sequential manner. It starts from decisions that must be made during the initial planning stages of the design, through the selection of key devices, electrical, and thermal requirements. For ensuring design success, issues discussed in each of the section should be resolved before moving to the next section.

Note

This guide may not cover every aspect of the board design.

Note

The AM62A7/AM62A3 device has capabilities to help board designers address safety requirements. This guide is focused on non-safety applications.

1.1 Before Getting Started

The AM62A7/AM62A3 family of processors includes wide variety of capabilities, not all of which will be used in every design. Consequently, the requirements for different designs using the same device can vary widely depending on the target application. Designers must understand the requirements before determining the details of the design. In addition, the design may require additional circuitry to operate correctly in the target environment. For the selected device and determine the following, see latest collaterals on TI.com like the device-specific Data Sheet, Errata, TRM and EVM User's guides:

- What are the expected environmental conditions for the device operation, target boot mode, storage type and interfaces used
- How much processing will each of the cores in the selected device be performing
- Peripherals attached to the processor

1.2 Device (Processor) Selection

Selection of device is the most important step during the board design process. For selecting the device variant, features, and speed grade that is applicable, see the *Functional Block Diagram* and *Device Comparison* section in device-specific data sheet.

1.3 Technical Documentation

A number of documents relevant to the selected device are provided on the product folder page. Read through relevant documents before the start of design.

The below links summarizes the collaterals that can be referred when starting a custom design.

AM62A7 and AM62A7-Q1 Custom board hardware design – Collaterals to Get started

AM62A3 and AM62A3-Q1 Custom board hardware design – Collaterals to Get started

1.4 Design Documentation

Throughout this guide, TI recommends generating a design document periodically. Generating and storing this information provides you with the foundation for the documentation package, and this design document is needed when seeking external review support.

2 System Block Diagram

A detailed System Block Diagram, covering all the functional blocks and required interfaces is key to a successful design.

2.1 Creating the System Block Diagram

The first step during the board design is to create a detailed System Block Diagram. The System Block Diagram includes all major functional blocks, associated devices, interfaces and illustrates the I/Os (ports) used for interconnecting the devices.

The following is a collection of resources to support the System Block Diagram creation process:

- The SK-AM62A-LP EVM (AM62A starter kit for low-power Sitara™ processors) and any other available EVMs are a good source to start with the design.
- The TI.com links referred to below provide device-specific Functional Block Diagrams, Data Sheet, User's Guide, Errata, Application Notes, design considerations, and other related information for various applications. The design and development section includes EVM information, design tools, simulation models and software. As part of support and training, links to commonly applicable E2E threads and FAQs are available.
  - AM62A7 Product Folder
  - AM62A7-Q1 Product Folder
  - AM62A3 Product Folder
  - AM62A3-Q1 Product Folder

2.2 Selecting the Boot Mode

The System Block Diagram should indicate the interface used for booting. This includes the primary boot and the backup boot.

The AM62A7/AM62A3 device contains multiple peripheral interfaces that support boot mode. Examples include: eMMC, MultiMedia Card/Secure Data Memory Card (MMC/SD), QSPI, OSPI, GPMC (NOR/NAND), Ethernet, USB (Target & Host), Serial Flash, xSPI and Inter-Integrated Circuit (I2C). The AM62A7/AM62A3 device supports a primary boot mode option and an optional backup boot mode. If the primary boot source fails to boot, the ROM moves on to the backup mode.

The boot mode pins and the associated resistor configurations provide inputs on the boot mode to be used by the ROM code during boot. These pins are sampled at power-on-reset, and must be properly set up before releasing (deassertion) the reset.

Boot mode configurations can be categorized as below:

PLL Config: BOOTMODE [02:00] – Denotes system clock frequency (MCU_OSC0_XI/XO) to the ROM code for PLL configuration.

Primary Boot Mode: BOOTMODE [06:03] – Selects the configured boot (primary) mode after POR, (that is), the peripheral/memory to boot from.

Primary Boot Mode Config: BOOTMODE [09:07] – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected.

Backup Boot Mode: BOOTMODE [12:10] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot fails.

Backup Boot Mode Config: BOOTMODE [13] – This pin provides optional configurations for the backup boot devices.

Reserved: BOOTMODE [15:14] – Reserved pins.

Key considerations for boot mode configuration:

- TI recommends including provision to configure boot modes used during development, such as UART boot or No-boot mode for JTAG debug.
- Boot pins have other functions after reset. Ensure the board design takes this into account when choosing pullup/pulldown resistors for the boot pins. If these pins are driven by another device, they must return to the proper boot configuration levels whenever the device is reset (indicated by the PORz_OUT pin) to enable it to boot properly.
- The functionality of some boot mode pins are reserved. These pins should not be left floating and must be terminated (pullup or pulldown). For details regarding termination of reserved boot mode pins, see the *Boot Mode Pins* section of the *Initialization* chapter of the device-specific TRM.

For details regarding boot modes, see the *Initialization* chapter of the device-specific TRM.

Note

It is the designers responsibility to set the boot mode configuration (via pullups or pulldowns, and optionally jumpers/switches) depending on the desired boot scenario.

2.3 Confirming Pin Multiplexing Compatibility

The processor contains a number of peripheral interfaces. To optimize size, pin count, package cost while maintaining maximum functionality, many of the device pads (pins) can multiplex up to eight signal functions. Thus, not all peripheral interface instances can be used simultaneously.

Texas Instruments has developed SysConfig-PinMux Tool that helps a board designer select the appropriate function using pin-multiplexing configuration too for their AM62A7/AM62A3 based board design.

Note

The pinmux configuration generated using SysConfig-PinMux Tool for the design should be saved along with other design documentation.

3 Power Supply

After completing the device (processor) selection and system block diagram, next step in the design process is to determine the power supply architecture for the selected processor.

3.1 Power Supply Architecture

The power supply architecture that can be considered are listed below:

3.1.1 Integrated Power Architecture

The power architecture could be based on Multi-channel ICs (PMIC) such as TPS6593-Q1.

For more information, see the *Starter Kit SK-AM62A-LP EVM* schematic.

3.1.2 Discrete Power Architecture

The power architecture could be based on DC-DC converters and LDOs.

3.2 Power (Supply) Rails

For the complete list of processor power supply rails and recommended operating range, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet. The following sections provide additional details about select power rails.

3.2.1 Core Supply

Core supplies VDD_CORE, VDDA_CORE_CSIRX0, VDDA_CORE_USB, and VDDA_DDR_PLL0 are always sourced from the same power source and can be operated at 0.75 V or 0.85 V. When these supplies are operating at 0.75 V, these are required to be ramped up prior to all 0.85 V supplies. VDDR_CORE is specified to operate at 0.85 V only. VDD_CORE and VDDR_CORE are expected to be powered by the same source so these ramp together when VDD_CORE is operating at 0.85 V.

VDD_CANUART can be connected to always on power sources when using Partial I/O low power mode or to the same power source as VDD_CORE when not using Partial I/O low power mode.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.2 Peripheral Power Supply

The processor includes dedicated peripheral supply pins for USB, CSIRX, PLLs and are operated at 1.8 V. An additional 3.3 V analog supply is required for USB. The DDR PHY and DDR clock IO supply can be 1.1 V.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3 Internal LDOs for I/O groups

The processor includes nine internal LDOs, with the output of each connected to a pin (CAP_VDDSx [x=0-6], CAP_VDDS_CANUART, CAP_VDDS_MCU) on the processor. A capacitor must be connected to each of these LDO output pins. For guidance on the capacitor selection and connection, see the *Power Supply* section in the *Signal Descriptions* chapter of the device-specific data sheet.

3.2.4 Dual-Voltage LVCMOS I/Os

The processor includes nine dual-voltage I/O domains (VDDSHVx [x=0-6], VDDSHV_MCU and VDDSHV_CANUART), where each domain provides power to a fixed set of I/Os. Each I/O domain can be configured for 3.3 V or 1.8 V, which determines a common operating voltage for the entire set of I/Os powered by the respective I/O domain. All signals connected to these domains must operate from the same power source that is being used to power the respective VDDSHVx supply rail. The AM62A7/AM62A3 I/O buffers are not fail-safe. The supply voltage for the VDDSHVx rails must be present before any voltage is applied to the associated I/Os.

I/O grouping information is summarized below:

VDDSHV0 – Voltage for the General I/O group

VDDSHV1 – Voltage for the Flash I/O group

VDDSHV2 – Voltage for the GEMAC I/O group

VDDSHV3 – Voltage for the GPMC I/O group

VDDSHV4 – Voltage for the MMC0 I/O group

VDDSHV5 – Voltage for the MMC1 I/O group

VDDSHV6 – Voltage for the MMC2 I/O group

VDDSHV_MCU – Voltage for the WKUP_MCU I/O group

VDDSHV_CANUART – Voltage for the CANUART I/O group

3.2.5 Dual-Voltage Dynamic Switching I/Os for SDIO

Integrated LDO to support SD card I/O voltage switching are not available. The Selected LDO should be able to handle the required voltage transition for the SD interface.

3.2.6 VPP (eFuse ROM programming supply)

VPP pin can be left floating (HiZ) or terminated to ground during power-up/power-down sequences and during normal device operation. This supply is only sourced while programming the eFuse. The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be ramped up after completion of proper device power-up sequence.
- The VPP supply has high current transients and local bulk capacitors are likely needed near the VPP pin to assist the LDO transient response.
- Select the power supply with quick discharge capability or use a discharge resistor. A Maximum current of 400 mA is required for programming. It is recommended to use an LDO for power the VPP.
- If an external power supply is used, the supply is applied after the processor power supplies are stable.
- The VPP power supply must be disabled (left floating (HiZ) or grounded) when not programming the OTP registers.

For more information, see the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.3 Determining System Power Requirements

The maximum and minimum current requirements for each of these supply voltage rails are not available in the device-specific data sheet. These requirements are highly application-dependent and must be calculated for a specific use case.

3.4 Power Supply Filters

The processor has multiple analog supply pins that provide power to sensitive analog circuitry such as VDDA_MCU, VDDA_DDR_PLL0, VDDA_PLLx [x=0-4], VDDA_1P8_CSIRX0 and VDDS_OSC0. These must be attached to filtered supply sources.

3.5 Power Supply Decoupling and Bulk Capacitors

To properly decouple the processor and supply planes from system noise, decoupling and bulk capacitors are required. For adding bulk and decoupling capacitors, see the *Starter Kit SK-AM62A-LP EVM* schematic.

For guidance on optimizing the selection and placement of the decoupling and bulk capacitors, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis*.

3.5.1 Note on PDN target impedance

Please note that we do not provide target impedance values since the target impedance calculation includes reference to the max current on the rail and is dependent on use case.

For updates on the target impedance, see to the AM62A7/AM62A7-Q1 or AM62A3/AM62A3-Q1 related FAQ listed in the document or E2.

3.6 Power Supply Sequencing

A detailed diagram of the power supply sequencing (Power-Up/Power-Down) for the processor are available in the device-specific data sheet. All power supplies associated with the processor should allow for controlled sequencing using on-board logic when using discrete power solution or a PMIC-based power supply.

3.7 Supply Diagnostics

The processor includes below voltage monitors:

- VMON_1V8_SOC and VMON_3V3_SOC: These pins are recommended to be connected directly to their respective 1.8 V and 3.3 V supplies. An internal resistor divider is implemented inside the processor for each of these pins.
- VMON_VSYS: Connects the system voltage (3.3 V or 5 V) through a voltage divider (0.45 V ±3%). Consider implementing a capacitor for noise filtering as described in the device-specific data sheet.

For more information see the *System Power Supply Monitor Design Guidelines* section in the *Applications, Implementation, and Layout* chapter of the device-specific data sheet.

3.8 Power Supply Monitoring

For improved system performance, consider provisioning for external monitoring of supply rails and load currents.

For more information, see the *Starter Kit SK-AM62A-LP EVM* schematic.

Now that the power supply architecture and the devices for generating the supply rails have been finalized, create a block diagram that includes the power supply rails and interconnection. It is also recommended to create a power sequence diagram.

4 Clocking

The next step of the design is proper clocking, and providing appropriate clocks to all connected devices in the system. These clocks can be generated by pairing external crystals with an internal oscillator or they can be generated externally by a clock generator or oscillator. This section describes the clocks available in the processor and the requirements for these clocks.

4.1 System Clock Inputs

The processor input clocks and recommended oscillator connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet. MCU_OSC0 clock is required for proper operation of the processor.

Use of WKUP_LFOSC0 is optional, depending on the system requirements.

4.2 Unused Clock Inputs

For guidance on the recommended connections for unused clock inputs, see the *WKUP_LFOSC0 Internal Oscillator Clock* section and *WKUP_LFOSC0 Not Used* sub-section in the *Specifications* chapter of the device-specific data sheet.

4.3 Clock Output

Provision to connect the internal clocks on the pins that can be used by the attach devices (external peripherals) are available. Clock output pins includes CLKOUT0 and WKUP_CLKOUT0. WKUP_CLKOUT0 is a buffered output of the high frequency oscillator HFOSC0 available during power-up as default.

For more details, see the device-specific data sheet.

4.4 Single-Ended Clock Sources

The MCU_OSC0 and WKUP_OSC0 internal oscillators can be sourced from a crystal or an LVCMOS square-wave digital clock source. For more details, see the *Input Clocks / Oscillators* section in the *Specifications* chapter of the device-specific data sheet.

Note

Be sure to terminate the XO pin as per the device-specific data sheet recommendation when using an external clock.

4.5 Crystal Selection

When selecting a crystal, the board designer must consider the temperature and aging characteristics based on the worst case environment and expected life expectancy of the system.

For more information, see the *MCU_OSC0 Crystal Circuit Requirements* and *WKUP_LFOSC0 Crystal Electrical Characteristics* tables of the device-specific data sheet.

5 JTAG

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. Although JTAG is not required for operation, TI strongly recommends that a JTAG connection be included in the designs.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- Standard emulation: requires only five standard JTAG signals
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates, see the device-specific TRM.

5.1.2 System Implementation of JTAG / Emulation

The JTAG and Emulation pins on this processor are in same power domains. The TDI, TDO, TCK, TMS, TRSTn, EMU0 and EMU1 I/Os are powered by the VDDSHV_MCU domain. VDDSHV_MCU can be configured either 1.8 V or 3.3 V.

For most other system-level implementation details, see the *Emulation and Trace Headers Technical Reference Manual*.

5.1.3 JTAG Termination

For terminating the JTAG interface signal, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

It is recommended to provision for connecting the JTAG during using test points when a JTAG connector is not used.

6 Device Configurations and Initialization

When the voltage rails and the required clocks are present and stable, the processor reset may be deasserted (released) to start the processor boot process.

6.1 Device Reset

The processor can be reset in several ways. The methods are described in detail in the device-specific data sheet and TRM.

The processor includes three external reset input pins (MCU_PORz, MCU_RESETz, and RESETz_REQ) and three reset status output pins (MCU_RESETSTATz, PORz_OUT and RESETSTATz). Be sure to provide the terminations recommended in the *Pin Connectivity Requirements* section of device-specific data sheet.

For MCU_PORz, 3.3 V input can be applied, but the input thresholds are still a function of the 1.8 V I/O supply voltage (VDDS_OSC0).

Additional reset modes are available through internal registers and emulation.

Note that TI recommends implementing RESET using ANDing logic for on-board Media and Data Storage devices and other peripherals as applicable. One of the AND gate input is controlled by processor general-purpose input/output (GPIO) pin with provision to isolate. The other AND gate input is the Main Domain warm reset status output (RESETSTATz) Signal. Ensure the reset inputs are terminated as per the device recommendations.

In case an ANDing logic is not used and the processor reset status output is used directly to reset the attach devices, ensure the I/O levels of the attach device match the processor I/O level or use a level translator to match the levels.

A controlled power switch is recommended to reset the SD Card since power cycling the SD Card is the only way to reset the card to its default state. The 3.3 V power supply for the SD Card needs to be connected through the controlled external power switch.

For more information, see the *Starter Kit SK-AM62A-LP EVM* schematic.

6.2 Latching of the Boot Modes

For more details about the processor boot mode options, see Section 2.2.

Boot modes and certain device configuration selections are latched at the rising edge of PORz_OUT. The configuration and boot mode inputs are multiplexed with pins having GPIO or other functions. After the status (level) on these pins are latched into the configuration registers, these pins are available to be used for their primary function. The PORz_OUT pin indicates latching of boot mode configuration.

6.3 Watchdog Timer

Consider using external or internal watchdog timer based on the application requirement.

7 Peripherals

This section covers the device peripherals and modules, and is intended to be used in addition to the information provided in the device-specific data sheet, TRM, and relevant Application Notes. The three types of documents should be used as follows:

- Data Sheet: AC Timings, Guidance on pin functions, Pin mapping
- TRM: Functional Description, Programming Guide, Register offsets
- Application Notes: System-level understanding and issues

7.1 Selecting Peripherals Across Functional Domains

The processor is partitioned into three functional domains, each containing specific processing cores and peripherals:

- MAIN domain
- Microcontroller (MCU) domain
- Wake-up (WKUP) domain

For most use cases, peripherals from any of the domain can be used. All peripherals, regardless of their domain, are memory mapped, and the Arm® Cortex®-A53 cores can see and access all peripherals in the MCU and WKUP domains.

7.2 Memory

DDR Subsystem currently supports LPDDR4. For more information, see the device-specific data sheet and TRM for data bus width (32-Bit), inline ECC support, speed (up-to 3733 MT/s) and Max addressable range (16 GBytes) selection.

The allowed configurations are 1 X 32-bit or 1 X 16-bit. 1 X 8-bit configuration is not a valid configuration.

Based on the application requirement, same memory device can be used with the AM625/AM623 and AM62A7/AM62A3 devices due to the availability of 1 X 16-bit configuration.

When the AM62A7/AM62A3 devices are configured for 16-bit configuration, follow the DQS2..3 and other termination recommendations shown in the 16-Bit, Single Rank LPDDR4 Implementation example of the *AM62Ax DDR Board Design and Layout Guidelines*.

For more details, see the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

7.2.1 Processor DDR Subsystem and Device Register Configuration

The DDR controller and PHY have a large amount of parameters to configure, so to facilitate the configuration, an online tool (SysConfig tool) is provided that generates an output file that is consumed by the driver.

Choose DDR Subsystem Register Configuration in the Software Product menu and choose the required processor this tool takes system information, timing parameters from DDR data sheet, and IO parameters as inputs and then outputs a header file that the driver uses to program the DDR controller and PHY. The driver then kicks off the full training sequence.

The SDK will have an integrated configuration file for the device that is on the EVM. If you need a configuration file for a different device, you need to generate that with the DDR Register Configuration tool.

For more information, see [FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration.

7.3 Media and Data Storage Interfaces

Media and Data Storage interface support includes 3 x Secure Digital (SD) ((4b+4b+8b) (4-bit SD/SDIO, 8-bit eMMC)) interface, 1 x General-Purpose Memory Controller (GPMC) and OSPI/QSPI.

For more details, see the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4 Ethernet Interface Using CPSW3G Common Platform Switch 3-port Gigabit Ethernet

The CPSW3G interface can either be configured as a 3-port switch (interfaces to two external Ethernet ports (port 1 and 2)) or a dual independent MAC interface having their own MAC address.

CPSW3G support RMII (10/100) or RGMII (10/100/1000). For RMII interface implementation, see the *CPSW0 RMII Interface* section of the device-specific TRM. TI recommends following the *RMII Interface Typical Application (External Clock Source)* described in the device-specific TRM.

CPSW3G allows using mixed RMII/RGMII interface topology.

For more details on the Ethernet interface, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.5 Programmable Real-Time Unit Subsystem (PRUSS)

Not Supported.

7.6 Universal Serial Bus (USB) Subsystem

AM62A7/AM62A3 processor provides two USB 2.0 Ports. These Ports can be configured as USB host, USB peripheral, or USB Dual-Role Device (DRD mode). USBn_ID functionality is supported via any of the GPIO.

Follow *USB VBUS Design Guidelines* section of the device-specific data sheet for scaling the VBUS voltage.

VBUS voltage is required to be connected when the device is configured in device mode. VBUS connection is optional in host mode.

For USB connections and On-The-Go feature support, see the device-specific TRM.

For more details, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

Note the supply requirements when configuring the USB for backup mode.

7.7 General Connectivity

The processor provides multiple instances of UART, Serial Peripheral Interface (SPI), I2C, Multichannel Audio Serial Port (McASP), Enhanced Pulse Width Modulator (ePWM), Enhanced Quadrature Encoder Pulse (eQEP), eCAP, CAN with CAN-FD support and GPIOs.

For I2C interface with open drain outputs (MCU_I2C0 and WKUP_I2C0), an external termination (pullup) is recommended irrespective of peripheral usage.

An external termination (pullup) is recommended for the other I2C interfaces based on the use case. For the available I2C instances, see the device-specific data sheet.

The number of instances available depends on the application and can be configured using the SysConfig-PinMux Tool.

For more details, see the *Peripherals* chapter of the device-specific TRM.

7.8 Display Subsystem (DSS)

AM62A7/AM62A3 processor provides DPI 24-bit RGB parallel Display interface. These supports up to 2048x1080 @ 60fps and 165-MHz pixel clock support with independent PLL.

For more details, see the *Display Subsystem (DSS)* section in the *Peripherals* chapter of the device-specific TRM.

7.9 Camera Subsystem (CSI)

One Camera Serial interface (CSI-RX) - 4 Lane with DPHY-RX. Support for 1,2,3 or 4 data lane mode up to 1.5 Gbps (per lane).

The DPHY-RX only supports a single clock lane and all the data lanes are clocked at the same frequency. The frame rate is determined by start-of-frame, end-of-frame signaling and allows handling the input sources with different frame rates per channel.

For more details, see the *Camera Subsystem* section in the *Peripherals* chapter of the device-specific TRM.

7.10 Termination of Unused Peripherals and I/Os

All power pins must be supplied with the supply voltages specified in *Recommended Operating Conditions* section, unless otherwise specified.

AM62A7/AM62A3 has pins (package balls) that have specific connectivity requirements and package balls that can be unused.

For information on terminating the unused peripherals and I/Os, see the *Pin Connectivity Requirements* section of the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

7.10.1 EXTINTn

EXTINTn is a dedicated, fail-safe interrupt pin and is recommended to be terminated when connected externally or a PCB trace is connected.

8 I/O Buffers and Termination

An important step in the hardware design, before beginning schematic capture, is to confirm both DC and AC electrical compatibility between the processor and attached external devices.

- The device-specific data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, run IBIS simulations using IBIS models provided for the processor to confirm signal integrity.
  - AM62Ax IBIS Model

For more information on terminations, see the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

9 Power Consumption and Thermal Solutions

The Processor power consumption depends on application, features implemented, temperature, architecture, design topology, and temperature/process variations.

9.1 Power Consumption

For information on the device power consumption, see *AM62A Power Estimation Tool*.

9.2 Power Savings Modes

The device supports multiple power saving modes. For more details, see the *Power Modes* section in the *Device Configuration* chapter of the device-specific TRM.

9.3 Guidance on Thermal Solution

The *Thermal Design Guide for DSP and Arm Application Processors* application report provides guidance for successful implementation of a thermal solution for board designs containing this device. This document provides information on common terms and methods related to thermal solutions. TI only supports designs that follow board design guidelines contained in the application report.

For more information, see AM62Ax Thermal Model.

10 Schematics Recommendations

At this stage of the design, schematic capture can be started. To support the schematics capture, see the sections below.

10.1 Selection of Component and Component Values

Be sure to use the device-specific data sheet recommended values when selecting the passive components as applicable.

10.2 Schematics Development

The schematics can be drawn newly or EVM schematics can be reused during the schematics capture phase, see the *Starter Kit SK-AM62A-LP EVM* schematic.

The below link summarizes the considerations designers have to be familiar when reusing TI EVM design files for designing custom board.

[FAQ] AM62A7 or AM62A3 Custom board hardware design - Reusing TI EVM design files.

During schematic capture, follow *Schematic Design and Review Checklist* and *AM62Ax Sitara Errata*.

Note

When EVM schematics is reused, ensure the functionality and change in net name are reviewed before reuse.

When schematics is reused, the DNI setting are reset. Make sure the DNIs are reconfigured (populating DNIs could affect the functionality).

10.3 Reviewing the Schematics

After completing the schematic capture, check the design against the *Starter Kit SK-AM62A-LP EVM*.

Plan an internal schematic review to review the schematics with reference to the schematic checklist. Check circuit implementation for errors, value or connection inaccuracies, missing net connections, and so forth.

10.4 Floor Planning of the PCB

After schematic capture, TI recommends floor planning of the board to determine the interconnect distances between the various devices, board size and outline.

11 Layout and Routing Guidelines

After completing schematic capture and reviews, the next design step is the PCB layout. For information supporting the board layout, see the following section.

11.1 Escape Routing Guidelines

The *AM62Ax Escape Routing PCB Design* application report provides a sample PCB escape routing for the AM62A7/AM62A3 processor.

11.2 LPDDR4 Board Design and Layout Guidelines

The goal of the *AM62Ax DDR Board Design and Layout Guidelines* is to make the LPDDR4 system implementation simpler for all designers. Requirements have been captured as a set of layout and routing guidelines that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using LPDDR4 memories that follow the guidelines in this document.

LPDDR4 target impedance is 40-ohm (single-ended) and 80-ohm (differential) on the LPDDR4 traces.

For the propagation delay, the delay to be considered for LPDDR4 is the delay related to the traces on the board. There is no need to include any package level propagation delay.

Ffor LPDDR4 SDRAM Count, Channel Width, Number of Channels, Number of Die, Number of Ranks, see the DDR board design guide.

Note

Data bit swizzle and byte swap is supported in the AM62A7/AM62A3 devices.

Note

DDR4, DDR3 or DDR2 are not supported in the AM62A7/AM62A3 devices.

11.3 High-Speed Differential Signal Routing Guidance

The *High-Speed Interface Layout Guidelines* provides guidance for successful routing of the high-speed differential signals. This includes PCB stack-up and materials guidance as well as routing skew, length, and spacing limits. TI supports only designs that follow the board design guidelines contained in the application report.

Note

Consider using the *Starter Kit SK-AM62A-LP EVM* layout as reference.

12 Device Handling and Assembly

Recommended reviewing the device thickness information, ball pitch, Lead finish/Ball material and the recommended MSL rating/Peak reflow to be followed.

For more information, see *MSL Ratings and Reflow Profiles* and *Moisture sensitivity level search*.

13 References

- Texas Instruments: *AM62Ax Sitara™ Processors Data Sheet*
- Texas Instruments: *AM62Ax Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM62Ax Silicon Errata*
- Starter Kit SK-AM62A-LP EVM
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- XDS Target Connection Guide
- Texas Instruments: *AM62A Power Estimation Tool*
- Texas Instruments: *AM62Ax Escape Routing PCB Design Application note*
- Texas Instruments: *AM62Ax DDR Board Design and Layout Guidelines*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *MSL Ratings and Reflow Profiles*
- Moisture sensitivity level search
- Texas Instruments: *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design*
- Texas Instruments: *Jacinto™ 7 DDRSS Register Configuration Tool*

14 Acronyms Used in This Document

CAN – Controller Area Network

CAN-FD – Controller Area Network Flexible Data-Rate

CPSW3G – Common Platform Ethernet Switch 3-port Gigabit

CSIRX – Camera Streaming Interface Receiver

DPI – Display Parallel Interface

E2E – Engineer to Engineer

eCAP – enhanced Capture

ECC – Error-Correcting Code

eMMC – embedded Multi-Media Card

EMU – Emulation Control

ePWM – enhanced Pulse-Width Modulator

eQEP – enhanced Quadrature Encoder Pulse

GEMAC – Gigabit Ethernet Media Access Controller

GPIO – General Purpose Input/Output

GPMC – General-Purpose Memory Controller

HS-RTDX – High Speed Real Time Data eXchange

I2C – Inter-Integrated Circuit Interface

IBIS – Input/Output Buffer Information Specification

JTAG – Joint Test Action Group

LDO – Low Dropout

LVCMOS – Low voltage complementary metal oxide semiconductor

LVDS – Low Voltage Differential Signaling

MAC – Media Access Controller

McASP – Multichannel Audio Serial Ports

MDIO – Management Data Input/Output

MMC – Multi-Media Card

MSL – Moisture Sensitivity Level

OSPI – Octal Serial Peripheral Interface

PCB – Printed Circuit Board

PMIC – Power management integrated circuit

POR – Power-on Reset

QSPI – Quad Serial Peripheral Interface

RGMII – Reduced Gigabit Media Independent Interface

RMII – Reduced Media Independent Interface

SD – Secure Digital

SDIO – Secure Digital Input Output

SPI – Serial Peripheral Interface

TCK – JTAG Test Clock Input

TDI – JTAG Test Data Input

TDO – JTAG Test Data Output

TMS – JTAG Test Mode Select Input

TRM – Technical Reference Manual

TRSTn – JTAG Reset

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

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