Application Note

AM62A Power Estimation Tool

ABSTRACT

The power estimation spreadsheet provides power consumption estimates based on measured and simulated data; they are provided “as is” and are not guaranteed within a specified precision. Power consumption depends on electrical parameters, silicon process variations, environmental conditions, and use cases running on the processor during operation. Actual power consumption should be verified in the real system. This tool is meant for estimating power consumption during realistic operating modes; it is not intended for power supply sizing. This power estimation spreadsheet is preliminary and subject to change. The spreadsheet mentioned in this document can be downloaded from here.

Table of Contents

Trademarks

1 Using the Power Estimation Tool

The input part of the spreadsheet consists of six sections: Operating Performance Point, Processor Core Utilization, LVCMOS IO, Peripheral, Estimated Power, and General. To use the input part the spreadsheet, users must modify the fields with their appropriate usage parameters. Cells designed for user input are in blue. Fields that cannot be modified are red. Fields in green are the output calculated power. Configure the blue cells to a value most closely aligned with your intended scenario.

The purpose of each of the four sections is:

- Operating Performance Point: Configure frequency of operation for A53s, R5s, M4, C7x DSP, VPAC, VPU, and HSM.
- Processor Core Utilization: User estimated percent utilization of each core.
- LVCMOS IO: Subset of commonly used IO with selectable mode and percent utilization.
- Peripherals: Other peripherals with selectable mode and percent utilization.
- General: High level system configuration.
- Estimated Power: Power estimation output by rail. Power rails are aligned with EVM design. Selectable VDD_CORE.

1.1 Operating Performance Point (OPP)

This section allows the user to set the operating frequency of each of the compute cores and clusters.

- A53: Bypass to 1400 MHz, depending on PLL resolution frequency step.

Note

If using 1400 MHz, VDD_CORE should be set to 0.85 V, per the data sheet.

- MCU R5F: Bypass to 800 MHz, depending on PLL resolution frequency step.
- Device Manager R5F: 400 or 800 MHz, depending on PLL resolution frequency step.
- M4F: 400 or 800 MHz, depending on PLL resolution frequency step.
- C7x: Bypass to 1000 MHz

Note

If using 1000 MHz, VDD_CORE should be set to 0.85 V, per the data sheet.

- HSM: 133 or 400 MHz
- VPAC: 187.5 or 375 MHz
- VPU: 100, 200, or 400 MHz

1.2 Processor Core Utilization

This section lets the user load each compute core with utilization between 0%-100% (inclusive). For guidance, 0% is an “off” or “unused” state. 1% is “idle”. 100% is maximum utilization (i.e. Dhrystone).

For the C7x DSP there is no mode to toggle MMA usage or not. Because of this we recommend if MMA is not used then the valid range of %Utilization is 0 to 50%. For example, if the customer intends to model 100% activity without MMA usage, then 50% is the appropriate value. When MMA of the DSP is used, the valid range is 0 to 100%.

1.3 LVCMOS IO

This section allows the user to select both Mode and Utilization of a subset of commonly used IOs on the AM62A, including UART (3.3 V), SPI (3.3 V), Ethernet (3.3 V), OSPI (1.8 V), and GPMC (3.3 V).

Note

This is not the complete set of IOs possible on the AM62A, and any IO configuration must be confirmed through the AM62A pinmux tool. These are dual voltage IO domains (1.8 V or 3.3 V), but currently are fixed to match the EVM design.

- Mode: IO dependent mode and operating speed.
- Utilization (%): Specifies the utilization as a percentage of activity relative to a full load condition.

1.4 Peripherals

This section allows the user to select both Mode and Utilization of the other peripherals on the AM62A. Other peripherals include DDR, USB2, SD card, eMMC, CSI and CANFD.

- Mode: Peripheral dependent operating mode.
- Utilization (%): Specifies the utilization as a percentage of activity relative to a full load condition.

1.5 General

This section lets the user select junction temperature (not ambient temperature) and power estimation mode.

- Junction Temperature (°C): -40 to 125 approximate junction temperature
- Power Estimation Mode: Typ or Max ('Typ' is the typical power consumption of most devices. 'Max' is the worst-case possible due to silicon variation).

1.6 Estimated Power Consumption

The power estimation tool generates a power analysis report in this section. There is a selectable field for the two modes of operation of VDD_CORE. The report lists power supply name, voltage in Volts (V), and power consumption in Watts (mW) per power rail groups. Power rail groups match the AM62A EVM design.

Note

The VDD_DDR4 estimated power is from AM62A SOC only, on the EVM this rail includes both SOC and external DDR device power. The total power consumption in Watts (mW) is listed at the end of the table.

VDD_CORE: 0.75 V or 0.85 V for AM62A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265