

TPS65910x Schematic Checklist

Version B

Application Report



Literature Number: SWCA139B
April 2012–Revised September 2012

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TPS65910x Schematic Checklist

ABSTRACT

This application note for TPS65910x, a power companion device for application processors (see the device data sheet) lists the connection details for each pin. The ball details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each ball on a system schematic.

In addition to this list, customers are advised to use the information in the data sheet, (TI literature number [SWCS046](#)).

NOTE: Customer must ensure that the power-up sequence for the application processor is met. This document does not cover the details of the power-up sequence for TPS65910 or the application processor. Refer to the device data sheet and the reference designs for the application processors for the correct power-up sequence requirements.

1 Recommended Operating Conditions

Parameter	Test Conditions	Min	Nom	Max	Unit
V_{CC} : Input voltage range on pins/balls VCC1, VCC2, VCCIO, VCC3, VCC4, VCC5, VCC7 ⁽¹⁾⁽²⁾		2.7	3.6	5.5	V
V_{CCP} : Input voltage range on pins/balls VCC6		1.7	3.6	5.5	V
Input voltage range on pins/balls VDDIO ⁽³⁾		1.65	1.8/3.3	3.45	V
Input voltage range on pins/balls PWRON		0	3.6	5.5	V
Input voltage range on pins/balls SDA_SDI, SCL_SCK, SDASR_EN2, SCLSR_EN1, SLEEP		1.65	VDDIO	3.45	V
Input voltage range on pins/balls PWRHOLD, GPIO_CKSYNC		1.65	VDDIO	5.5	V
Input voltage range on balls BOOT1, BOOT0, OSC32KIN		1.65	VRTC	1.95	V

⁽¹⁾ VCC7 should be connected to the highest supply that is connected to the device VCCx pin. The exception is that VCC2 and VCC4 can be higher than VCC7.

⁽²⁾ VCC2 and VCC4 must be connected together (to the same voltage).

⁽³⁾ If VDD3 boost is used, VAUX33 must be set to 2.8 V or higher and enabled before VDD3.

2 TPS65910x Schematic Checklist

Table 1. TPS65910x Schematic Checklist

Name	BGA Pin	Type	I/O ⁽¹⁾	Description	Recommended Connection ⁽²⁾	Not Used Features
PWRHOLD	1	Digital	I	Switch on, switch off control signal, mode defined in EEPROM	Switch-on, switch-off mode: Can be connected to an external signal for PMIC power-up/power-down control or If control is not required, then can be tied to VRTC	Floating (internal pulldown active by default)
VMMC	2	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	Floating
VCC3	3	Power	I	VMMC and VAUX33 power input	Connect to VBAT with a 4.7- μ F capacitor	Connected to VCCs
VAUX33	4	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	Floating
VDIG2	5	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	Floating
VCC6	6	Power	I	VDIG1 and VDIG2 power input	Connect to VBAT with a 4.7- μ F capacitor. Needs external input or preregulated output from TPS65910x	Connected to VCCs
VDIG1	7	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	Floating
SDA_SDI	8	Digital	I/O	I ² C bidirectional data signal/serial peripheral interface data input (multiplexed)	External 1.2-k pullup to I/O supply	N/A
SCL_SCK	9	Digital	I/O	I ² C bidirectional clock signal/serial peripheral interface clock input (multiplexed)	External 1.2-k pullup to I/O supply	N/A
SDASR/EN2	10	Digital	I/O	Enable for supplies/voltage scaling dedicated I ² C data	Processor I ² C for SmartReflex™ control with external pullup to VIO or connected to GPIO for DC-DC/LDO control; external 1.2-k pullup to I/O supply	Floating
SCLSR/EN1	11	Digital	I/O	Enable for supplies/voltage scaling dedicated I ² C clock	Processor I ² C for SmartReflex control with external pullup to VIO or connected to GPIO for DC-DC/LDO control; external 1.2-k pullup to I/O supply	Floating
VDDIO	12	Power	I	Digital I/Os supply	Connect to system I/O supply: an external I/O supply or I/O supply provided by TPS65910x (usually VIO).	N/A
VCCIO	13	Power	I	VIO DC-DC power Input	Connect to VBAT with a 10- μ F capacitor	Connected to VCCs
SWIO	14	Power	O	VIO DC-DC switched output	Connected to a 2.2- μ H inductor and a 10- μ F capacitor to ground	Floating
GNDIO	15	Power	I/O	VIO DC-DC power ground	GND	GND
VFBI0	16	Analog	I	VIO feedback voltage	Connected to a 2.2- μ H inductor (other node that is away from the device)	GND or floating (internal pulldown)

⁽¹⁾ I = Input; O = Output; OD = Open Drain

⁽²⁾ VBAT is the battery or any input source other than preregulation. The maximum level is 5.5 V.

Table 1. TPS65910x Schematic Checklist (continued)

Name	BGA Pin	Type	I/O ⁽¹⁾	Description	Recommended Connection ⁽²⁾	Not Used Features
REFGND	17	Analog	I/O	Reference ground	Connect to AGND (clean ground), same as 32K crystal GND	N/A
VREF	18	Analog	O	Bandgap voltage	Connect to 0.1- μ F capacitor to REFGND. Capacitor close to device	N/A
BOOT1	19	Digital	I	Power-up sequence selection	Connect to VRTC for the EEPROM boot up sequence	N/A
OSC32KIN	20	Analog	I	32-kHz crystal oscillator	Depending on EEPROM configuration: – If RC oscillator, then OSC32KIN: grounded – If crystal oscillator, then crystal oscillator connected to OSC32KIN – If bypass clock, then OSC32KIN: input	N/A
OSC32KOUT	21	Analog	I	32-kHz Crystal oscillator	Depending on EEPROM configuration: – If RC oscillator, then OSC32KOUT: floating – If crystal oscillator, then crystal oscillator connected to OSC32KOUT – If bypass clock, then OSC32KOUT: floating	N/A
VDAC	22	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	Floating
VCC5	23	Power	I	VDAC and VPLL power input	Connect to VBAT with a 4.7- μ F capacitor	Connected to VCCs
VPLL	24	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	Floating
TESTV	25	Analog	O	Analog test output (DFT)	Floating	Floating
BOOT0	26	Digital	I	Digital I Power-up sequence selection	Connect to GND for the EEPROM boot up	N/A
VBACKUP	27	Power	I	Backup battery input	Backup battery - supercap or rechargeable coin cell; $C_{BB} = 10$ mF	Connected to VCC7
VCC7	28	Power	I	VRTC power input and analog references supply	VBAT (5.5-V maximum) or other preregulated supply. Must be first supply provided for TPS65910x. Connect to a 4.7- μ F filter capacitor	N/A
VRRTC	29	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	N/A
VFB3	30	Analog	I	VDD3 feedback voltage	Connect to an LED and to a 10- μ F capacitor to GND. See page 2 of the datasheet.	GND
SW3	31	Power	O	VDD3 DC-DC switched output	Connect to a LED and to a 4.7- μ H inductor to VBAT and use a 4.7- μ F input capacitor. See page 2 of the datasheet.	Floating
VFB1	32	Analog	I	VDD1 feedback voltage	Connected to a 2.2- μ H inductor (other node that is away from the device)	GND or floating (internal pulldown)
PWRON	33	Digital	I	External switch-on control (on button)	Push-button. PWRON transition low will power up PMIC	Floating (internal pullup active by default)
GND1	34	Power	I/O	VDD1 DC-DC power ground	GND	GND
SW1	35	Power	O	VDD1 DC-DC switched output	Connected to a 2.2- μ H inductor and a 10- μ F capacitor to ground	Floating

Table 1. TPS65910x Schematic Checklist (continued)

Name	BGA Pin	Type	I/O ⁽¹⁾	Description	Recommended Connection ⁽²⁾	Not Used Features
VCC1	36	Power	I	VDD1 DC-DC power input	Connect to VBAT with a 10- μ F capacitor	Connected to VCCs
SLEEP	37	Digital	I	ACTIVE-to-SLEEP state transition control signal	Connected to processor control pin (that is, GPIO or any other low-power mode control pin). The polarity of SLEEP signal is set in DEVCTRL2_REG.SLEEPSIG_POL.	GND or floating
CLK32KOUT	38	Digital	O	32-kHz clock output	To processor 32K clock input	Floating
GPIO_CKSYNC	39	Digital	I/O	Configurable general-purpose I/O or DC-DCs synchronization clock input signal	GPIO (GPI with PU set by default) or DC-DCs synchronization clock input	Floating
NRESPWRON	40	Digital	O	Power off reset	Connect to reset input of the processor or any other similar function to show device power up is complete	N/A
VCC2	41	Power	I	VDD2 DC-DC power input	Connect to VBAT with a 10- μ F capacitor	Connected to VCCs
SW2	42	Power	O	VDD2 DC-DC switched output	Connected to a 2.2- μ H inductor and a 10- μ F capacitor to ground	Floating
GND2	43	Power	I/O	VDD2 DC-DC power ground	GND	GND
VFB2	44	Analog	I	VDD2 DC-DC feedback voltage	Connected to a 2.2- μ H inductor (other node that is away from the device)	GND or floating (internal pulldown)
INT1	45	Digital	O	Interrupt flag	Connect to the processor interrupt pin or a GPIO (optional)	Floating
VAUX1	46	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	Floating
VCC4	47	Power	I	VAUX1 and VAUX2 power input	Connect to VBAT with a 4.7- μ F capacitor	GND if VAUX1 and VAUX2 are not used
VAUX2	48	Power	O	LDO regulator output	Connect to a 2.2- μ F filter capacitor	Floating

3 Revision History

The following table summarizes the TPS65910x Schematic Checklist versions.

Note: Numbering may vary from previous versions.

Version	Literature Number	Date	Notes
*	SWCA139	April 2012	See ⁽¹⁾
A	SWCA139A	May 2012	See ⁽²⁾
B	SWCA139B	September 2012	See ⁽³⁾

⁽¹⁾ TPS65910x Schematic Checklist, (SWCA139) - initial release.

⁽²⁾ TPS65910x Schematic Checklist, (SWCA139A) -

- Update [Table 1](#) - Update OSC32KIN and OSC32KOUT Recommended Connection and Not Used Features

⁽³⁾ TPS65910x Schematic Checklist, (SWCA139B) -

- Update [Table 1](#) - Update VBACKUP: Replace Connected to VCC5 by Connected to VCC7

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