

## CC2430 to CC2530 Migration Guide

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### Keywords

- 2.4 GHz IEEE 802.15.4 systems
- ZigBee® systems
- RemoTI systems
- CC2430, CC2431
- CC2530, CC2531

## 1 Introduction

The CC2530 is TI's second generation ZigBee® / IEEE 802.15.4 RF SoC for the 2.4 GHz unlicensed ISM band. This chip enables industrial grade applications by offering state-of-the-art selectivity/co-existence, an excellent link budget, and low voltage operation.

Changes from the CC2430 to the CC2530 can be categorized into the following categories:

- Tools and EVM changes

- Pinout / Layout changes
- Added features
- Changed modules/features

This document describes the functional changes per module.

For detailed features, performance and functionality of the CC2430 and the CC2530, the user is referred to the respective datasheets/user guides ([1], [2], [3]).

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## 2 Abbreviations

CSP	Command Strobe Processor
DMA	Direct Memory Access
EVM	Evaluation Module
EVM	Error Vector Magnitude
GPIO	General Purpose Input Output
ISM	Industrial, Scientific, Medical
LNA	Low Noise Amplifier
MAC	Medium Access Control
PA	Power Amplifier
PCB	Printed Circuit Board
RF	Radio Frequency
RX	Receive, Receive Mode
SoC	System-on-Chip
SPI	Serial Peripheral Interface
TX	Transmit, Transmit Mode
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter

## 3 Features and Performance Comparison

The CC2530 represents a significant improvement on the CC2430 in terms of program memory sizes, package size and RF performance as can be seen in Table 1.

**Table 1 - Features and Performance Comparison**

Metric	CC2430	CC2530
<b>Features</b>		
MCU	8051 compatible	8051 compatible
Flash	Up to 128K	Up to 256KB
RAM	8K (<4K during PM2/3)	8KB in all PMs
Clock loss detection	No	Yes
Timer 1 Channels	3	5
MAC timer Size	16-bit, 20-bit overflow	16-bit, 24-bit overflow
Core Freq	32 MHz	32 MHz
Package	7 x 7, 48 pin	6 x 6, 40 pin
Operating Temperature	-40 to +85	-40 to +125
<b>Radio Performance</b>		
Sensitivity (dBm)	-92	-97
Max Tx Power (dBm)	0	+4.5
Link Budget (dB)	92	101.5
EVM at max output power	11%	2%
adjacent -5 MHz	30	49
adjacent +5 MHz	41	49
alternate -10 MHz	53	57
alternate +10 MHz	55	57
<b>Low Power</b>		
Operating Voltage	2.0-3.6 V	2.0-3.6 V
Rx Current	27 mA	24 mA
Tx Current (0 dBm)	27 mA	29 mA
Tx Current (+4.5 dBm)	NA	34 mA
CPU active current (32 MHz)	10.5 mA	6.5 mA
PM1 current	190 uA	200 uA
PM2 current	0.5 uA	1 uA
PM3 current	0.3 uA	0.4 uA
PM1 -> Active	4 us	4 us
PM2/3 -> Active	0.1ms	0.1 ms
Xtal startup time	0.5 ms	0.3 ms

## 4 Tools and EVM

The CC2530 is fully supported by the SmartRF05 tools platform, while the CC2430 is fully supported by the SmartRF04 platform. The CC2530 can also be supported by the SmartRF04EB boards that were shipped with the CC2430, but a firmware upgrade is necessary and not all functionality will be available. Software stacks and examples are not built for the SmartRF04EB board. Older SmartRF05EB boards may need a firmware upgrade to recognize the CC2530.

Although most peripheral registers have the same functionality in the CC2530 as they do in the CC2430, most register addresses have changed and a new definitions (.h) file is used for the CC2530. Current IAR releases support the CC2530 with all necessary header files and drivers.

## 5 Layout Considerations and Antennas

The reference designs for CC2430 are not valid for the CC2530 due to the pin-out and RF changes. New reference designs have been made for the CC2530 and are available on the CC2530 product page on <http://www.ti.com/>.

The antennas for CC2430 are not directly compatible with the CC2530, especially the differential ones. New antenna recommendations will be made for CC2530 with very similar antennas to what is recommended for CC2430. Please see the CC2530 product folder on [www.ti.com](http://www.ti.com) for antenna recommendations and reference designs.

## 6 Top Level and Pinout

The CC2530 comes in a 6x6mm QFN40 package, while the CC2430 comes in a 7x7 QFN48 package.

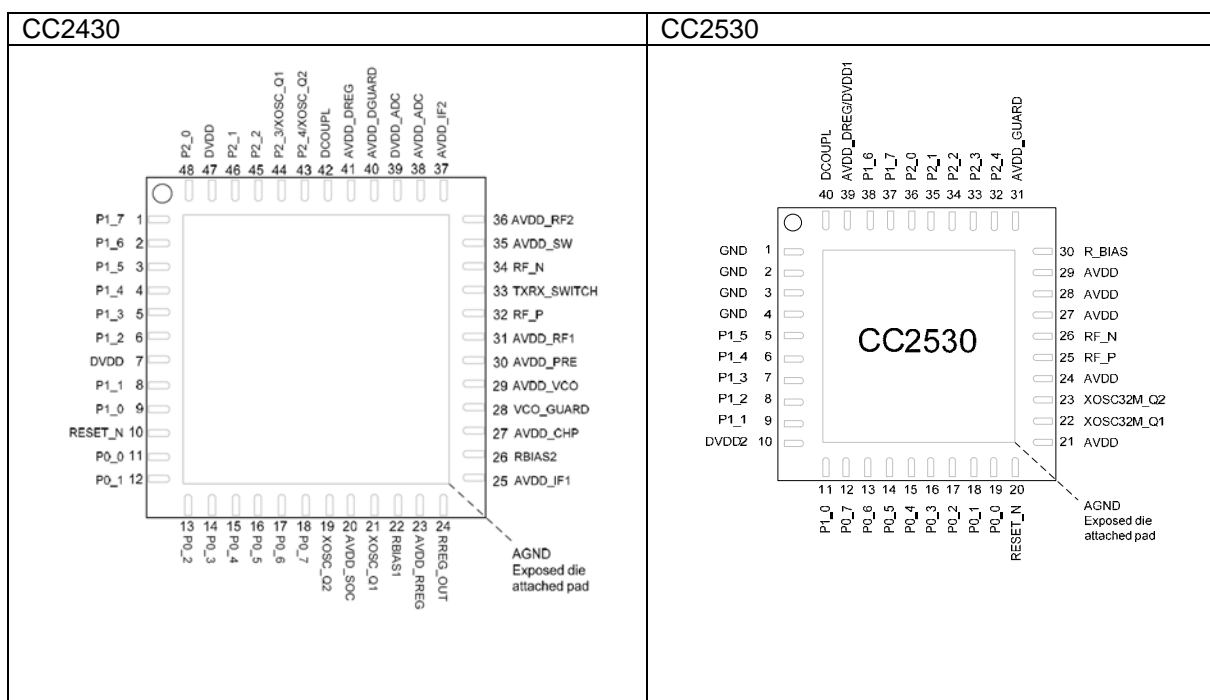


Figure 1 - CC2430 and CC2530 Pinouts

It is important to note in particular the changes to the RF side of the chip. To a large extent, the digital ports have been kept facing in the same direction to require minimal PCB layout changes to upgrade.

All digital pins have the internal pull-up resistor enabled during reset on CC2530 whereas on the CC2430, only the debug clock had pull-up during reset.

Hysteresis has been added to the GPIO and reset pads to ensure more robust inputs.

Note that the CC2530 does not have a dedicated TXRX\_SWITCH pin as on the CC2430. Control of external PA/LNA solutions like the CC2590/1 is done by configuring pins from P1[5:0] to output control signals directly from the radio. See the "Radio Test Output Signals" section of the "I/O Ports" chapter in [2] for details.

## 7 Flash Controller

### 7.1 Flash Write Change

On the CC2530, it is no longer necessary to set a FWT (flash write timing) register as hardware automatically adjusts its timing depending on the clock source. On CC2530 one has to start the writing process and then write data to the register (the other way around was possible on CC2430).

### 7.2 Information page change

The information page is not writable from the debug interface on the CC2530. The information page contains lock information for information page and configuration/calibration data from production test. This data includes and IEEE address that can be used by MAC software. Please see [2] for details. The flash lock bits that protect the flash from inadvertently being written in-system are on the CC2530 located in the highest normal flash page. There is one lock bit per 2KB page for improved granularity of locking.

## 7.3 Bank registers

The memory maps on the CC2530 are slightly changed from the CC2430 to accommodate the larger memory sizes better. This primarily affects the FMAP and MEMCTR registers.

## 7.4 Code prefetch

To accommodate larger flash sizes the flash read latency has increased by one clock cycle. To compensate for that, a prefetch mechanism has been added which enables zero wait-states flash reads for sequentially executing code. See the "Flash Controller" chapter in [2].

## 8 Observability signals

The CC2530 contains an observability mux that is used to amongst other things implement a promiscuous mode packet sniffer.

## 9 Watchdog Timer

In CC2430 the watchdog timer had different behavior in different power modes. In CC2530, the watchdog timer is reset in power modes.

## 10 Clock Loss Detector

A clock loss detector has been added to enable compliance with regulations that require resilience against clock frequency deviations and clock loss.

## 11 New RADIO

The radio in CC2530 is based mainly on the CC2520 radio while the radio in the CC2430 was based on the CC2420 radio. Certain features are recognizable from the CC2430 such as the CSP while the packet filtering functionality has been greatly improved. The transmitter chain is the same as in the CC2520 while the TX chain is new. This means that compared to the CC2430, most of the radio registers have changed.

## 12 Sleep Timer

In the CC2530 it is possible to capture the sleep timer when an I/O event occurs. There is also a change to the way the sleep timer registers should be accessed. Updating and reading of sleep timer registers must be timed differently than on the CC2430.

## 13 Timer 1 channels

The number of channels has been increased to 5 on Timer 1 (the 16-bit timer).

## 14 GPIO

All GPIOs on CC2530 have individual interrupt enable bits. This means that it can be decided which pins in a port should generate a port interrupt to the CPU.

## 15 Timer 2

Timer 2 has been changed to add longer timers and more compare registers.

## 16 Debug Interface

A DBGDATA register has been added and made writable directly through the debug interface to allow burst writes using the DMA. This enables very efficient production programming of the CC2530. The debug interface on the CC2530 must be clocked 8 times before a result is ready for clocking out as opposed to a simple wait period on the CC2430. Debugging of PM2/3 is supported on the CC2530 at the cost of not being able to debug idle mode.

## 17 DMA

On the CC2530, the timing of the DMA transfers has changed, and there is now one clock cycle added latency for starting a transfer. The variable length VLEN=010 option is on CC2530 limited to only do single transfers. On the CC2530, there is a new DMA trigger that enables burst write for DBGDATA during production programming.

## 18 System controller

The registers in the system controller of the CC2530 have been changed to a command/status structure. This makes changing clock sources and speeds simpler in software. The only aspect that needs to be handled in software when entering power modes is that the PCON.IDLE=1 instruction should be aligned such that a flash read is not started on the last clock cycle. See the "Power-Management Control" section of chapter "Power Management and Clocks" in [2].

## 19 32 kHz RCOSC Cal

The 32 kHz RC oscillator calibration is not done continuously on the CC2530 but only once after the 32 MHz clock is turned on. To initiate further calibration, it suffices to switch quickly back to the 16 MHz RCOSC and back to the 32 MHz XOSC again.

## 20 USART

The CC2530 implements UART parity differently than on the CC2430. The CC2530 does not support 9-bit data transfers. The SPI slave select signal (SSN) is edge detected on CC2430 while it is level detected on CC2530.

## 21 References

- [1] CC2530 Datasheet ([SWRS081](#))
- [2] CC253x User Guide ([SWRU191](#))
- [3] CC2430 Datasheet ([SWRS036](#))

## 22 General Information

### 22.1 Document History

Revision	Date	Description/Changes
SWRA287	2009.04.29	Initial release.

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