FEC Decoding

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Keywords

- FEC
- Trellis
- Viterbi
- CC1100
- CC1100E
- CC1101
- CC1110Fx
- CC1111Fx
- CC1110
- CC1150
- CC2500
- CC2510Fx
- CC2550
- CC430Fx

1 Introduction

The CC1100, CC1100E, CC1101, CC1110Fx, CC1111Fx, CC1150, CC2500, CC2510Fx, CC2511Fx, and CC2550 all implement FEC encoding and decoding in HW. The purpose of this design note is to describe how one can implement the same FEC decoding in SW. This is in particular very important for the CC430Fx device, which has the same radio as the CC1101 and CC1110/11Fx but without HW FEC included. This design note is not meant as a tutorial on FEC and it will not cover the FEC encoding, as it is described in DN504 [1].
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2 Abbreviations

CRC  Cyclic Redundancy Check
FEC  Forward Error Correction
FIFO  First In First Out
HW  Hardware
LSB  Least Significant Bit
MSB  Most Significant Bit
RAM  Random Access Memory
SW  Software
3 Implementation

3.1 Code Example Assumptions and Limitations

Assume that you want to use the CC1101 [5] to transmit a packet and the CC430Fx [2] to receive it. The payload is 29 bytes and 2 bytes of CRC are appended. If FEC is enabled (MDMCFG1.FEC_EN = 1) on the transmitter, 64 bytes will be transmitted over the air in addition to preamble and sync word. Due to the appended trellis terminator and the size of the interleaving buffer the packet length will always be a multiple of 4 after encoding (see DN504 [1]). The number of bytes sent over the air (not including preamble and sync word) can be calculated as shown in Equation 1.

\[
\text{# of Bytes on the Air} = \left(\frac{\text{Payload Length} + 2 \text{ Bytes Optional CRC}}{2}\right) \times 4
\]

The code example shown in Section 3.2 does not show how to set up the CC430Fx to receive a packet and it does not show how to implement the function (readRxFifo) that will read from the RXFIFO in Figure 5 (see the CC430Fx User’s Guide [2] on how this can be done). It is assumed that a flag, packetReceived, is asserted when the packet is received and the 64 bytes are in the RXFIFO. It is important to notice that there is no packet size limitation to the FEC decoding itself, but if more than 64 bytes are sent over the air, the receiver must start to read the RXFIFO before the complete packet is received and additional RAM is needed to store the un-coded packet. When 64 bytes or less is sent on the air, the un-coded data can simply be kept in the RXFIFO until being decoded. The CC1101 [5] only support fixed packet length mode (PKTCTRL0.LENGTH_CONFIG = 0) when FEC is enabled, so the CC430Fx should also use this mode. Overflow of the RXFIFO will therefore not be an issue as long as the maximum packet length is less than 64 bytes (PKTLEN <= 0x40).

If the receiver is not the CC430Fx but some other radio which do not have an RXFIFO, it will be necessary to store the receive packet in a temporary buffer and then the function readRxFifo should read from this buffer instead of from the RXFIFO. It is assumed that the bytes in this buffer are read in the same order as they would have been read from a traditional FIFO.

1 The division is a “whole number” division; i.e., all variables are of type unsigned short
3.2 C Code

The C code in this section is organized as follows: Figure 1; Function Prototypes, Global Variables, and Defines, Figure 2; Function Definitions, Figure 3 and Figure 4; FEC Decoder Implementation, and Figure 5; main.

```c
/*************************************************************
* FUNCTION PROTOTYPES
*/
unsigned short fecDecode(unsigned char *pDecData, unsigned char *pInData, unsigned short RemBytes);
static unsigned char hammWeight(unsigned char a);
static unsigned char min(unsigned char a, unsigned char b);
static unsigned short calcCRC(unsigned char crcData, unsigned short crcReg);

/******************************
* GLOBAL VARIABLES
*/
// The payload + CRC are 31 bytes. This way the complete packet to be received will fit in the RXFIFO
unsigned char rxBuffer[4]; // Buffer used to hold data read from the RXFIFO (4 bytes are read at a time)
unsigned char rxPacket[31]; // Data + CRC after being interleaved and decoded

// Look-up source state index when:
//                     Destination state --\ /-- Each of two possible source states
const unsigned char aTrellisSourceStateLut[8][2] =
{ {0, 4}, // State {0,4} -> State 0
  {0, 4}, // State {0,4} -> State 1
  {1, 5}, // State {1,5} -> State 2
  {1, 5}, // State {1,5} -> State 3
  {1, 5}, // State {1,5} -> State 4
  {2, 6}, // State {2,6} -> State 5
  {2, 6}, // State {2,6} -> State 6
  {2, 6}, // State {2,6} -> State 7
};

// Look-up expected output when:
//                     Destination state --\ /-- Each of two possible source states
const unsigned char aTrellisTransitionOutput[8][2] =
{ {0, 3}, // State {0,4} -> State 0 produces "00", "11"
  {3, 0}, // State {0,4} -> State 1 produces "11", "00"
  {2, 1}, // State {1,5} -> State 2 produces "01", "10"
  {2, 1}, // State {1,5} -> State 3 produces "10", "01"
  {0, 3}, // State {2,6} -> State 4 produces "00", "11"
  {1, 2}, // State {2,6} -> State 5 produces "11", "00"
  {1, 2}, // State {2,6} -> State 6 produces "10", "01"
  {1, 2}, // State {2,6} -> State 7 produces "01", "10"
};

// Look-up input bit at encoder when:
//                     Destination state --\ /-- Each of two possible source states
const unsigned char aTrellisTransitionInput[8] =
{ 0,
  1,
  0,
  1,
  0,
  1,
  0,
  1,
};

/******************************
* DEFINES
*/
// NUMBER_OF_BYTES_AFTER_DECODING should be given the length of the payload + CRC (CRC is optional)
#define NUMBER_OF_BYTES_AFTER_DECODING 31
#define NUMBER_OF_BYTES_BEFORE_DECODING (4 * (NUMBER_OF_BYTES_AFTER_DECODING / 2) + 1))
```

Figure 1. Function Prototypes, Global Variables, and Defines
/* @fn hammWeight
 * @brief Calculates Hamming weight of byte (# bits set)
 * @param a - Byte to find the Hamming weight for
 * @return Hamming weight (# of bits set in a)
 */
static unsigned char hammWeight(unsigned char a)
{
    a = ((a & 0xAA) >> 1) + (a & 0x55);
    a = ((a & 0xCC) >> 2) + (a & 0x33);
    a = ((a & 0xF0) >> 4) + (a & 0x0F);
    return a;
}

/* @fn min
 * @brief Returns the minimum of two values
 * @param a - Value 1
 *          b - Value 2
 * @return Minimum of two values
 *          Value 1 (Value 1 < Value 2)
 *          Value 2 (Value 2 < Value 1)
 */
static unsigned char min(unsigned char a, unsigned char b)
{
    return (a <= b ? a : b);
}

/* @fn calcCRC
 * @brief Calculates a checksum over n data bytes
 * Example of usage
 * checksum = 0xFFFF;
 * for (i = 0; i < n; i++)
 *    checksum = calcCRC(dataBytes[i], checksum);
 * @param crcData - checksum (initially set to 0xFFFF)
 *              crcReg - data byte
 * @return Checksum
 */
static unsigned short calcCRC(unsigned char crcData, unsigned short crcReg)
{
    unsigned char i;
    for (i = 0; i < 8; i++) {
        if (((crcReg & 0x8000) >> 8) ^ (crcData & 0x80))
            crcReg = (crcReg << 1) ^ 0x8005;
        else
            crcReg = (crcReg << 1);
        crcData <<= 1;
    }
    return crcReg;
}
Figure 3. FEC Decoder Implementation (1)
void

/main (void)

unsigned short checksum;
unsigned short nBytes;
unsigned char *pDecData = rxPacket; // Destination for decoded data
// Init MCU and Radio
while (1) {
    // Wait for packet to be received (64 bytes in the RXFIFO)
    packetReceived = 0;
pDecData = rxPacket;
    // Perform de-interleaving and decoding (both done in the same function)
    fecDecode(NULL, NULL, 0); // The function needs to be called with a NULL pointer for initialization before every packet to decode
    nbytes = NUMBER_OF_BYTES_AFTER_DECODING;
    while (nbytes > 0) {
        unsigned short nByteOut;
        nByteOut = fecDecode(pDecData, rxBuffer, nbytes);
        nByteOut += nByteOut;
        pDecData += nByteOut;
    }
    // Perform CRC check (Optional)
    unsigned short i;
    nbytes = NUMBER_OF_BYTES_AFTER_DECODING;
    checksum = 0xFFFF;
    for (i = 0; i < nbytes; i++)
        checksum = calcCRC(rxPacket[i], checksum);
    if (!checksum) {
        // Do something to indicate that the CRC is OK
    }
}
4 Explanation to the Code

The most important part of the code is the decoder part implemented in the function *fecDecode* (see Figure 3 and Figure 4). The function will process 4 and 4 bytes of received data since this is the data size the interleaver works on. This means that in most cases the function will be called several times for each received packet. The pseudo code for the function is shown in Figure 6.

```plaintext
fecDecode() {
    // Variable Declaration
    // Initialize variables at start of packet (and return without doing any more)
    // De-interleave 4 bytes of received data (4 bytes of data means 16 (2b) encode symbols
    // For all 16 symbols do one iteration of Viterbi decoding
    for (nIterations = 16; nIterations > 0; nIterations--) {
        // Get 2b input symbol [MSB first] and do one iteration of Viterbi decoding
        // For each destination state in the trellis
        for (iDestState = 0; iDestState < 8; iDestState++) {
            // Calculate cost of transition from each of the two source states (cost is Hamming difference between
            // received 2b symbol and expected symbol for transition)
            // Select transition that gives lowest cost in destination state, copy that source state's path and add
            // new decoded bit
            nPathBits++;
        }
        // If trellis history is sufficiently long, output a byte of decoded data. After 32 iterations
        // (nPathBits == 32) the 8 MSB bits will be the same for all 8 surviving paths and a byte can be output
        // After having processed 3-symbol trellis terminator, flush out remaining data
        // Swap current and last buffers for next iteration
    }
    // Normalize costs so that minimum cost becomes 0
}
```

**Figure 6. Pseudo Code for the FEC Encoder**

The “key” elements of the code are the two for loops that for every symbol goes through each destination state in the trellis. An example is used to illustrate what is going on in this loop.

Example: A packet consisting of 5 bytes (0x01, 0x02, 0x03, 0x04, 0x05) is being interleaved and encoded by the CC1101 (*MDMCFG1.FEC_EN* = 1). The data transmitted on the air will be the following (preamble and sync word is not shown):

0x4C, 0xF0, 0x30, 0x10, 0xC8, 0x7C, 0xC3, 0x23, 0x40, 0x34, 0x7C, 0xE3 (see DN504 [1])

In chunks of 4 and 4 bytes, this data will on the receiver side be interleaved, giving the symbols shown in Table 1 to be decoded (only the 4 first bytes are shown):

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<th>Symbol #</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
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<th>13</th>
<th>14</th>
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<th>16</th>
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<tr>
<td>Symbol</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>11</td>
<td>01</td>
<td>11</td>
<td>11</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>11</td>
<td>01</td>
<td></td>
</tr>
<tr>
<td>Byte</td>
<td>0x00</td>
<td>0x03</td>
<td>0x7C</td>
<td>0x0D</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Table 1. Symbols to be Encoded**
Figure 7. Trellis 1 (the number in () indicates the source state of that given cost)

For each received symbol (2b), all possible encoder output symbols (00, 01, 10, and 11) in Figure 7 are compared against the received symbol and a transition cost is calculated (nCost0 and nCost1). The appropriate transition cost is added to the accumulated path cost of each path that terminates in the source state on the left in the figure. It can be seen that there are two transitions into each destination state on the right in the figure. For each destination state the incoming transition with the lowest accumulated path cost is selected (the survivor path) and the other one thrown away - nothing is lost as all future paths that go through this state at this point in the trellis would do the same selection. Thus the number of paths that the Viterbi Algorithm tracks is always constant and the optimal path is always one of them.
Figure 8. Trellis 2

Figure 9. $nCost$ and $aPath$ after 1st iteration (received symbol: $00_b$)
Figure 10. Trellis 3

Figure 11. nCost and aPath after 2\textsuperscript{nd} Iteration (received symbol: 00\textsubscript{b})
iCurrBuf = 1
iLastBuf = 0
nCost[iCurrBuf][] = [0, 2, 3, 3, 5, 3, 4, 4]
aPath[iCurrBuf][iDestState] = (aPath[iLastBuf][iSrcState] << 1) | nInputBit;
aPath[1][0] = (aPath[0][0] << 1) | Input to state 0 = 00000000000000000000000000000000
aPath[1][1] = (aPath[0][0] << 1) | Input to state 1 = 00000000000000000000000000000001
aPath[1][2] = (aPath[0][1] << 1) | Input to state 2 = 00000000000000000000000000000010
aPath[1][3] = (aPath[0][1] << 1) | Input to state 3 = 00000000000000000000000000000011
aPath[1][4] = (aPath[0][2] << 1) | Input to state 4 = 00000000000000000000000000000100
aPath[1][5] = (aPath[0][2] << 1) | Input to state 5 = 000000000000000000000000000000101
aPath[1][6] = (aPath[0][3] << 1) | Input to state 6 = 000000000000000000000000000000110
aPath[1][7] = (aPath[0][3] << 1) | Input to state 7 = 000000000000000000000000000000111

Figure 13. nCost and aPath after 3rd Iteration (received symbol: 00b)
iCurrBuf = 0
iLastBuf = 1
nCost[iCurrBuf][] = [0, 2, 3, 3, 4, 3, 4, 4]

aPath[iCurrBuf][iDestState] = aPath[iLastBuf][iSrcState] << 1 | nInputBit;

iCurrBuf = 0
iLastBuf = 1
nCost[iCurrBuf][] = [0, 2, 3, 3, 4, 3, 4, 4]

aPath[iCurrBuf][iDestState] = aPath[iLastBuf][iSrcState] << 1 | nInputBit;

Figure 14. Trellis 5

Figure 15. nCost and aPath after 4th Iteration (received symbol: 00b)
iCurrBuf = 1
iLastBuf = 0
nCost[iCurrBuf][] = [0, 2, 3, 3, 4, 3, 4, 4]

aPath[iCurrBuf][iDestState] = (aPath[iLastBuf][iSrcState] << 1) | nInputBit;
aPath[1][0] = aPath[0][0] << 1 | Input to state 0 = 00000000000000000000000000000000
aPath[1][1] = aPath[0][0] << 1 | Input to state 1 = 00000000000000000000000000000001
aPath[1][2] = aPath[0][1] << 1 | Input to state 2 = 00000000000000000000000000000010
aPath[1][3] = aPath[0][1] << 1 | Input to state 3 = 00000000000000000000000000000011
aPath[1][4] = aPath[0][6] << 1 | Input to state 4 = 00000000000000000000000000001100
aPath[1][5] = aPath[0][2] << 1 | Input to state 5 = 00000000000000000000000000000101
aPath[1][6] = aPath[0][3] << 1 | Input to state 6 = 00000000000000000000000000000110
aPath[1][7] = aPath[0][3] << 1 | Input to state 7 = 00000000000000000000000000000111

Figure 16. Trellis 6

Figure 17. nCost and aPath after 5th Iteration (received symbol: 00b)
After having processed 32 symbol, the 8 MSBs of \textit{aPath}[0][0] \ (0000001_b) is copied to \textit{rxFifo[0]}. 

\begin{verbatim}
\begin{array}{l}
aPath[iCurrBuf][iDestState] = (aPath[iLastBuf][iSrcState] << 1) | nInputBit;
\hline
aPath[0][0] = 00000010000001000000000000000000
aPath[0][1] = 00000010000001100000000000000000
aPath[0][2] = 00000010000001100000000000000000
aPath[0][3] = 00000010000001100000000000000000
aPath[0][4] = 00000010000001100000000000000000
aPath[0][5] = 00000010000001100000000000000000
aPath[0][6] = 00000010000001100000000000000000
aPath[0][7] = 00000010000001100000000000000000
\end{array}
\end{verbatim}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{path.png}
\caption{\textit{aPath} after having Processed 32 Symbols}
\end{figure}

After 8 more symbols, \textit{aPath[iCurrBuf][iDestState]} looks like in Figure 19 and 00000010_b (8 MSBs of \textit{aPath[0][0]}) are copied to \textit{rxFifo[1]}. 

\begin{verbatim}
\begin{array}{l}
aPath[iCurrBuf][iDestState] = (aPath[iLastBuf][iSrcState] << 1) | nInputBit;
\hline
aPath[0][0] = 00000010000001000000000000000000
aPath[0][1] = 00000010000001100000000000000000
aPath[0][2] = 00000010000001100000000000000000
aPath[0][3] = 00000010000001100000000000000000
aPath[0][4] = 00000010000001100000000000000000
aPath[0][5] = 00000010000001100000000000000000
aPath[0][6] = 00000010000001100000000000000000
aPath[0][7] = 00000010000001100000000000000000
\end{array}
\end{verbatim}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{path.png}
\caption{\textit{aPath} after having Processed 40 Symbols}
\end{figure}

After having processed 3 more symbols, the trellis terminator has been processed and the remaining bytes of the packet are being copied to \textit{rxFifo}. 

\begin{verbatim}
rxFifo[2] = aPath[1][0] bit 26:19 = 00000011_b
rxFifo[3] = aPath[1][0] bit 18:11 = 00000100_b
rxFifo[4] = aPath[1][0] bit 10:3  = 00000101_b
\end{verbatim}

\begin{verbatim}
\begin{array}{l}
aPath[iCurrBuf][iDestState] = (aPath[iLastBuf][iSrcState] << 1) | nInputBit;
\hline
aPath[1][0] = 00010000001100000000000000000000
aPath[1][1] = 00010000001100000000000000000000
aPath[1][2] = 00010000001100000000000000000000
aPath[1][3] = 00010000001100000000000000000000
aPath[1][4] = 00010000001100000000000000000000
aPath[1][5] = 00010000001100000000000000000000
aPath[1][6] = 00010000001100000000000000000000
aPath[1][7] = 00010000001100000000000000000000
\end{array}
\end{verbatim}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{path.png}
\caption{\textit{aPath} after having Processed 43 Symbols}
\end{figure}
5 References

[1] DN504 FEC Implementation (swra113.pdf)
[4] CC1100E Low-Power Sub-GHz RF Transceiver (470-510 MHz & 950-960 MHz) (CC1100E.pdf)
[6] CC1110Fx/CC1111Fx Low-Power Sub-1 GHz RF System-on-Chip (SoC) with MCU, Memory, Transceiver, and USB Controller (cc1110f32.pdf)
[9] CC2510Fx/CC2511Fx Low-Power SoC (System-on-Chip) with MCU, Memory, 2.4 GHz RF Transceiver, and USB Controller (cc2510f32.pdf)
[10] CC2550 Low-Cost Low-Power 2.4 GHz RF Transmitter (cc2550.pdf)
6 General Information

6.1 Document History

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<th>Revision</th>
<th>Date</th>
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<td>SWRA313</td>
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<td>Initial release.</td>
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