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Thermal Derating Curves for Logic-Products Packages

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Thermal Derating Curves for Logic-Products Packages

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Abstract

Thermal metrics, such as θ_{JA} and θ_{JC}, are used to compare thermal performance of plastic integrated circuit (IC) packages. The thermal conductivity of all materials of the IC packaging and of the test board affect the thermal resistance values reported by semiconductor manufacturers. Recent advancements in reporting thermal data include standard test-board designs. Texas Instruments (TI™) has published values for all logic-products IC packages. Also, derating curves that allow calculation of the maximum power dissipation of a plastic IC package have been developed. The derating curves, which are available on a TI web page, can be modified interactively to determine maximum power dissipation with different ambient-temperature ranges and junction temperatures.

Introduction

The maximum allowable power consumption of an IC package can be calculated, given the thermal resistance of the package, the junction temperature, and the ambient temperature. This calculation of maximum power using thermal resistance values with different airflows makes possible the generation of derating curves. These derating curves allow the system designer to see the effect of ambient-temperature changes on the maximum power that the package can dissipate. The system designer can also use this type of thermal data to compare performance of packages from different suppliers, assuming the same test-board conditions.

Thermal data and derating curves for TI logic-products IC packages have been published on a TI web page discussed in *Application to Semiconductor Packaging*. The user can vary the junction temperature and ambient-temperature range used to calculate the derating curves for each package as described in *Derating Curves.*

Background

Semiconductor users need to know the thermal performance of IC packages to be used in their end equipment. Knowing the thermal performance of the IC package for a given device allows the system designer to determine the maximum power that the package can handle. However, it is critical that the user of any thermal data know the test conditions under which the thermal data was generated.

Many thermal metrics exist for IC packages. These include thermal resistance of the package measured from junction to ambient (θ_{JA}) and measured from junction to case (θ_{JC}). A simple analogy can be used to define these terms before applying them to semiconductor packages.

The Concept

Consider a closed cup of heated coffee at a certain temperature (see Figure 1). The temperature of the coffee is analogous to the junction temperature (T_J) of a semicondutor device. The outer surface of the coffee cup is at some temperature analogous to the temperature of the outside of the semiconductor package, or case temperature, (T_C). Finally, the room is at ambient, or free-air, temperature (T_A). Clearly, $T_J > T_C > T_A$.

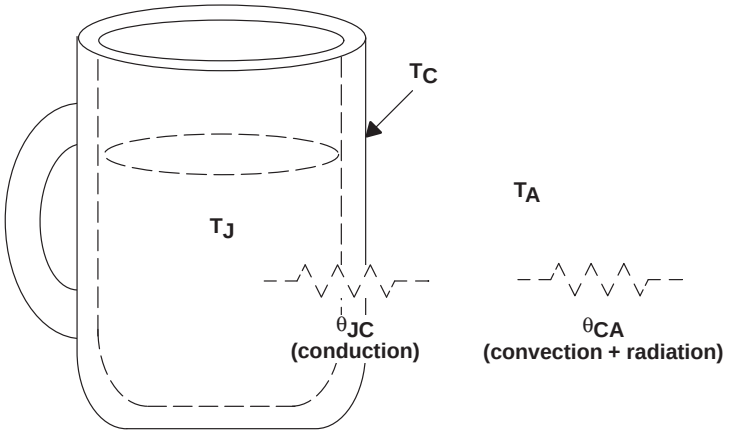

Figure 1. Coffee-Cup Example for Thermal Metrics

Heat transfers from the coffee through the cup by conduction. Thus, there is a temperature differential between the coffee and the outer surface. The rate of heat transfer through the cup is determined by the thermal resistance of the walls of the cup. The thermal resistance is a function of the material used to make the cup (e.g., paper, Styrofoam™, or porcelain), the thickness of the walls of the cup, and the overall geometry of the cup. The higher the thermal resistance, the slower the heat travels through the cup. The thermal resistance between the junction (the coffee) and the case (cup) can be designated θ_{JC}.

Moving away from the junction, heat then transfers from the surface of the cup by radiation and convection. There is a thermal resistance associated with this transfer that is expected to be a function of the geometry, smoothness, and color of the surface. This thermal-resistance value is termed θ_{CA}.

The overall rate of heat transfer is then a combination of θ_{JC} and θ_{CA}. There is a temperature drop (much like a voltage drop) from the inner side to the outer side of the cup and another drop from the surface of the cup to the ambient environment. Of course, the objective is to keep coffee warm. But, with semiconductors, the objective is to move heat away from the IC chip as quickly as possible.[1]

Application to Semiconductor Packaging

Figure 2 shows a typical IC plastic package with the silicon chip and the thermal metrics identified.

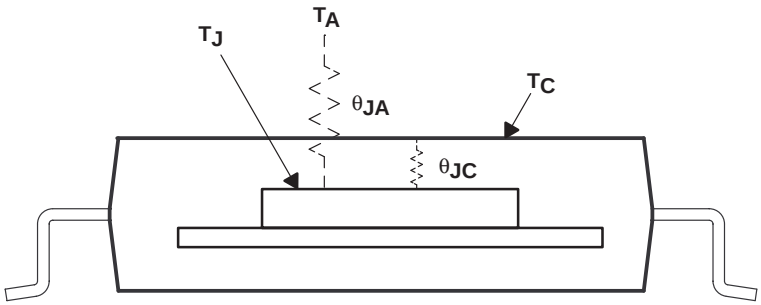

Figure 2. IC Package Thermal Metrics

Styrofoam is a trademark of Dow Chemical Company.

For semiconductor devices, the junction-to-ambient thermal resistance (θ_{JA}) is the most commonly used thermal metric and is defined mathematically in Equation 1.

$$\theta_{JA} = \left(T_J - T_A\right) / P \quad \textbf{(1)}$$

Where:
T_J = junction temperature of the chip
T_A = ambient temperature
P = power to the chip

Thermal resistance is the resistance of the package to heat dissipation and is related inversely to the thermal conductivity of the package. Of course, the source of heat in an IC package is the chip. All electrical circuits dissipate some amount of power in the form of heat, which is conducted through the package to the ambient environment. Because the process is not 100% efficient, the temperature of the die (T_J) rises above ambient. The thermal conductivity of the silicon chip, die-attach epoxy, copper leadframe, and mold compound all affect the rate at which the heat is dissipated. The geometries of the package and of the printed circuit board (PCB) greatly influence how quickly the heat sinks into the PCB and away from the chip.

To eliminate the test-board design as a variable in data reported between IC manufacturers, thermal-test-board design standards have been developed and released.[2,3] The primary factors in these test-board designs are shown in Table 1.

Table 1. Critical PCB Design Factors for JEDEC 1s and 2s2p Test Boards

DESIGN FACTORS	THERMAL TEST-BOARD DESIGNS	
	JEDEC 1s (Low-K) (inches)	JEDEC 2s2p (High-K) (inches)
Trace thickness	0.0028	0.0028
Trace length	0.98	0.98
PCB thickness	0.062	0.062
PCB width	4	4
PCB length	4.5	4.5
Power/ground-plane thickness	No internal copper planes	0.0014 (2 planes)

When reviewing thermal data supplied by the IC manufacturer, it is critical that users know the details of the PCB design in Table 1 to accurately compare data from different suppliers.

In 1996, TI's Logic Products group published θ_{JA} values for its IC packages. The data published in 1996 was generated using a JEDEC 1s PCB design. Thermal data is either generated in a laboratory environment or arrived at from thermal models of the PCB and IC package. The thermal model program used by TI is ThermCAL, a proprietary finite-difference thermal-modeling tool. The thermal data for SLL packages is available on the TI external web page:

http://www.ti.com/sc/docs/asl/package/thermal.htm

The Thermal Comprehensive Data Table on this web page lists the θ_{JA} data for each package at airflows of 0, 150, 250, and 500 linear feet per minute (lfm). Pertinent information about leadframe pad size and die size is listed for each package. Also, the source of the data (laboratory measurements or model) is indicated. Model data has been verified to be accurate within ±10% of laboratory measurements.

Derating Curves

When a device reaches a state of thermal equilibrium, the electrical power delivered is equal to the thermal heat dissipated. This thermal energy is in the form of heat and is given off to the surroundings. The maximum allowable power consumption (P) at a given ambient temperature (T_A) is computed using the maximum junction temperature for the chip (T_J) and the thermal resistance of the package (θ_{JA}) (see Equation 2).

$$P = \left(T_J - T_A\right) / \theta_{JA} \quad \textbf{(2)}$$

Over time, heat destroys semiconductors. Thus, manufacturers usually specifiy a maximum junction temperature [$T_{J(max)}$]. If the junction temperature goes above this value, irreversible damage occurs. Because the IC user typically knows the ambient temperature of the operating environment (T_A), the thermal resistance of the IC package (θ_{JA}) provided by the supplier, and a specified maximum junction temperature, Equation 2 can be used to determine the maximum power that can be applied to the particular package under the specified test conditions.

In Equation 2, by varying the ambient temperature at a given airflow, a derating curve can be developed for each package. By using the thermal resistance value of the package at different airflows, a derating curve can be developed for each airflow. A typical set of derating curves for the 16-pin SOIC (DW) package is shown in Figure 3. The data for the 16-pin SOIC (DW) package (θ_{JA}) used to calculate the curves was generated using a JEDEC 1s PCB design.

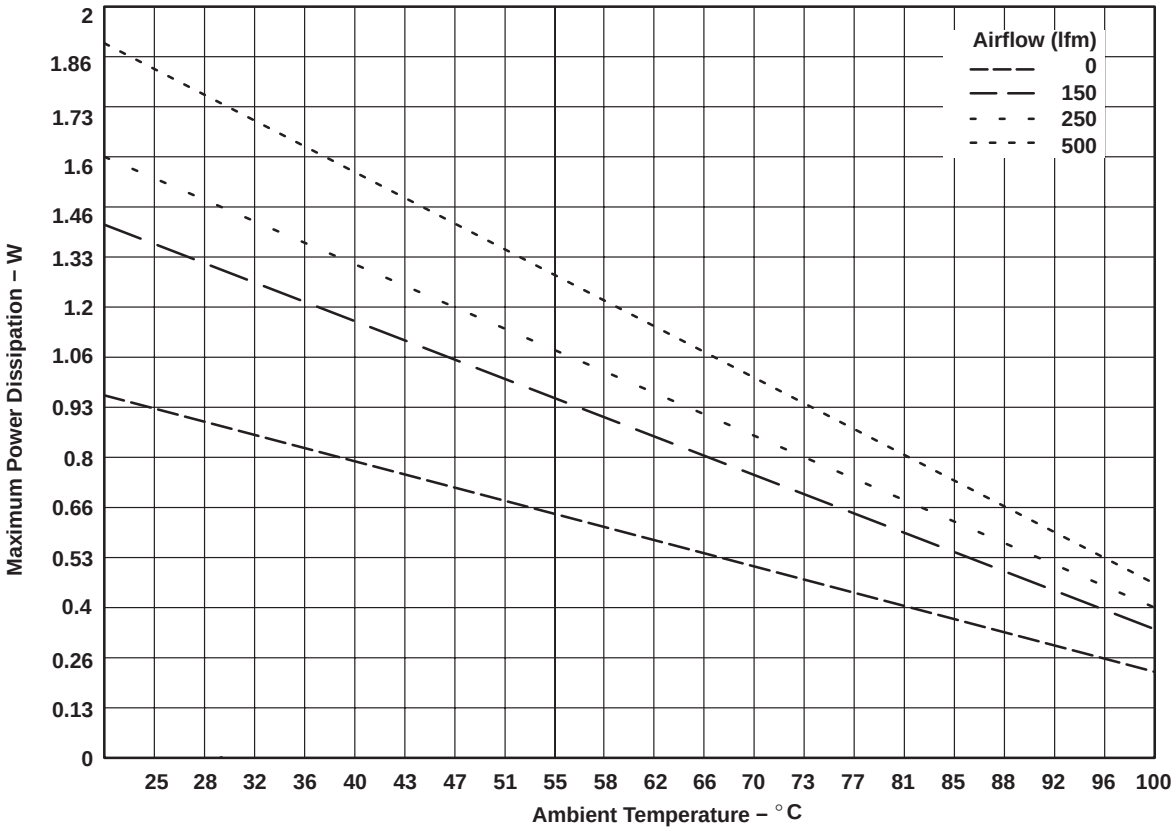

Figure 3. Derating Curves for 16-Pin SOIC (DW) Package

As an example, the 16-pin SOIC (DW) package has a θ_{JA} value of 104.6°C/W at 0-lfm airflow. The maximum power that the package can withstand at T_A = 25°C and T_J = 125°C, remembering that the θ_{JA} value was derived using a JEDEC 1s PCB, is:

$$P = (125°C - 25°C) / (104.6°C/W) = 0.956 W$$

For a given package, these derating curves allow the designer to see the effect of rising ambient temperature on the maximum power allowed. The derating curves for each package can be viewed on the TI web page mentioned previously. The program uses the θ_{JA} data shown to display the maximum power dissipation (y-axis) of the package over a range of ambient temperatures (x-axis). This maximum power dissipation of the package is equivalent to the maximum allowable consumption of the IC device. The user can vary the junction temperature and the ambient-temperature range used in the interactive calculation of maximum power dissipation.

The user is reminded that the system θ_{JA} is usually significantly different than the two quoted JEDEC θ_{JA}s which are based on the high effective thermal conductivity and low effective thermal conductivity test cards. In an actual system, many characteristics impact the junction temperatures. A few are listed here:

(1) The temperature profile of neighboring components interact through the PCB.

(2) Power dissipation up wind of the component of interest can heat the localized ambient.

(3) The area of the PCB impacts it heat sinking efficiency.

(4) Subtle design features of the PCB, such as power and ground plane isolations, can modify thermal conduction in the PCB.

The user is strongly encouraged to use system-level thermal modeling tools to determine system junction temperatures. JEDEC θ_{JA} values are for comparison of relative power-dissipation capabilities of packages, not for system junction temperature estimation. [4][5]

Conclusion

Integrated-circuit designers and end users need to compare the thermal performance of plastic IC packages. The most commonly used thermal metrics are package thermal resistance measured either from junction to ambient (θ_{JA}) or junction to case (θ_{JC}). Once the thermal resistance of the package is determined, it is possible to calculate the maximum power that a package can take at an assumed junction temperature and ambient temperature. By calculating the maximum power dissipation a package can withstand at a number of different ambient temperatures, derating curves can be developed for each package. These curves allow the user to see graphically the maximum power dissipation for a given package over a range of conditions. The web-based derating curves allow the user to vary the junction temperature and the ambient-temperature range used to calculate the curves.

Acknowledgment

The authors of this application report are Douglas W. Romm and Jeffrey D. Pfeifle.

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