

This document can handle board shapes up to 7.9in x 10in, although our panel vendors top out at 7in x 10in.

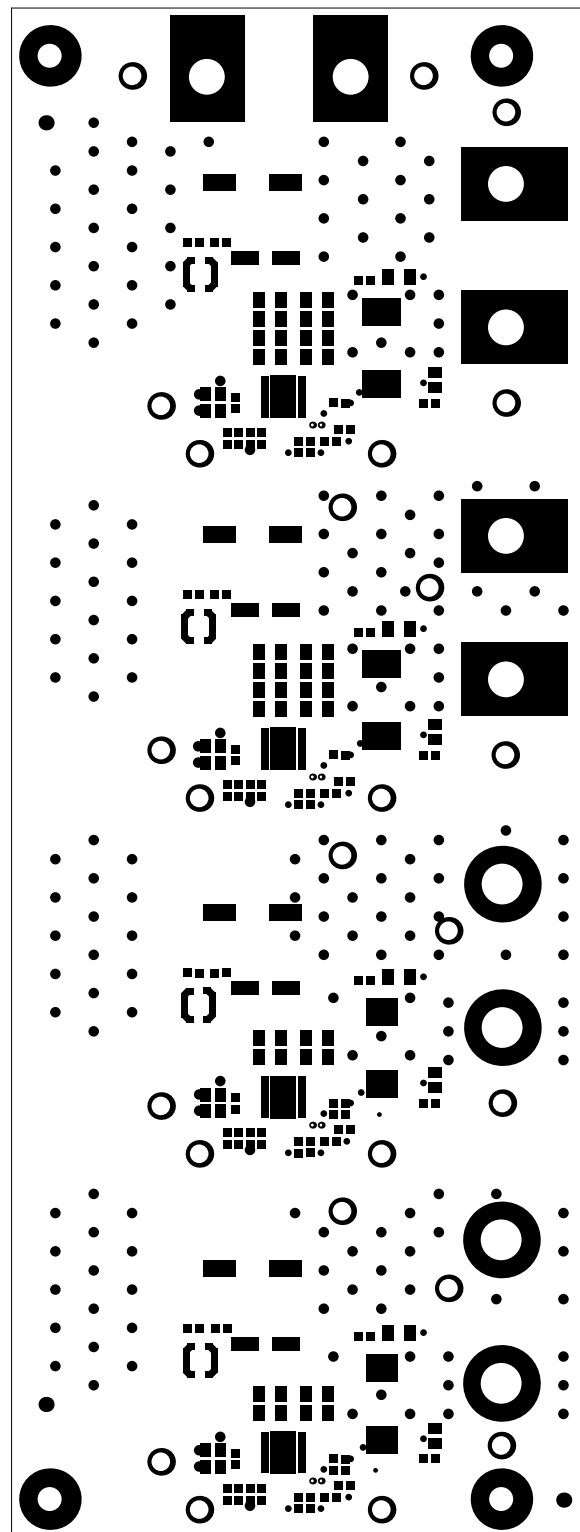
To re-size the board shape, do the following:

- Select lines on MI Board Outline and delete
- Draw a rectangle using lines (example will be for a 4 x 6 board)
- Enter Place line mode (keyboard pl)
- keyboard jo to jump to origin, hit enter
- keyboard j1 to jump to location, set x to 6000, hit enter twice
- keyboard j1 to jump to location, set x to 6000 and y to 4000, hit enter twice
- keyboard j1 to jump to location, set x to 0 and y to 4000, hit enter twice
- keyboard jo to jump to origin, hit enter
- Hit ESC twice to exit place line mode
- Select all on MI Board Outline (keyboard sy)
- Menu DesignBoard ShapeDefine from Selected Objects (keyboard dsd)
- With MI tracks still selected, copy them and use the origin as reference (keyboard jo)
- Select the Keep-Out Layer, and Paste Special (keyboard ea)
- Paste on the Keep-Out Layer using origin again (keyboard jo)
- Don't forget to delete these strings

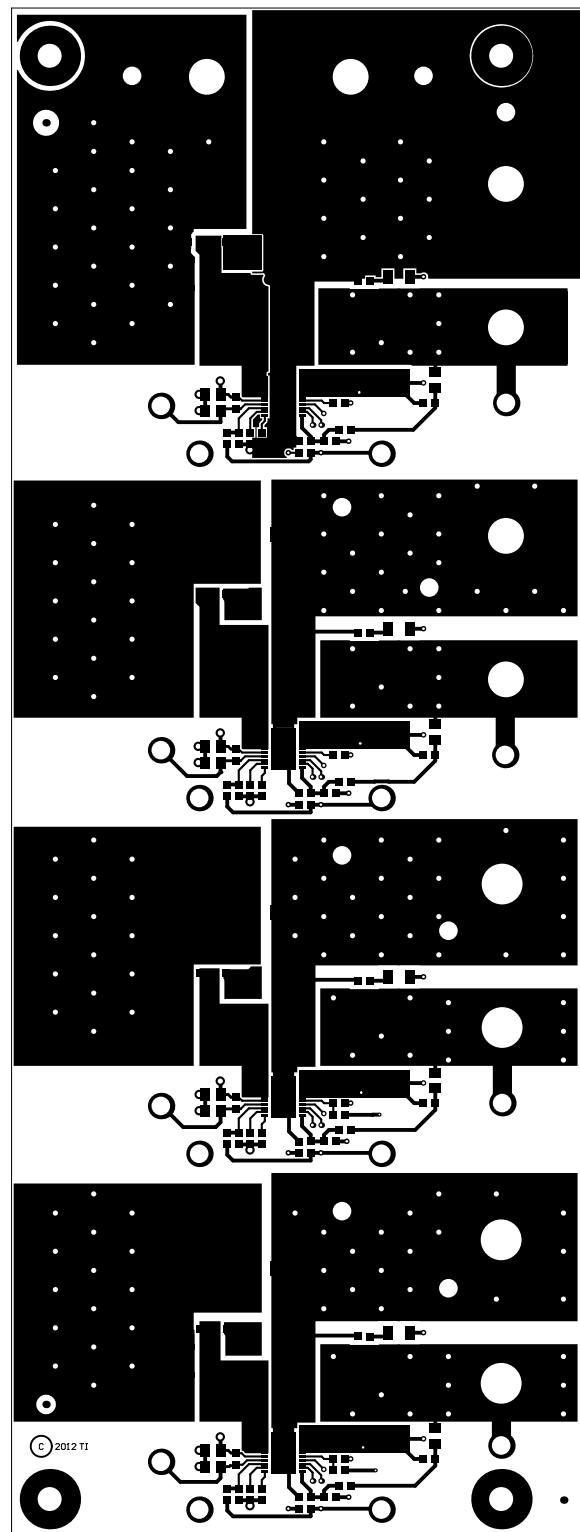
Keep the mounting holes 200 mil from board edge if you re-size the board

If you re-size the board, don't forget to move the drill table strings on Drill Drawing Layer  
...they should be just to the right of your board shape

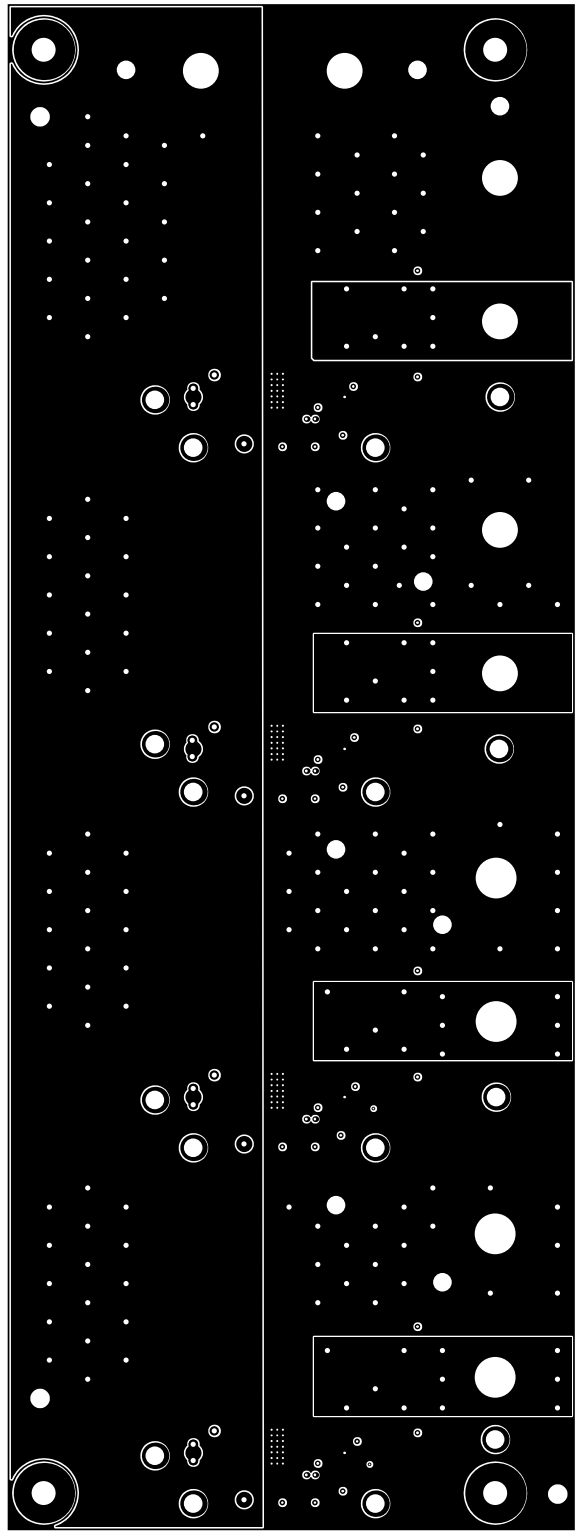
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7828 REVA	
LAYER NAME = Top Overlay	ARTWORK # = 880007828-001 REV A	NATIONAL SEMICONDUCTOR
PLOT NAME = Top Overlay	GENERATED : 6/14/2012	3:11:10 PM

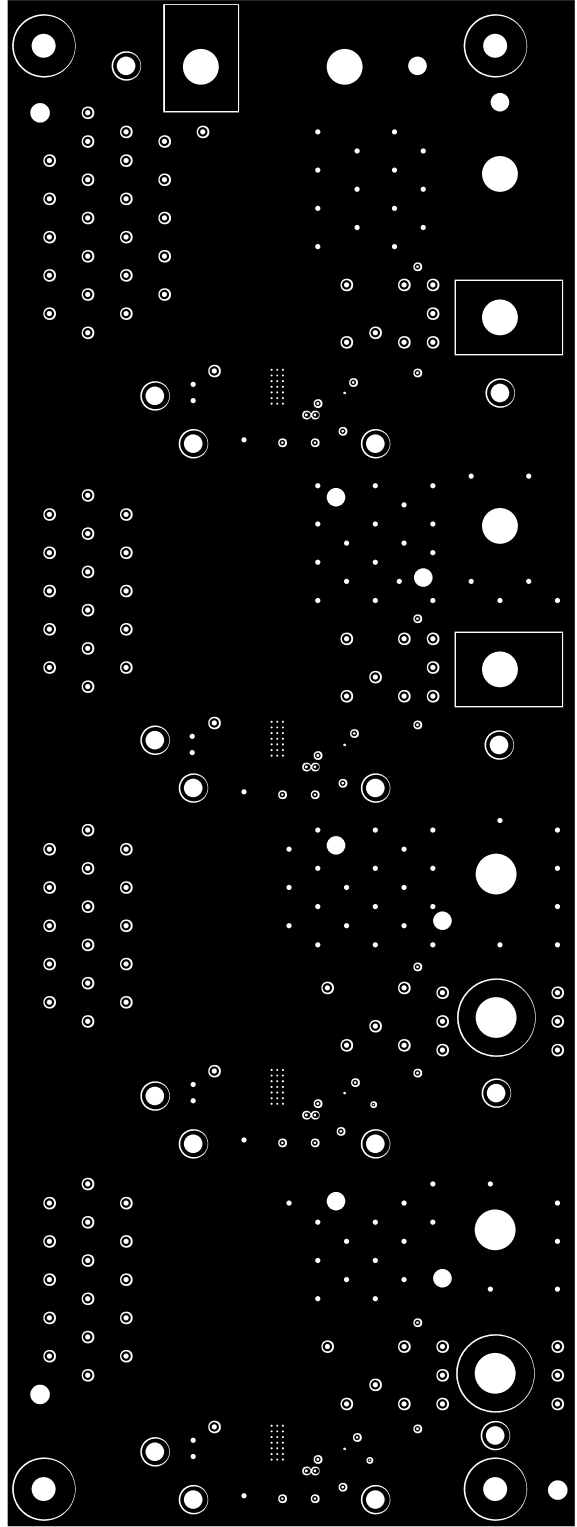


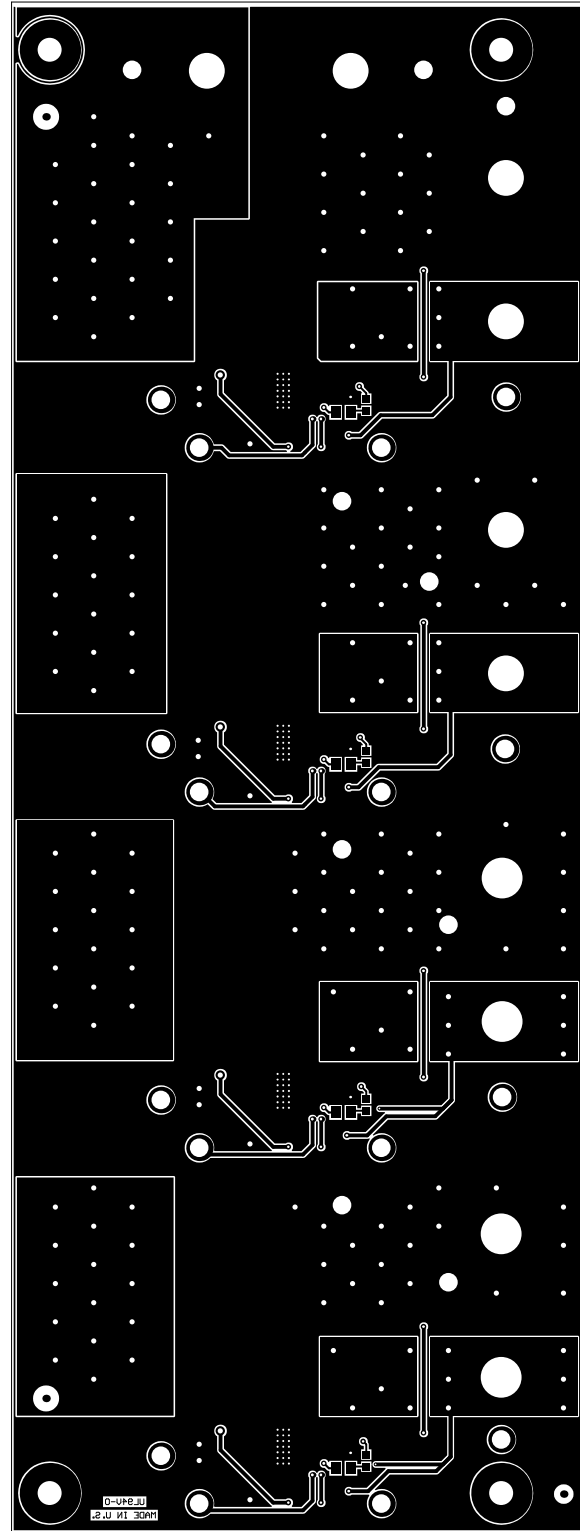
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7828 REVA	
LAYER NAME = Top Solder	ARTWORK # = 880007828-001 REV A	NATIONAL SEMICONDUCTOR
PLOT NAME = Top Solder Mask	GENERATED : 6/14/2012 3:11:11 PM	



ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7828 REVA	
LAYER NAME = Top Layer	ARTWORK # = 880007828-001 REV A	NATIONAL SEMICONDUCTOR
PLOT NAME = Top Layer	GENERATED : 6/14/2012	3:11:11 PM

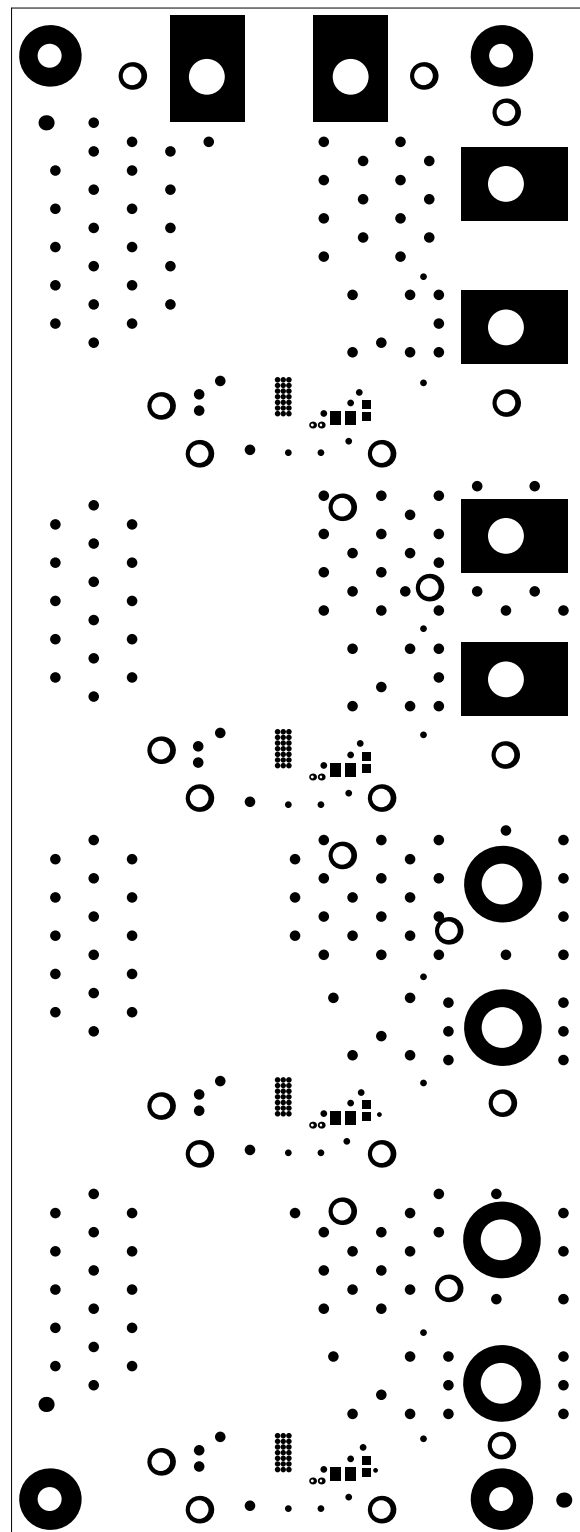




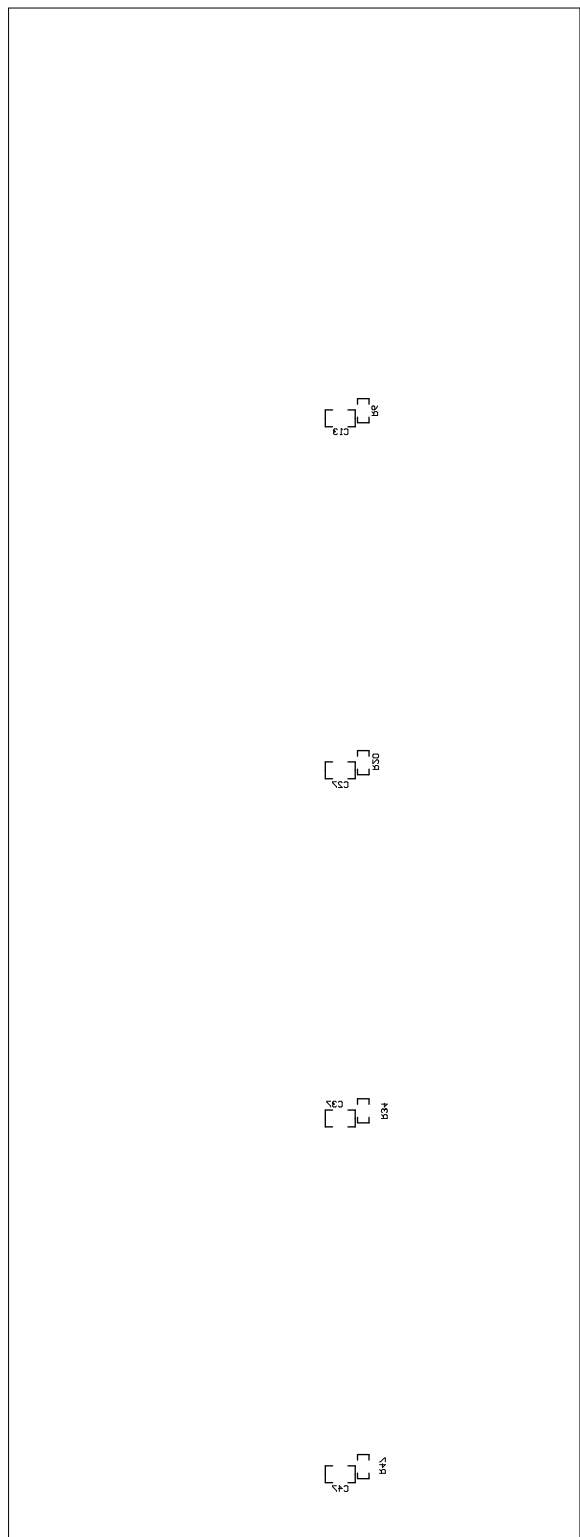


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ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7828 REVA	
LAYER NAME = Bottom Layer	ARTWORK # = 880007828-001 REV A	NATIONAL SEMICONDUCTOR
PLOT NAME = Bottom Layer	GENERATED : 6/14/2012 3:11:12 PM	



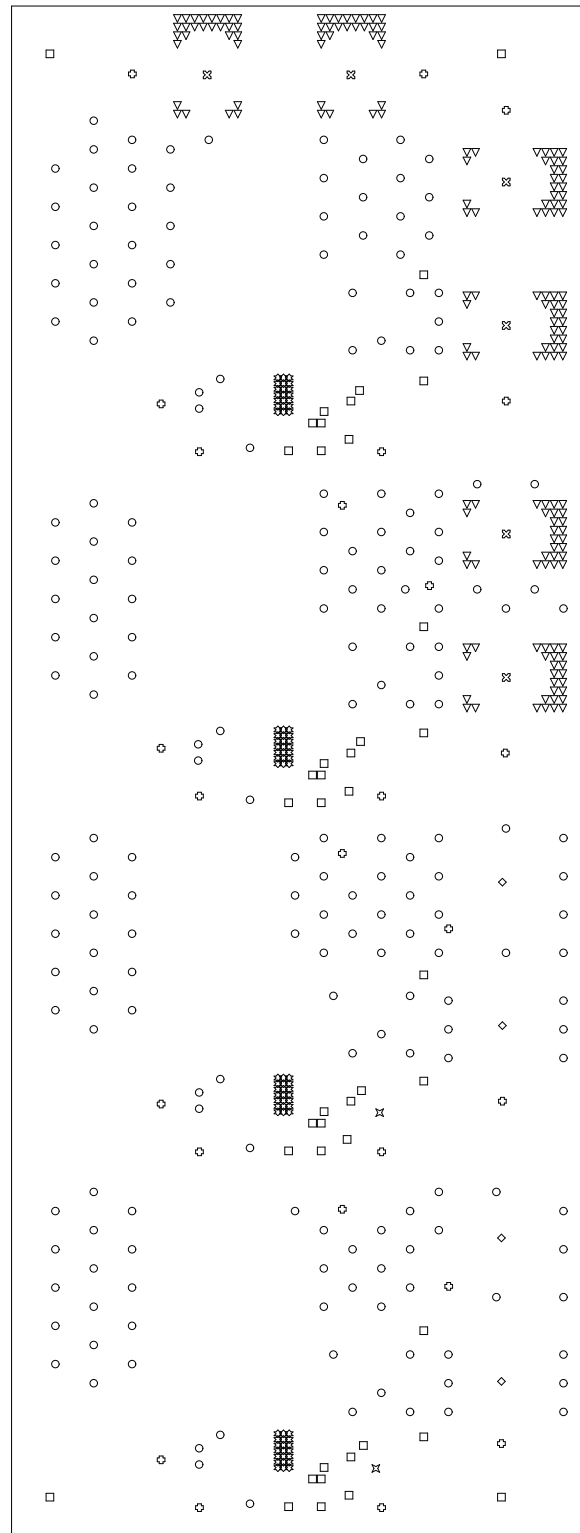
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7828 REVA	
LAYER NAME = Bottom Solder	ARTWORK # = 880007828-001 REV A	NATIONAL SEMICONDUCTOR
PLOT NAME = Bottom Solder Mask	GENERATED : 6/14/2012 3:11:12 PM	



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ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7828 REVA	
LAYER NAME = Bottom Overlay	ARTWORK # = 880007828-001 REV A	NATIONAL SEMICONDUCTOR
PLOT NAME = Bottom Overlay	GENERATED : 6/14/2012 3:11:12 PM	

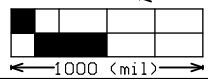
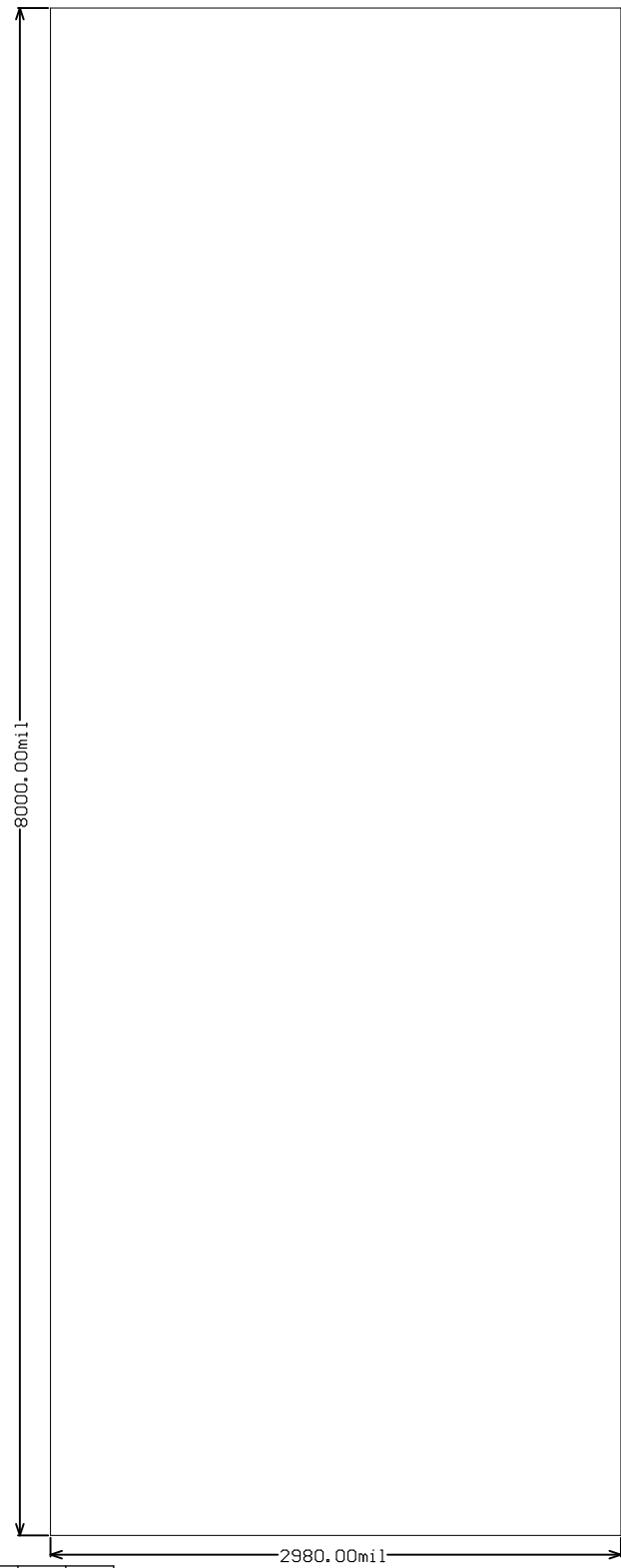




Symbol	Hit Count	Tool Size	Plated	Hole Type
⊠	2	10mil (0.254mm)	PTH	Round
○	84	11.81mil (0.3mm)	PTH	Round
□	40	15mil (0.381mm)	PTH	Round
▽	168	16mil (0.4064mm)	PTH	Round
○	208	20mil (0.512mm)	PTH	Round
○	25	98.425mil (2.5mm)	PTH	Round
□	4	125.984mil (3.2mm)	PTH	Round
■	6	188mil (4.7752mm)	PTH	Round
○	4	214.567mil (5.45mm)	PTH	Round
	541	Total		

Drill Table

ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7828 REVA	
LAYER NAME = Drill Drawing	ARTWORK # = 880007828-001 REV A	NATIONAL SEMICONDUCTOR
PLOT NAME = Drill Drawing	GENERATED : 6/14/2012 3:11:13 PM	



ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = PMP7828 REVA	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880007828-001 REV A	NATIONAL SEMICONDUCTOR
PLOT NAME = Board Dimensions	GENERATED : 6/14/2012 3:11:13 PM	

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