PR413
TMS320x281x Design 2
TPS70202 Low Cost Design

FEATURES:

- Meets the sequencing requirements (Option 2) of the TMS320F281x processor. Can be simplified to power the TMS320C281x and TMS320R281x.
- Dual-channel TPS70202 500mA/200mA low-dropout (LDO) linear regulator in thermally enhanced PowerPAD^{TM} package saves cost and space.
- Linear regulators start-up fast, allowing large in-rush currents for charging bulk capacitors at start-up. The current draw on the input power supply is minimized by sequencing first the I/O rail then the core rail.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at http://power.ti.com then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at http://focus.ti.com/lit/ds/symlink/tps70202.pdf
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.

IMPLEMENTATION NOTES:

- **Component selection:**
  - If different capacitors are used for C4 and C5 than recommended per the BOM, they must meet the ESR requirements per the datasheet.
- **Power Dissipation/Thermal Issues:**
  - The maximum output current per channel of the dual regulator is dependent on the device's power dissipation. The following equation can be used to compute actual power dissipation and/or maximum output current per channel:

    $$P_{Dact} = (V_{IN} - V_{DD\text{-}3.3V}) * I_{Vdd\text{-}3.3V} + (V_{IN} - V_{DD\text{-}CORE})*I_{Vdd\text{-}core}$$

    For example, the IC can only dissipate 1.1W at $T_A = 85^o$ C and no airflow.
  - The maximum power dissipation of which the package is capable is

    $$P_{Dmax} = (T_{Jmax} - T_A)/R_{\Theta JA}$$

    where T_{Jmax} is the maximum junction temperature of the device and $R_{\Theta JA}$ is the thermal resistance for a given board type and set of ambient conditions.
  - Refer to the application section of the datasheet for thermal resistances at different ambient temperatures, airflows and ground plane heatsink area.
- **Modifications for C281x and R281x:**
  - Since sequencing is not required for the TMS320C281x or the TMS320R281x, transistor Q1 and resistors R1 and R7 can be omitted, PG1 and PG2 can be tied to MR and both /EN1 and /EN2 can be tied

together, thereby allowing both regulators to be enabled at the same time and removing power rail sequencing. However, sequencing is still recommended since it helps to prevent the input power supply from being pulled down at start-up due to in-rush currents for charging each rail's bulk capacitors.

- **Waveforms:**
  Waveforms were generated while powering an ezDSP TMS320F2812 evaluation board loaded with the 1.8-V rail pulling 200 mA and the 3.3-V rail pulling 175 mA steady state.

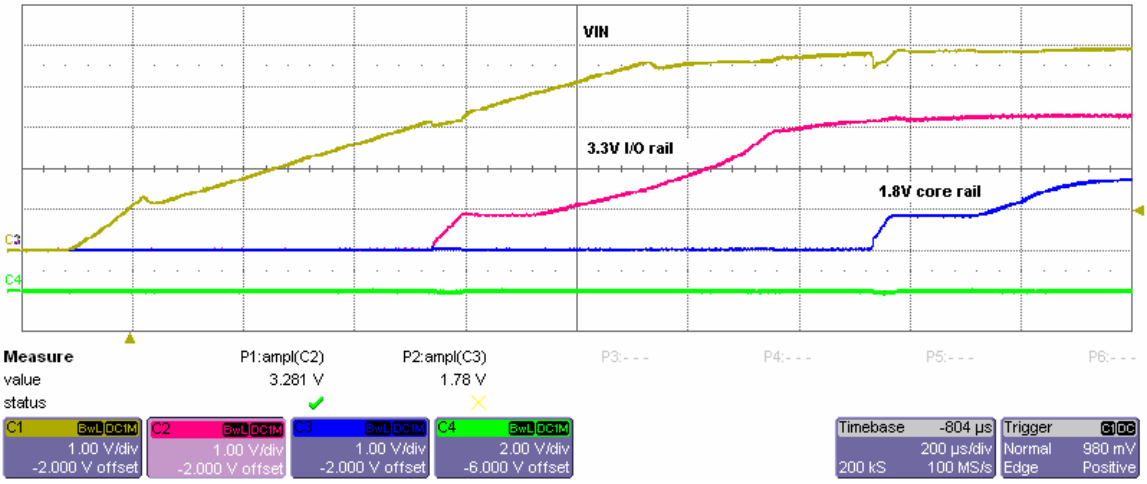


Figure 1 - Power up with V_{IN} = 5.0 V, /EN grounded

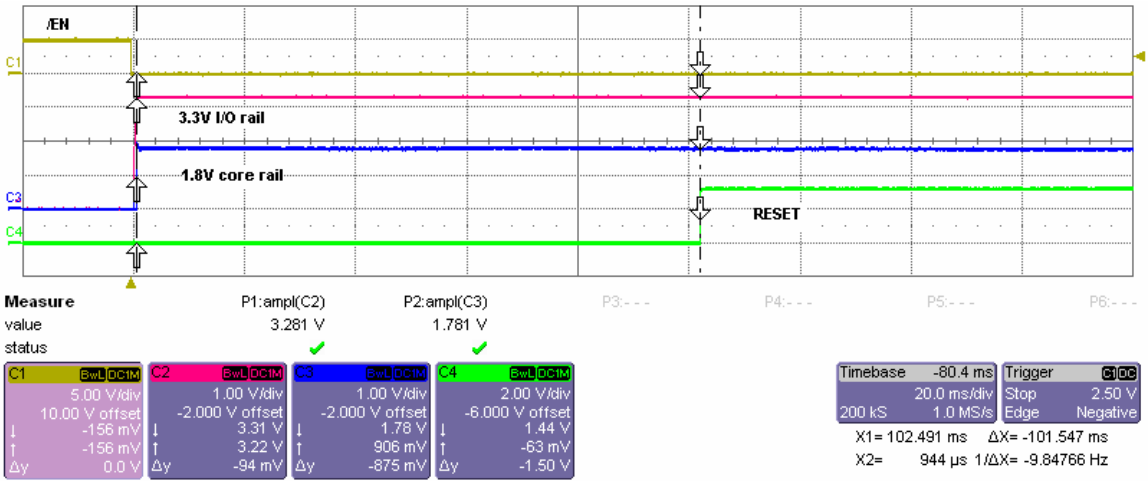


Figure 2 - Power up from enable when V_{IN} = 5.0 V

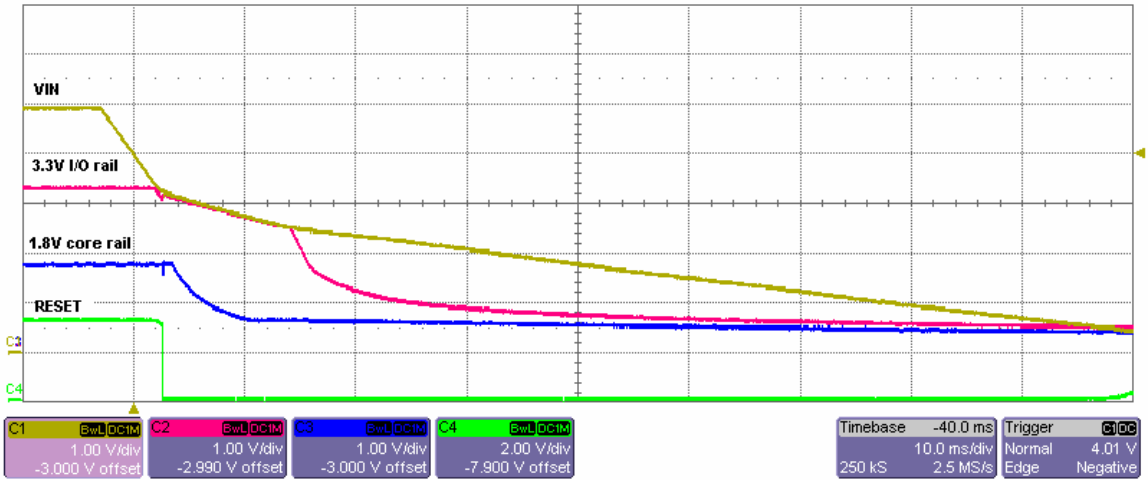


Figure 3 - Power down with V_{IN} = 5.0 V, /EN grounded

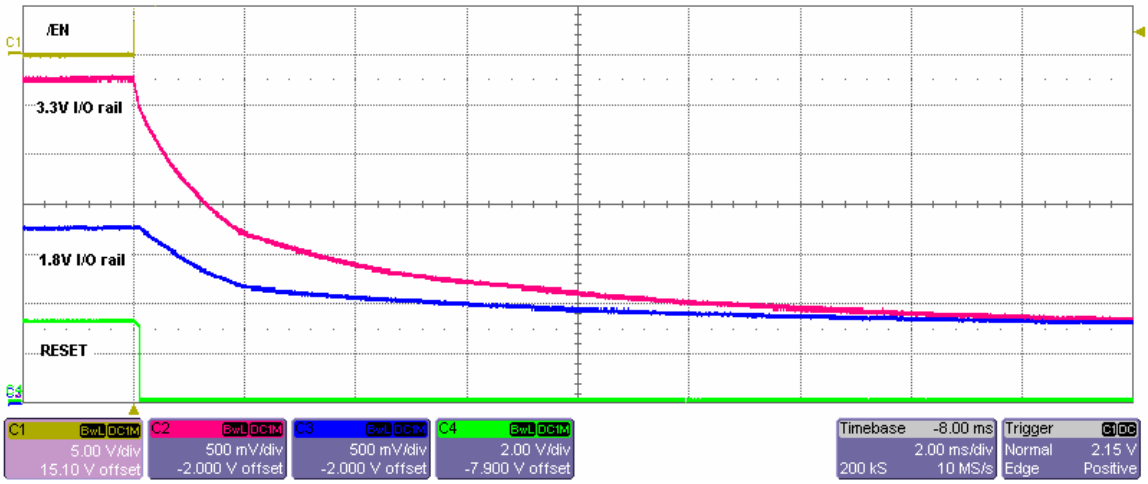


Figure 4 - Power down from enable when V_{IN} = 5.0 V

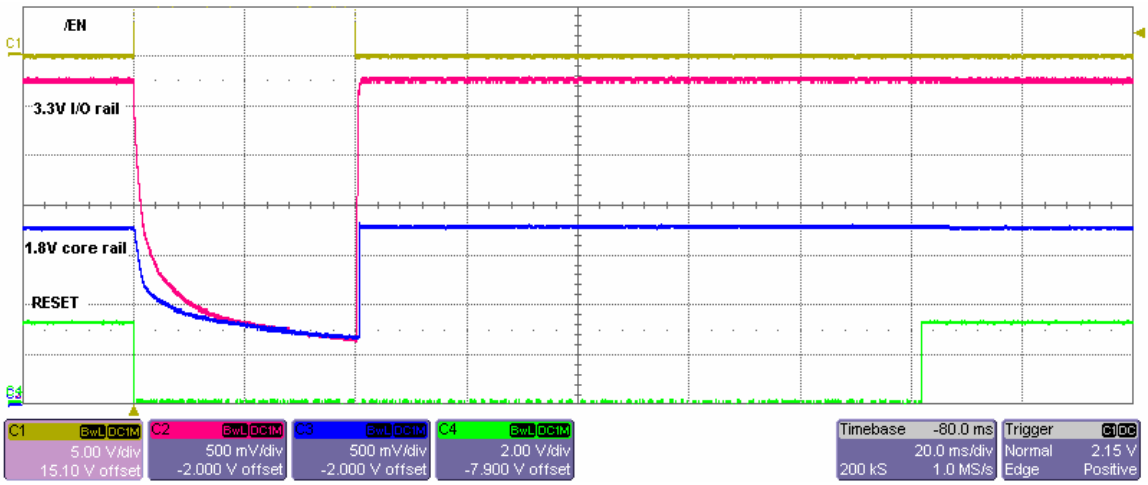


Figure 5 - RESET and recovery after V_{DD} = 3.3V fails

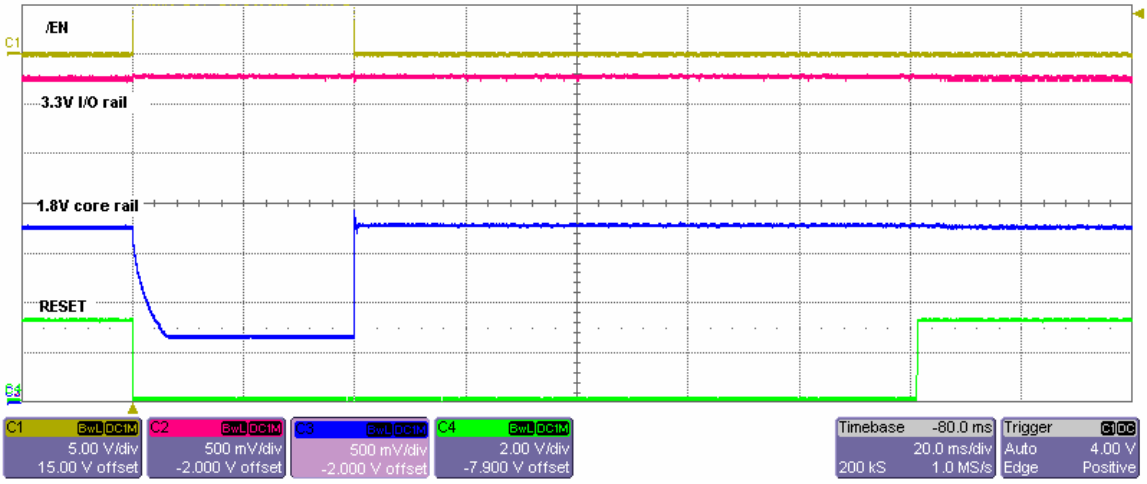
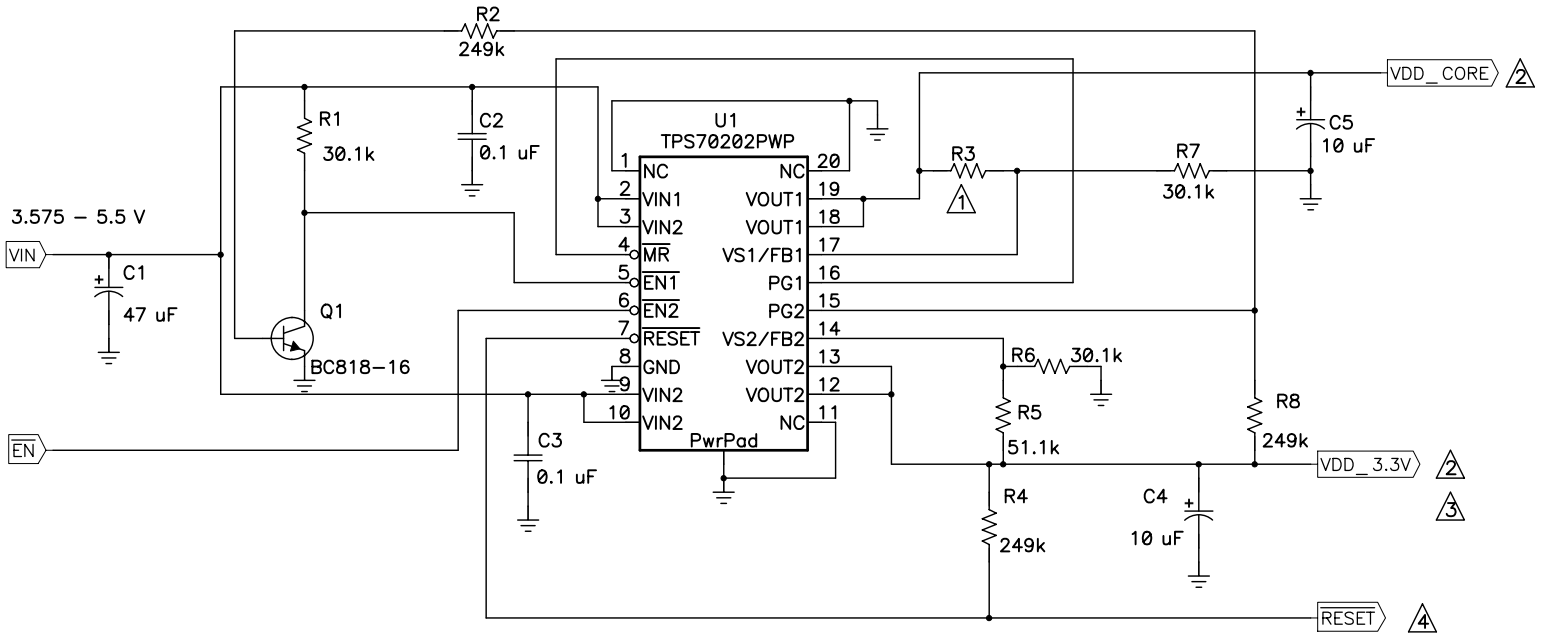


Figure 6 - RESET and recovery after V_{DD} = 1.8V fails

QUESTIONS?

- Send an email to mailto:**dsppower@list.ti.com**



1

VDD_CORE	R3	VDD_CORE TOL	LDO SVS TOL
1.8V	14.3k	1.76–1.85	92%–98% VDD_CORE
1.9V	16.5k	1.84–1.95	92%–98% VDD_CORE

Assumes 1% resistors

2 Package power dissipation (Pd) determines maximum current.
Pd is a function of Vin and ambient temperature.

3

VDD_3.3V TOL	LDO SVS TOL
3.22–3.38	92%–98% VDD_3.3V

4 /RESET on the TPS70202 has a 120 ms delay and an open drain output which requires an external pullup resistor (R4 on this design).

Title	TMS320x281x DSP Attach Design 2 Low Cost	
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Date: 12/16/2004

PR413 BOM

COUNT		RefDes	Description	Size	Part Number	Mfr
1	1	C1	Capacitor, Tantalum, 47-uF, 6.3-V, 1.4-ohm, 20%	3528(B)	293D476X6R3B2	Vishay
2	2	C2, C3	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	0603	C1608X7R1E104KT	TDK
2	2	C4, C5	Capacitor, Tantalum, 10-uF, 6.3-V, 2.9-ohm, 20%	3528(B)	293D106X6R3B2	Vishay
1	1	Q1	Bipolar, NPN, 25-V, 500-mA, 310-mW	SOT23	BC818-16	Vishay
3	3	R1, R6, R7	Resistor, Chip, 30.1k-Ohms, 1/16-W, 1%	0603	Std	Std
3	3	R2, R4, R8	Resistor, Chip, 249k-Ohms, 1/16-W, 1%	0603	Std	Std
1		R3	Resistor, Chip, 14.3k-Ohms, 1/16-W, 1%	0603	Std	Std
	1		Resistor, Chip, 16.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R5	Resistor, Chip, 51.1k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	U1	IC, Dual-output LDO Regulator w/SVS	PWP20	TPS70202PWP	TI

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