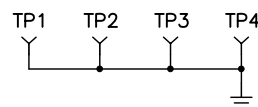


Layout plan for UCD9240 & related circuitry:  
 Top & bottom layer: Signal traces  
 Layer two: ground plane  
 layer 3: Analog ground near near UCD9240  
 to pick up all analog connections  
 and V33 elsewhere  
 if inner layers needed for signal traces  
 use layer 3, not 2

Generally: most critical to get  
 filter caps close as possible to respective pins  
 All grounded pins to be tied directly to U1 powerpad  
 and have a feed thru close by to layer 2

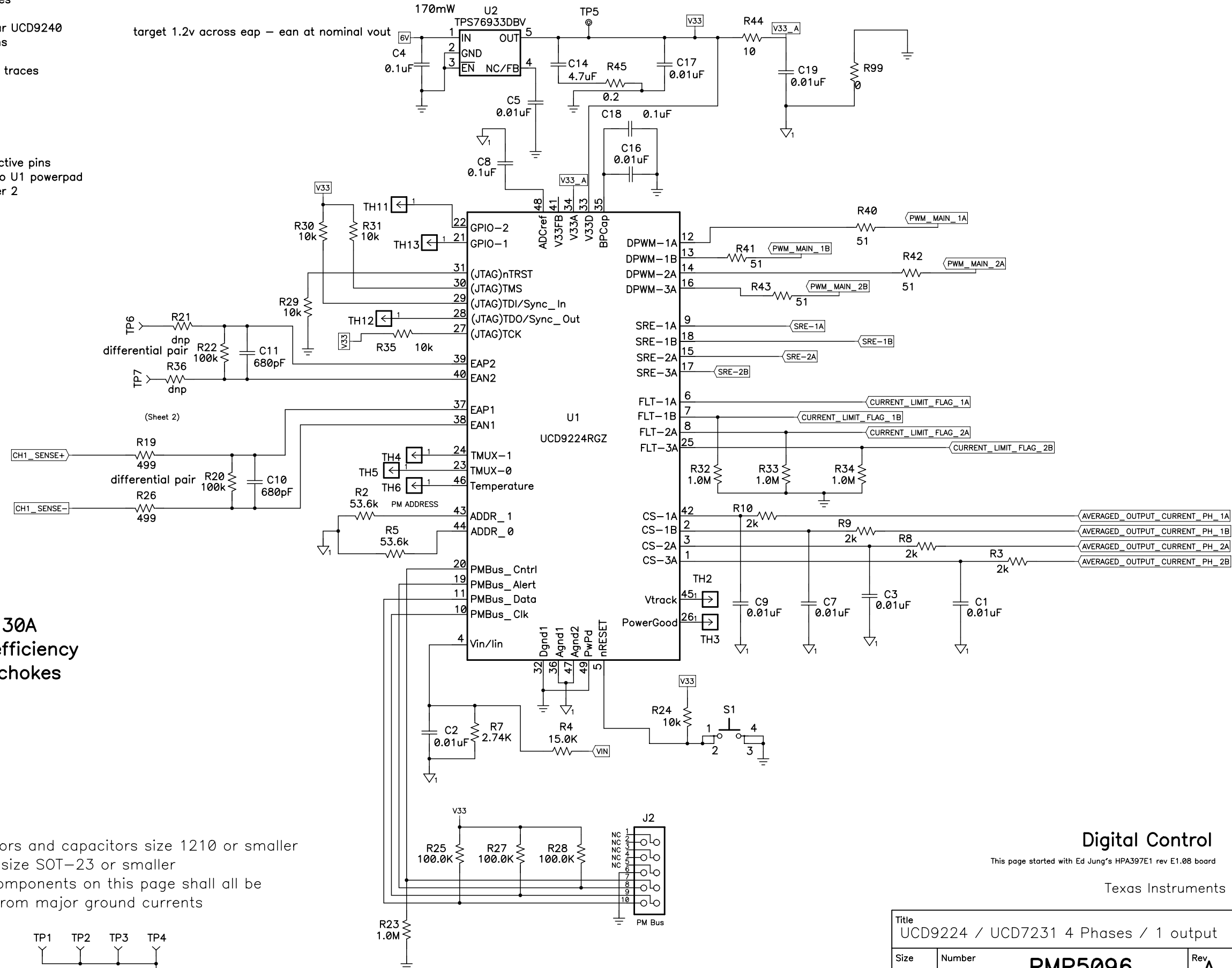
First build:  
 1.0V at 120A  
 each channel at 30A  
 Will target max efficiency  
 300kHz, largest chokes

Parts placement:  
 Top side: any  
 bottom side: Only resistors and capacitors size 1210 or smaller  
 and active components size SOT-23 or smaller  
 UCD9240 and related components on this page shall all be  
 in corner of PCB away from major ground currents



R45 added in Test in series with C14  
 to prevent U2 from oscillating.

C17, C19 near U1 pins 33,34



### Digital Control

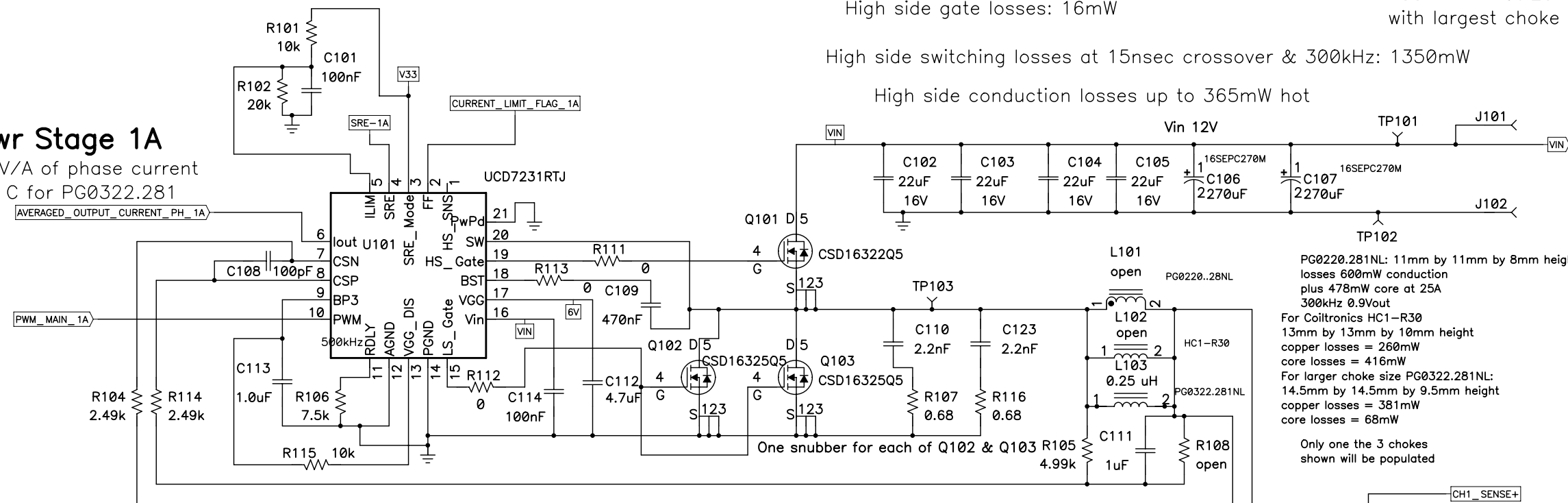
This page started with Ed Jung's HPA397E1 rev E1.08 board

Texas Instruments

Title UCD9224 / UCD7231 4 Phases / 1 output		
Size C	Number <b>PMP5096</b>	Rev <b>A</b>
Date Oct. 27, 2009	Drawn by Josh Mandelcorn	
Engineer Josh Mandelcorn	Filename PMP5096_revA.sch	Sheet 1 of 5

# Pwr Stage 1A

0.5V + 37.6mV/A of phase current at 25 degrees C for PG0322.281



Overall efficiency estimate:  
160mW / A at 25 A  
with smallest choke  
135mW / A at 25 A  
with largest choke

High side gate losses: 16mW

High side switching losses at 15nsec crossover & 300kHz: 1350mW

High side conduction losses up to 365mW hot

PG0220.281NL: 11mm by 11mm by 8mm height plus leads  
losses 600mW conduction  
plus 478mW core at 25A  
300kHz 0.9Vout  
For Coiltronics HC1-R30  
13mm by 13mm by 10mm height  
copper losses = 260mW  
core losses = 416mW  
For larger choke size PG0322.281NL:  
14.5mm by 14.5mm by 9.5mm height  
copper losses = 381mW  
core losses = 68mW  
Only one the 3 chokes  
shown will be populated

differential pair  
Low side conduction losses 940mW  
gate losses at 300kHz / 6Vgs: 68mW  
for 2 FETs

Layout plan for power stages:  
layers top & bottom for most power and signal traces  
layer 2 will be ground,  
power pad of Ux01 to ground with several vias  
layer 3 will be VIN

Sanyo SEPC caps:  
max ESR listed is for 100kHz - 300kHz  
Based on current deratings for 10-100kHz  
it appears that ESR doubles at 10kHz to be 14mOhms max

100uF, 6.3V, X5R Murata VDC=1.8V  
size 1210  
max Z at 50kHz -j55mOhms  
at 30kHz -j92mOhms

Output ripple estimate:  
With only the ceramic caps  
about 25mV p-p  
With the OSCON caps added  
under 20mV p-p

Common output caps & load connections  
for all 4 phases

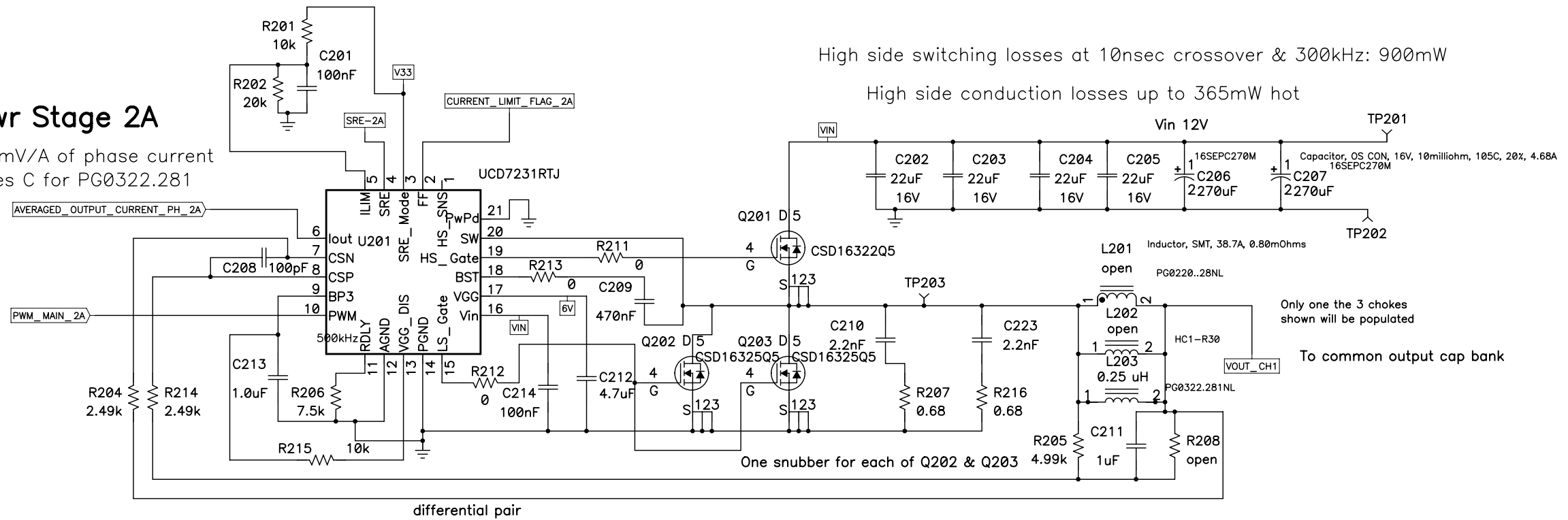
Texas Instruments

Title UCD9224 / UCD7231 4 Phases / 1 output		
Size C	Number <b>PMP5096</b>	Rev <b>A</b>
Date Oct. 27, 2009	Drawn by Josh Mandelcorn	
Engineer Josh Mandelcorn	Filename PMP5096_revA.sch	Sheet 2 of 5

## Phase 1a

# Pwr Stage 2A

0.5V + 37.6mV/A of phase current at 25 degrees C for PG0322.281



Layout plan for power stages:  
 layers top & bottom for most power and signal traces  
 layer 2 will be ground,  
 power pad of Ux01 to ground with several vias  
 layer 3 will be VIN

Low side conduction losses 872mW  
 gate losses at 300kHz / 6Vgs: 34mW

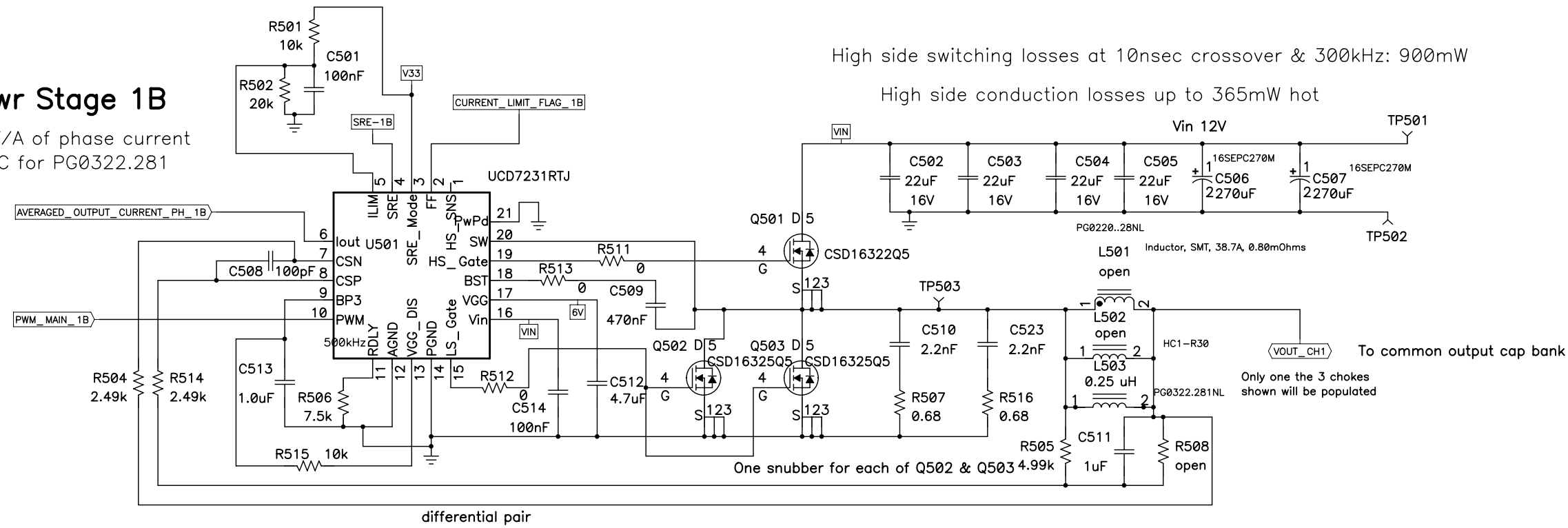
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## Phase 2a

Title UCD9224 / UCD7231 4 Phases / 1 output		
Size C	Number <b>PMP5096</b>	Rev <b>A</b>
Date Oct. 27, 2009	Drawn by Josh Mandelcorn	
Engineer	Filename PMP5096_revA.sch	Sheet 3 of 5

# Pwr Stage 1B

0.5V + 37.6mV/A of phase current  
at 25 degrees C for PG0322.281



High side switching losses at 10nsec crossover & 300kHz: 900mW

High side conduction losses up to 365mW hot

Low side conduction losses 872mW  
gate losses at 300kHz / 6Vgs: 34mW

Layout plan for power stages:  
layers top & bottom for most power and signal traces  
layer 2 will be ground,  
power pad of Ux01 to ground with several vias  
layer 3 will be VIN

Modified from PMP4914 rev A PCB

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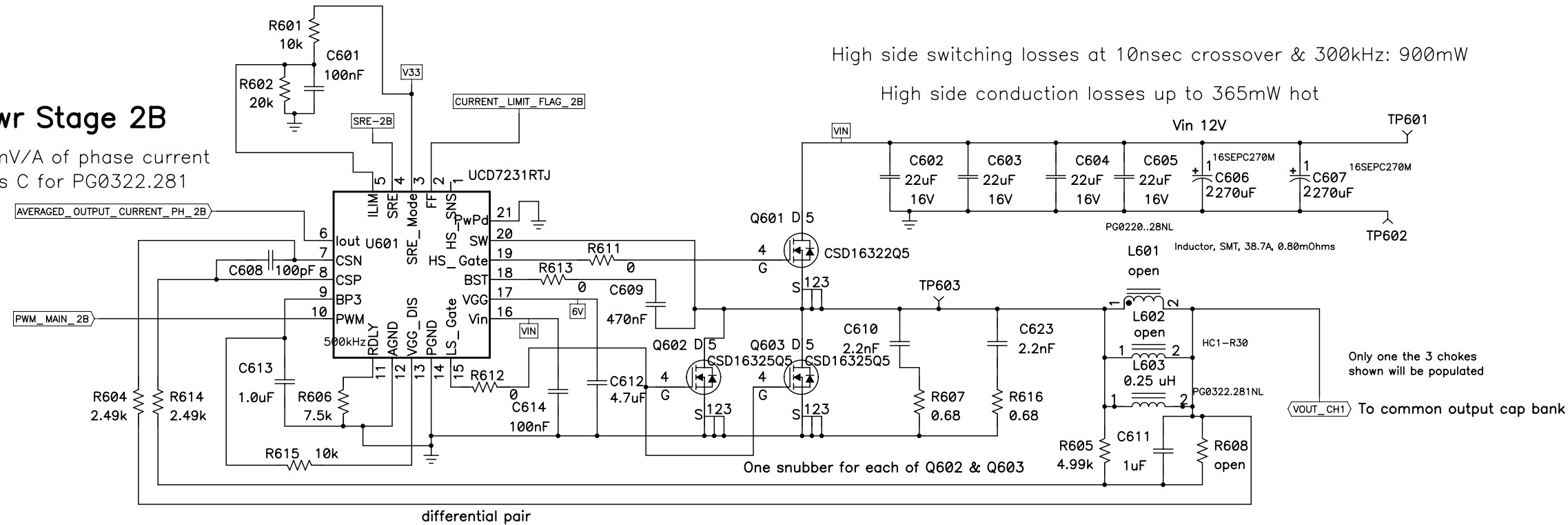
Power trains from PMP2581 by B. Geck

## Phase 1b

Title UCD9224 / UCD7231 4 Phases / 1 output		
Size C	Number <b>PMP5096</b>	Rev <b>A</b>
Date Oct. 27, 2009	Drawn by Josh Mandelcorn	
Engineer Josh Mandelcorn	Filename PMP5096_revA.sch	Sheet 4 of 5

## Pwr Stage 2B

0.5V + 37.6mV/A of phase current  
at 25 degrees C for PG0322.281



High side switching losses at 10nsec crossover & 300kHz: 900mW

High side conduction losses up to 365mW hot

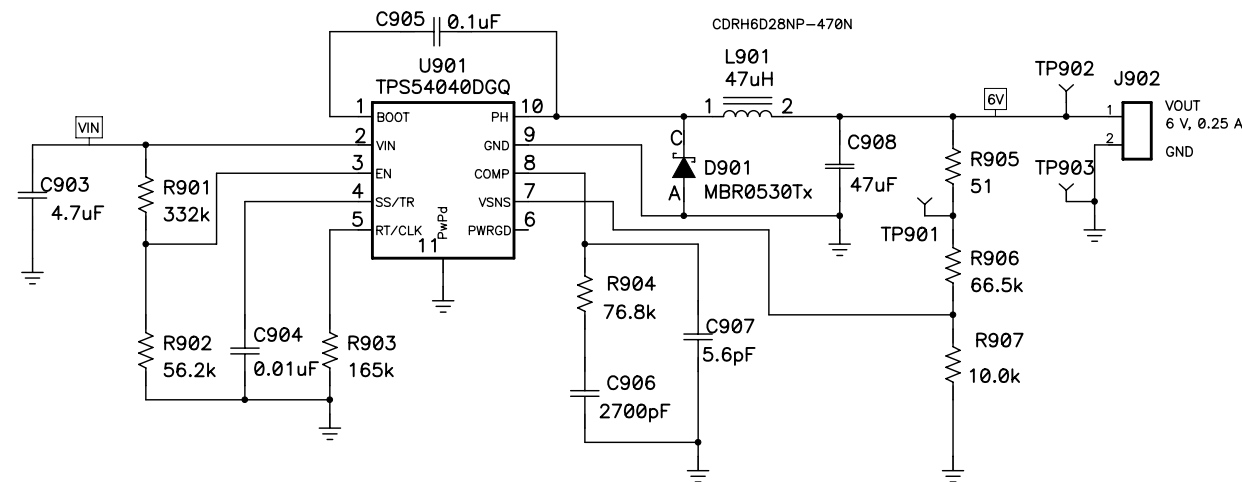
Low side conduction losses 872mW  
gate losses at 300kHz / 6Vgs: 34mW

Layout plan for power stages:  
layers top & bottom for most power and signal traces  
layer 2 will be ground,  
power pad of Ux01 to ground with several vias  
layer 3 will be VIN

Only one the 3 chokes  
shown will be populated

To common output cap bank

## Bias For Gate Drive



Texas Instruments

## Phase 2b

Title UCD9224 / UCD7231 4 Phases / 1 output		
Size C	Number <b>PMP5096</b>	Rev A
Date Oct. 27, 2009	Drawn by Josh Mandelcorn	
Engineer Josh Mandelcorn	Filename PMP5096_revA.sch	Sheet 5 of 5

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