## Fabrication Chart

<table>
<thead>
<tr>
<th>FINISHED THICKNESS</th>
<th>SILSCREEN</th>
<th>SOLDMASK</th>
<th>FINISHED COPPER WEIGHT</th>
</tr>
</thead>
<tbody>
<tr>
<td>□ 0.031</td>
<td>[Layer 1]</td>
<td>[Layer 1]</td>
<td>□ 1 oz.</td>
</tr>
<tr>
<td>□ 0.062</td>
<td>[Layer 4]</td>
<td>[Layer 4]</td>
<td>□ 2 oz.</td>
</tr>
<tr>
<td>□ 0.093</td>
<td>[NONE]</td>
<td>[NONE]</td>
<td>□ 2 oz.</td>
</tr>
<tr>
<td>□ 0.125</td>
<td>[NONE]</td>
<td>[NONE]</td>
<td>□ OTHER</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DESIGN</th>
<th>TRACE/GAP SPACING</th>
<th>LAYER COUNT</th>
</tr>
</thead>
<tbody>
<tr>
<td>□ GND</td>
<td>0.010/0.010</td>
<td>□ SINGLE SIDED</td>
</tr>
<tr>
<td>□ THRU-HOLE</td>
<td>0.008/0.007</td>
<td>□ 2 LAYER</td>
</tr>
<tr>
<td>□ MIX</td>
<td>0.006/0.006</td>
<td>□ 4 LAYER</td>
</tr>
</tbody>
</table>

### Notes: Unless Otherwise Specified

1. **Material:**
   All materials, including but not limited to base laminate, bonding materials, and solidmask coatings forming the finished printed circuit board shall meet UL-746B requirements and be RoHS compliant and have a flammability of UL94-EV0.

2. **Base Laminate:**
   Plastic sheet, laminated metal clad, one or two sides, base material NEEMA Type FR-4 or equivalent, R/tg =140 deg C or higher. Minimum decomposition temp (Td) of 320 deg C. Glass epoxy resin, copper-clad in accordance with 4 layer stack-up, compliant with lead free process.

3. **Solidmask:**
   Solldmask over bare copper (SM_BC) using liquid photo-imageable solidmask in accordance with IPC-SM-840. Color: Green. Minor solidmask adjustments to facilitate PCB fab and/or assembly is allowed provided no defects are created to final assembly as a result.

4. **Tolerances:**
   Unless otherwise specified PCB tolerances shall be ±0.003 inches, hole diameters shall be ±0.003 inches.

5. **Plating:**
   Holes requiring plating, see hole chart, to have 1 oz. (0.0014) min. thick copper.

6. **Finish:**
   Plate with RoHS compliant, immersion silver preferred, immersion tin or Sn/Ag/Cu, with Pd via 0.003" to 0.005" thick all exposed areas.
   As coated, no active pluses are acceptable.

7. **Legend:**
   If required, silkscreen Legend(s) with white non-conductive epoxy ink.

8. **Markings:**
   Board must bear vendor's identification code (etch or white non-conductive ink).
   Location optional.

9. **Workmanship:**
   Board is to be manufactured per PC-A-600 Class 2 requirements or better.

10. **Documentation:**
    PCB vendor is required to return any and all documents supplied or ultimately purchased by Texas Instruments upon completion of purchase order.

11. **Drill Sizes:**
    Hole diameters shown are finished sizes after plating unless otherwise noted.

12. **Panel Border:**
    Any metal in border area including part number, date code and/or revision letters must be covered with solidmask.

13. **Process Changes:**
    All dimensional, material, or process changes are allowed without prior explicit written permission from Texas Instruments.

14. **Controlled Impedance:**
    All pairs of 11 mil traces with 8 mil spacing between them on the top and bottom layer are controlled impedance.
    All pairs of 20 mil traces with 13 mil spacing between them on the top and bottom layer are controlled impedance.
    Requirement for the 11 and 20 mil edge-coupled coated micro strip on the top and bottom layer is 100 ohms ±10%.
    Controlled impedance applies to the following net pairs: PDP/PDQ, PD/PP2, PD/QD, PS4/PD4, PS4/PD4, PD/PD4, PD/QD, PD/QD, PD/QD.
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