AM64xx STARTER KIT EVM BOARD

SK-AM64

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REV	E2
VER	2.0

Note: Raspberry Pi is the trademark / wordmark of Raspberry Pi Foundation

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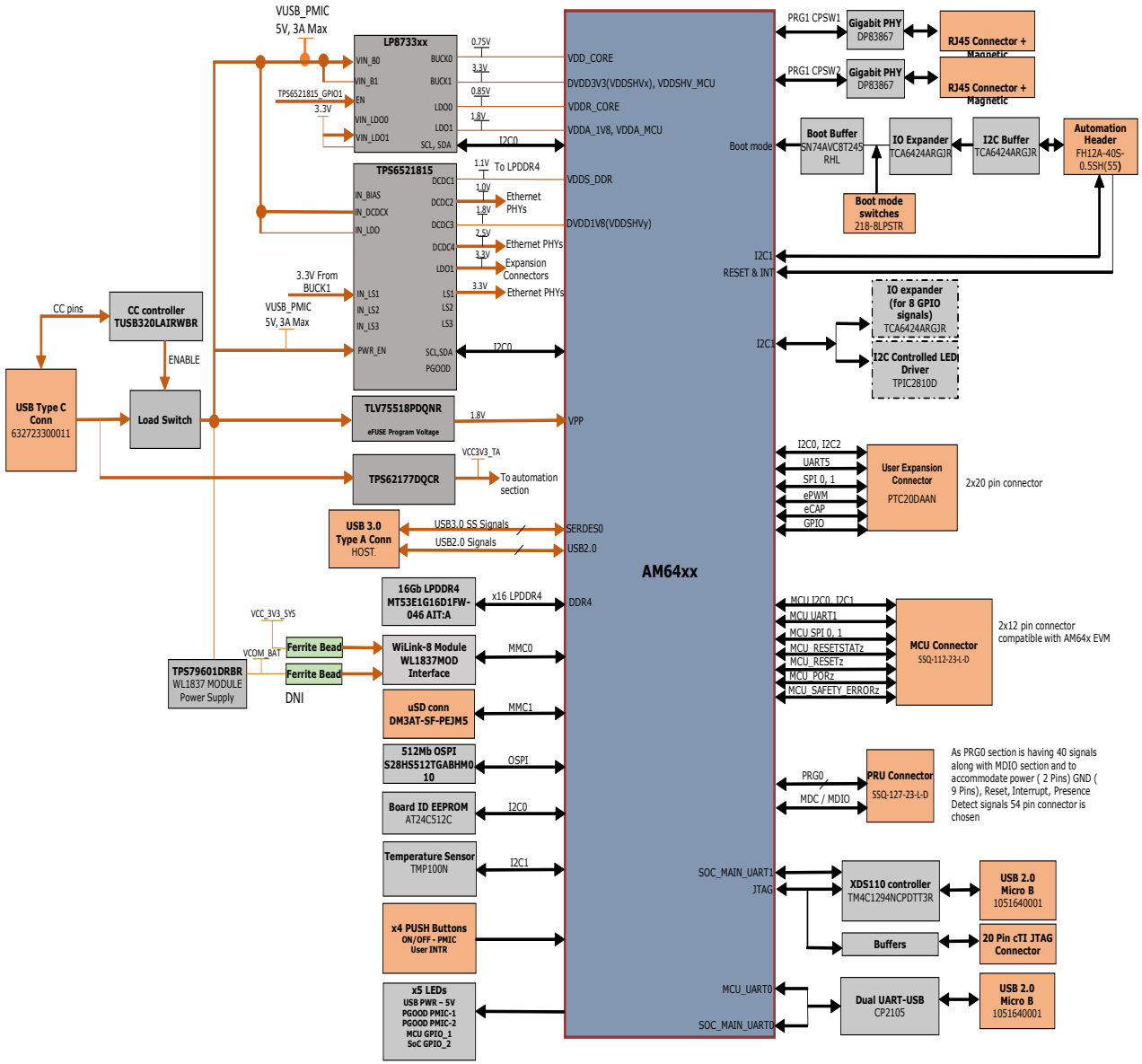
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
1.0	22nd JANUARY 2021	Drafted from "PROC100E1_SCH" Document	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.1	22nd JANUARY 2021	JP1,JP2,JP3,JP4,JP5 and JP6 removed. FL9 and FL14 made DNI. U31 Part Changed	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.2	24th JANUARY 2021	J9 changed to 28 pins. LD18 Added	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.3	27th JANUARY 2021	R246 changed to 0 ohm and R400 added	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.4	27th JANUARY 2021	U11,U13,U36,U37,U45 and U47 package changed LPDDR4_RESET_N pulled to VDD2_LPDDR4_1V1	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.5	02nd FEBRUARY 2021	FL24, FL25 Added. R237 changed from 0402 to 0201. VCC1V8_WLAN and VCC1V8_OSPI nets added	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.6	01st MARCH 2021	Text added for LP873345 PMIC	Mistral Design Team	Krishna Prasad	Krishna Prasad
1.7	17th MARCH 2021	R303 MADE AS DNI AND R301 MOUNTED	Mistral Design Team	Krishna Prasad	Krishna Prasad
2.0	30th MARCH 2021	Schematics Baselined	Mistral Design Team	Krishna Prasad	Krishna Prasad

BLOCK DIAGRAM_AM64x_SKEVM



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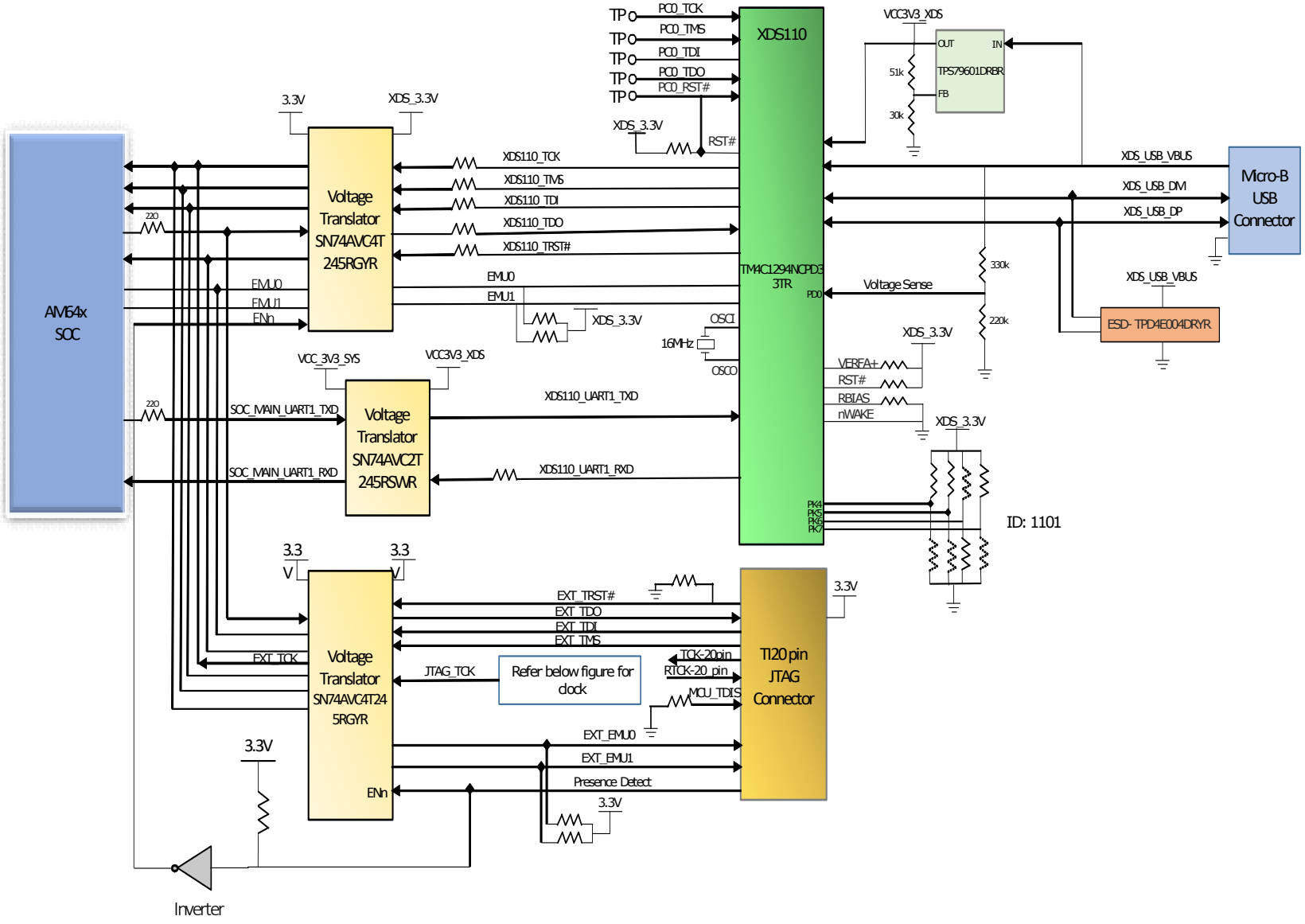
BLOCK DIAGRAM_XDS110



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Title	BLOCK DIAGRAM_XDS110		
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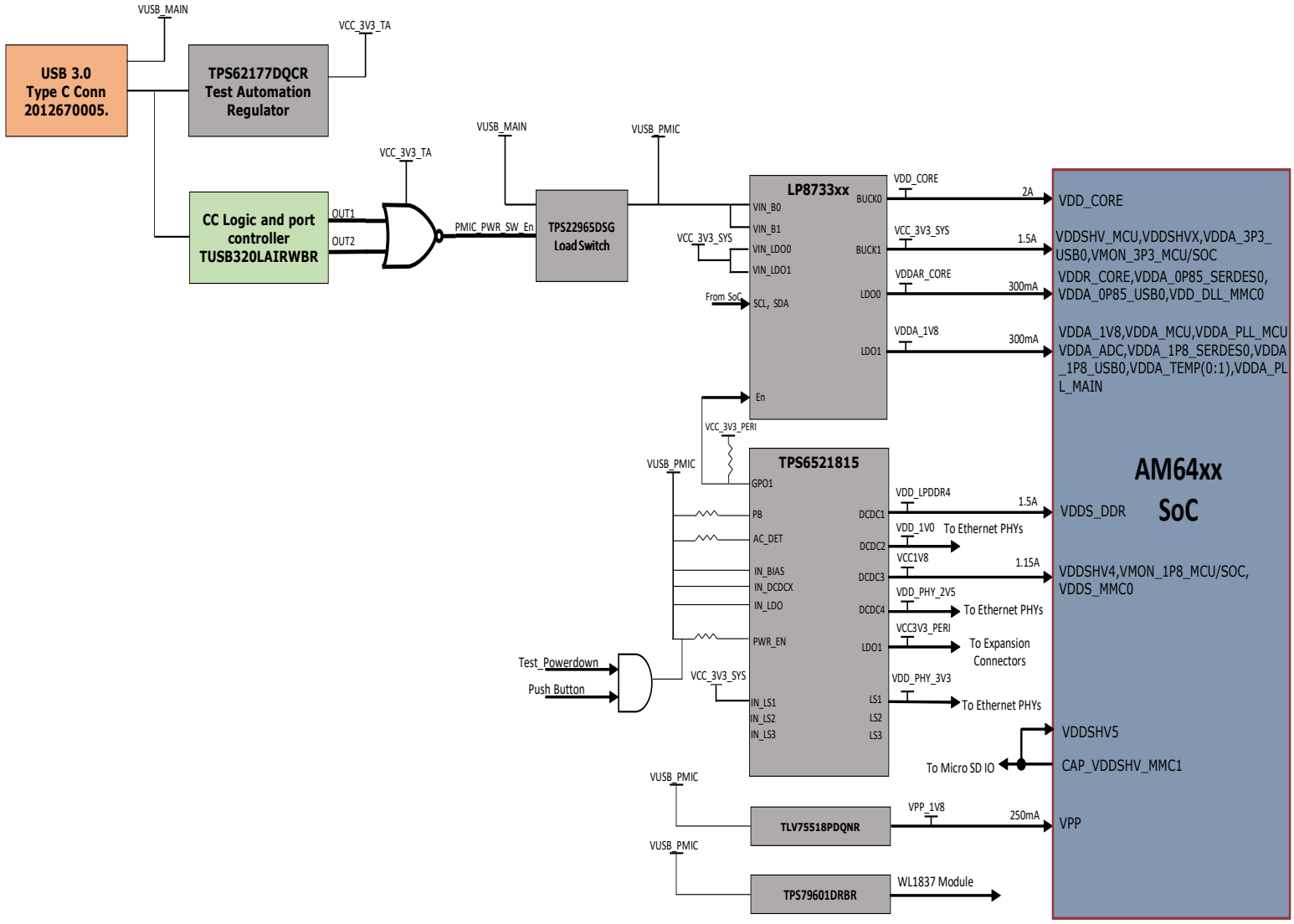
POWER BLOCK DIAGRAM



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Title	POWER BLOCK DIAGRAM	
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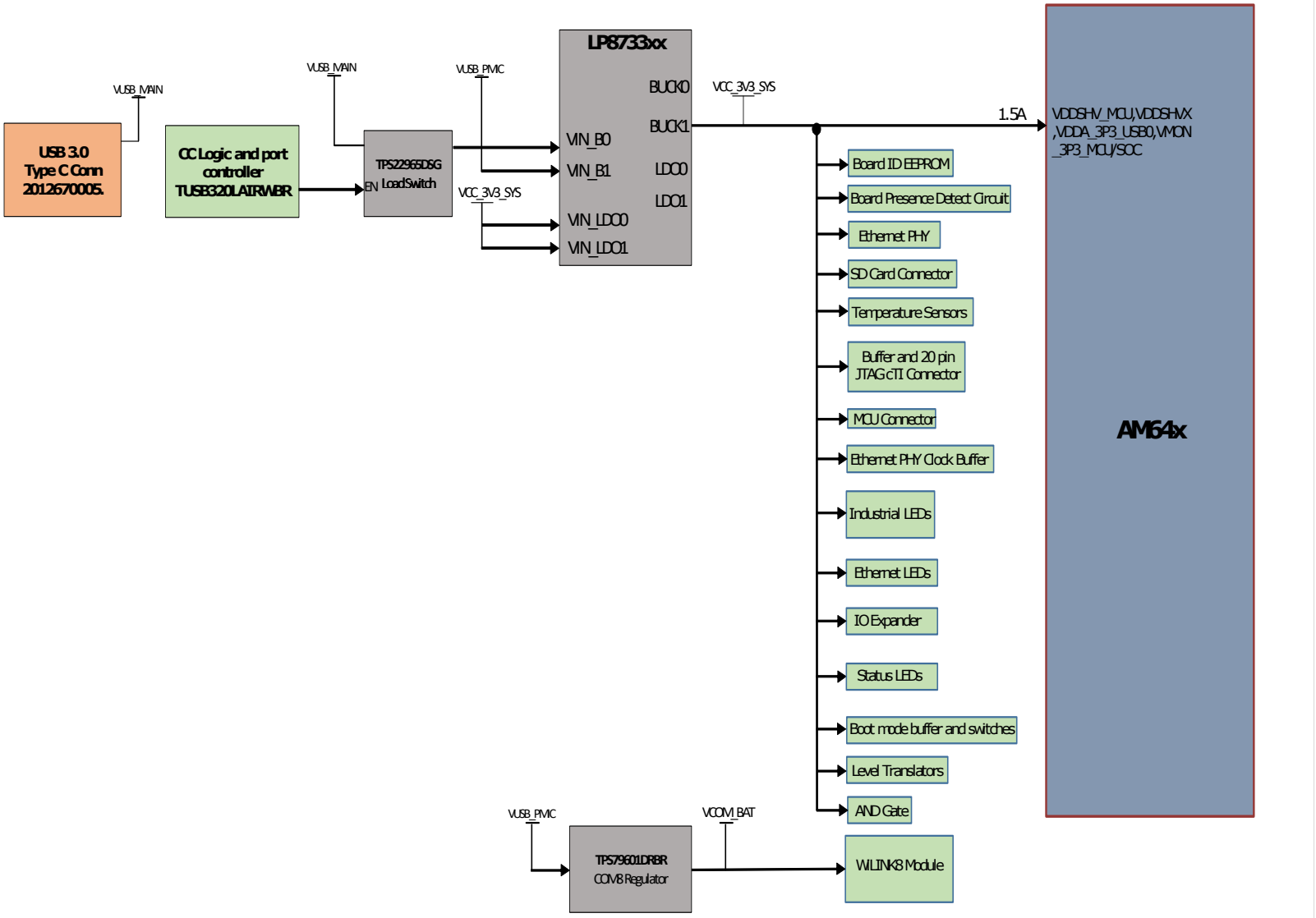
3V3 SUPPLY POWER FLOW



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Title	3V3 SUPPLY POWER FLOW	
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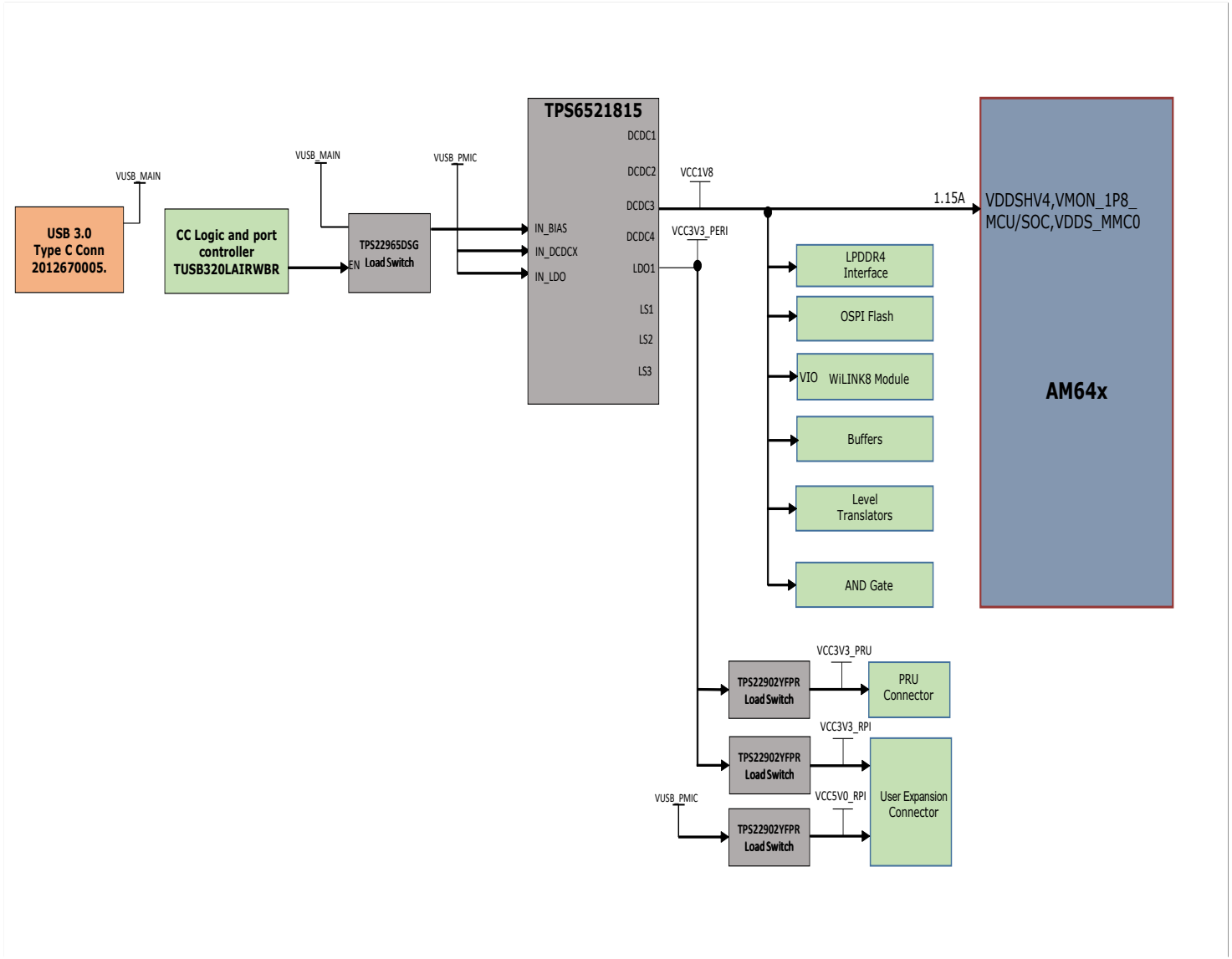
1V8 SUPPLY POWER FLOW



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Title	1V8 SUPPLY POWER FLOW	
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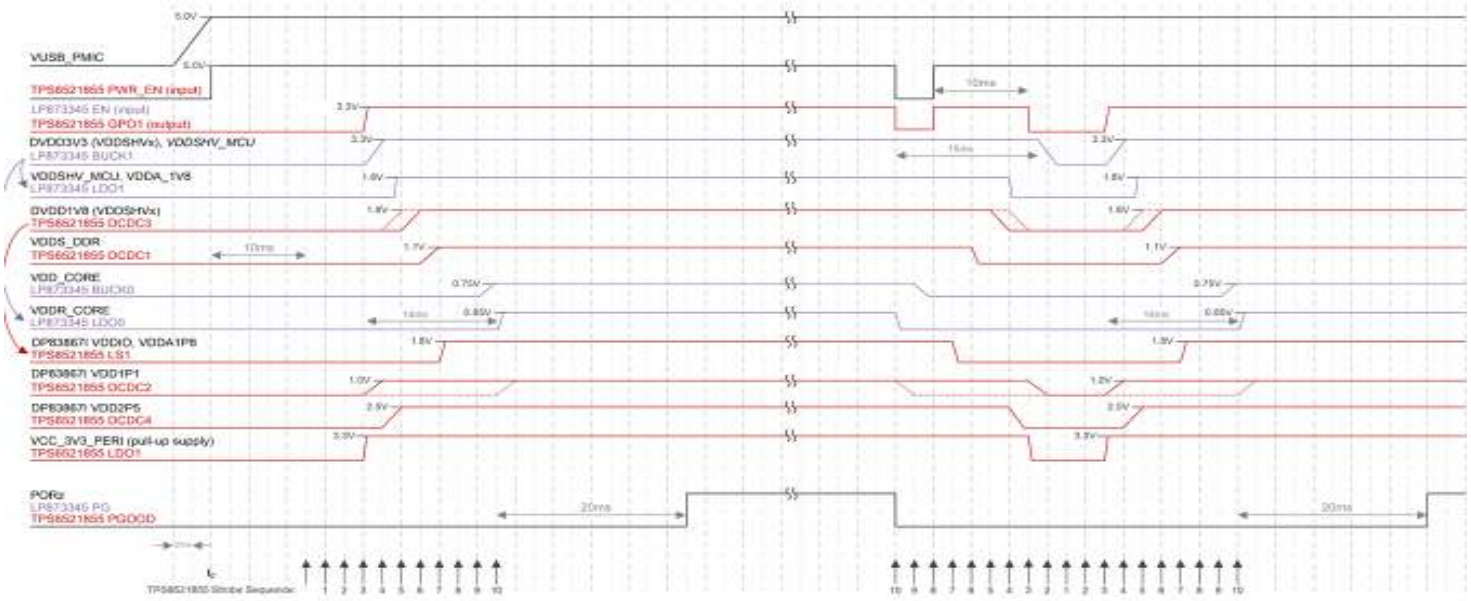
POWER SEQUENCE



LP873345 OTP Configuration

STARTUP_DELAY_SEL=1

BUCK1_STARTUP_DELAY[3:0] = 0x0 = 0ms

LDO1_STARTUP_DELAY[3:0] = 0x3 = 3ms

BUCK0_STARTUP_DELAY[3:0] = 0xC = 12ms

LDO0_STARTUP_DELAY[3:0] = 0xE = 14ms

BUCK1_SHUTDOWN_DELAY[3:0] = 0xF = 15ms

LDO1_SHUTDOWN_DELAY[3:0] = 0xC = 12ms

BUCK0_SHUTDOWN_DELAY[3:0] = 0x2 = 2ms

LDO0_SHUTDOWN_DELAY[3:0] = 0x0 = 0ms

*Max delay time = 0xF = 15ms

LP873345 GPOx (outputs) = un-used

BUCK0_RDIS_EN = 1b, BUCK1_RDIS_EN = 1b

LDO0_RDIS_EN = 1b, LDO1_RDIS_EN = 1b

PGOOD = Push-pull, active high
(VOL = VANA = 5V, VI of SN74LVC1G11 rated up to 5.5V, independent of VCC supply)

TPS6521855 EEPROM Configuration

SEQ1-2 = 0x00
(DLY1-9 = 0b = 2ms, DLYFACTR = 0b = 1x)

SEQ3[3:0] = DC1_SEQ = 0x5 = Strobe 5

SEQ3[7:4] = DC2_SEQ = 0x6 = Strobe 6

SEQ4[3:0] = DC3_SEQ = 0x5 = Strobe 5

SEQ4[7:4] = DC4_SEQ = 0x4 = Strobe 4

SEQ6[3:0] = LDO1_SEQ = 0x3 = Strobe 3

SEQ6[7:4] = LS1_SEQ = 0x7 = Strobe 7

SEQ7[3:0] = GPO1_SEQ = 0x3 = Strobe 3

SEQ7[7:4] = GPO3_SEQ = 0x0 = Disconnected from sequencer

SEQ5 = 0x00 = DCDC5/6 disconnected from sequencer

*PWR_EN deglitch + 9*2ms = 10ms + 18ms = 28ms

CONFIG1 = 0x08
(GPO2_BUF = 0b, PGDLY = 01b = 20ms, STRICT = 0b

CONFIG1 = 0x40
(DC12_RST = 0b, UVLOHYS = 1b = 400mV

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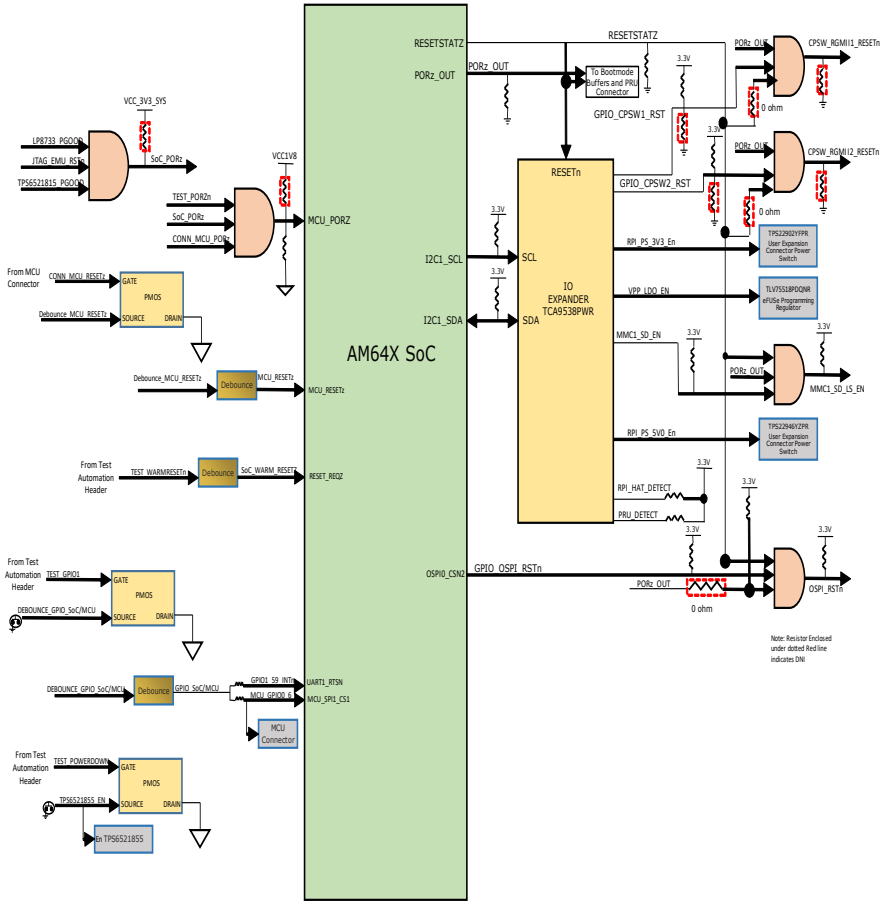
RESET ARCHITECTURE



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Title	RESET ARCHITECTURE	
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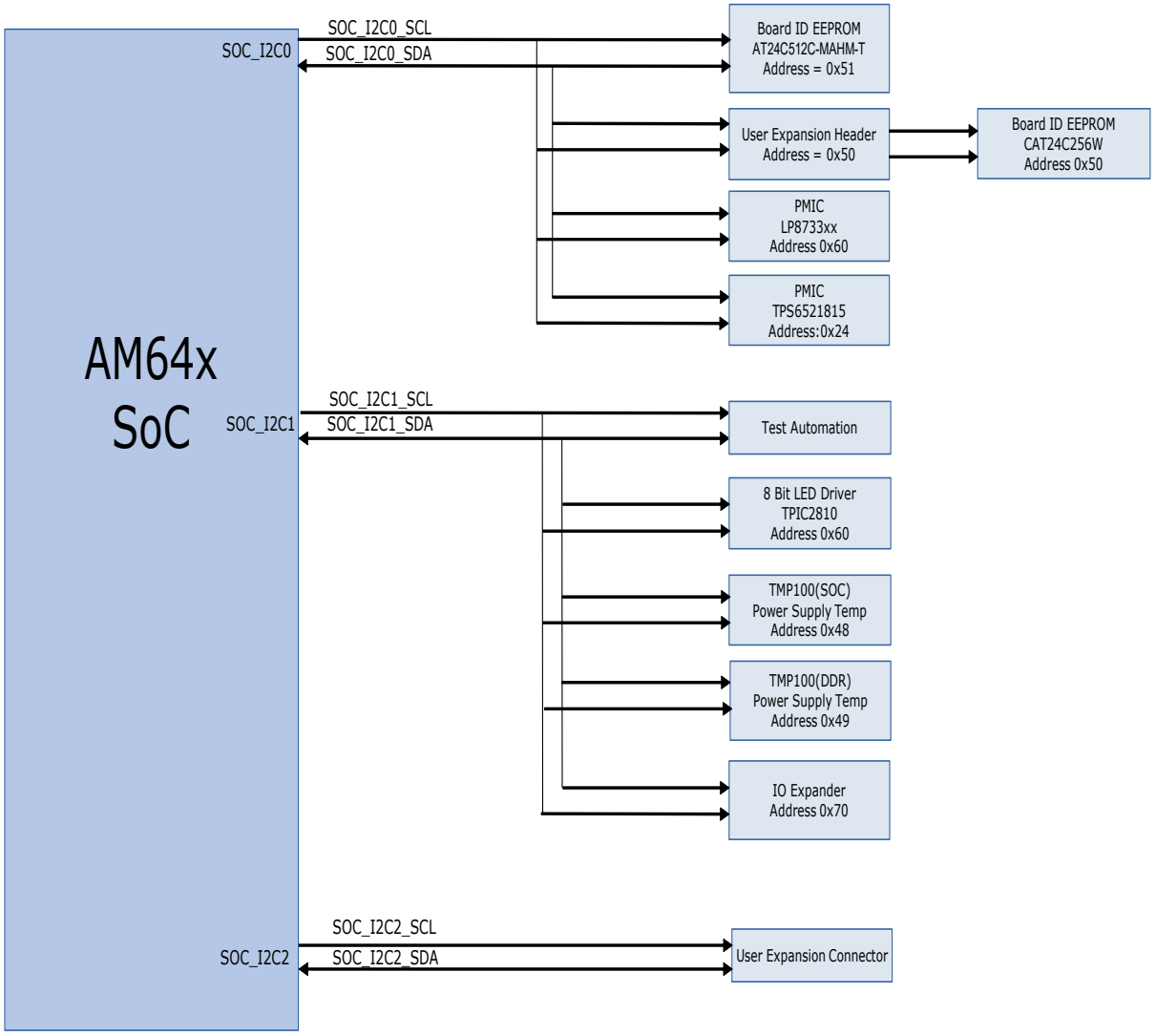
GPIO MAPPING TABLE

AM64xx GPIO MAPPING TABLE										
Sl.NO	GPIO Description	GPIO Netname	Functionality	GPIO Used	SoC Muxed Signal Name	Direction with respect to SoC	Default State	Active State	Voltage Domain On Processor Side	Voltage Connected on SKEVM
1	IO Expander Interrupt	IO_EXP_INTn_SDIO	Interrupt	GPIO1_78	MMC1_SDWP	Input	High	Low	VDDSHV0	SoC_DVDD3V3
2	Enable for COM8 Level Translator	COM8_LS_EN	Enable	GPIO0_62	PRG1_PRU0_GPO17	Output	High	Low	VDDSHV2	SoC_DVDD3V3
3	Enable for WLAN Interface in COM8 Connector	WLAN_EN_SoC_LS	Enable	GPIO0_48	PRG1_PRU0_GPO3	Output	Low	High	VDDSHV2	SoC_DVDD3V3
4	Enable for BT Interface in COM8 Connector	BT_EN_SOC_LS	Enable	GPIO0_49	PRG1_PRU0_GPO4	Output	Low	High	VDDSHV2	SoC_DVDD3V3
5	WLAN SDIO out-of band interrupt line	WLAN_IRQ_LS	Interrupt	GPIO0_46	PRG1_PRU0_GPO1	Input	High	Low	VDDSHV2	SoC_DVDD3V3
6	OSPI Interrupt	OSPI_INTn	Interrupt	GPIO0_14	OSPI0_CSN3	Input	High	Low	VDDSHV4	SOC_DVDD1V8
7	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	Reset	GPIO0_13	OSPI0_CSN2	Output	High	Low	VDDSHV4	SOC_DVDD1V8
8	User LED	TEST_LED1	Test	GPIO0_60	PRG1_PRU0_GPO15	Output	Low	High	VDDSHV2	SoC_DVDD3V3
9	User LED	TEST_LED2	Test	MCU_GPIO0_5	MCU_SPI1_CS0	Output	Low	High	VDDSHV_MCU	SoC_DVDD3V3
10	SD card load switch enable control	MMC1_SD_EN	Enable	IO Expander-P3		Output	High	High	VDDSHV0	SoC_DVDD3V3
11	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	Interrupt	GPIO1_70	EXTINTn	Input	High	Low	VDDSHV0	SoC_DVDD3V3
12	PRU Connector Interrupt	PRU_INTn								
13	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	Reset	IO Expander-P1		Output	High	Low	VDDSHV0	SoC_DVDD3V3
14	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	Reset	IO Expander-P0		Output	High	Low	VDDSHV0	SoC_DVDD3V3
15	TEST GPIO1 from Test Automation Connector	TEST_GPIO1	GPIO for communication with AM64x	GPIO1_59	UART1_RTSN	Input	High	Low	VDDSHV0	SoC_DVDD3V3
				MCU_GPIO0_6	MCU_SPI1_CS1	Input	High	Low	VDDSHV_MCU	SoC_DVDD3V3
16	LP8733xx PMIC Interrupt	PMIC_INT_B	Interrupt	GPIO0_45	PRG1_PRU0_GPO0	Input	High	Low	VDDSHV2	SoC_DVDD3V3
17	TPS6521815 PMIC Interrupt	PMIC_INT_B	Interrupt							
18	BTUART_RTS or Bootmode10 switch select	BTUART_RTS_SEL	Switch Selection	GPIO0_63	PRG1_PRU0_GPO18	Output	Low	High	VDDSHV2	SoC_DVDD3V3
19	VPP 1.8V regulator Enable	VPP_LDO_EN	Enable	IO Expander-P4		Output	Low	High	VDDSHV0	SoC_DVDD3V3
20	COM8 Regulator Enable	COM8_REG_EN	Enable	GPIO0_61	PRG1_PRU0_GPO16	Output	Low	High	VDDSHV2	SoC_DVDD3V3
21	Power Switch Enable for USB device	USB0_DRVBUS	Enable	GPIO1_79	USB0_DRVVBUS	Output	Low	High	VDDSHV0	SoC_DVDD3V3
22	RPI-HAT Detection	RPI_HAT_DETECT	Detection	IO Expander-P7		Input	High	Low	VDDSHV0	SoC_DVDD3V3
23	PRU Detection	PRU_DETECT	Detection	IO Expander-P2		Input	High	Low	VDDSHV0	SoC_DVDD3V3
24	PRU Power Switch Enable	PRU_3V3_En	Enable	GPIO0_64	PRG1_PRU0_GPO19	Output	Low	High	VDDSHV2	SoC_DVDD3V3
25	Rpi Power Switch Enable	RPI_PS_5V0_En	Enable	IO Expander-P6		Output	Low	High	VDDSHV0	SoC_DVDD3V3
26	Rpi Power Switch Enable	RPI_PS_3V3_En	Enable	IO Expander-P5		Output	Low	High	VDDSHV0	SoC_DVDD3V3

I2C TREE



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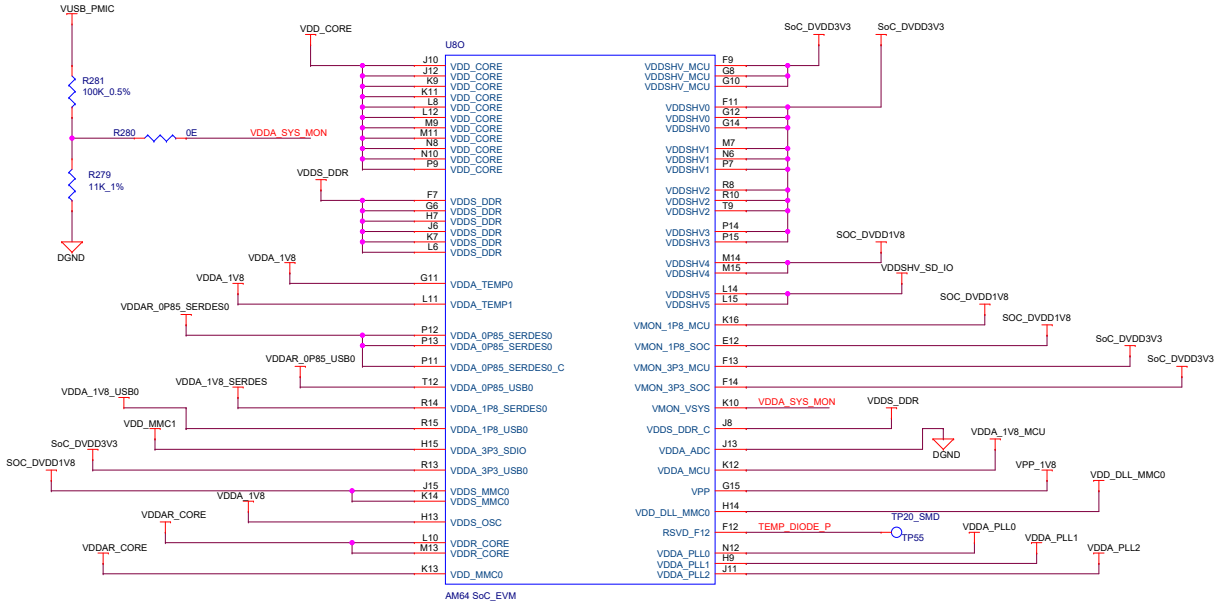
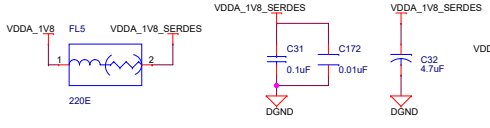
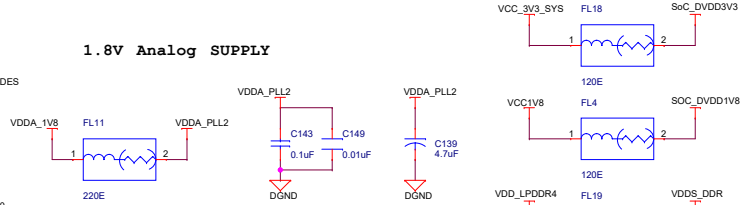
SOC POWER



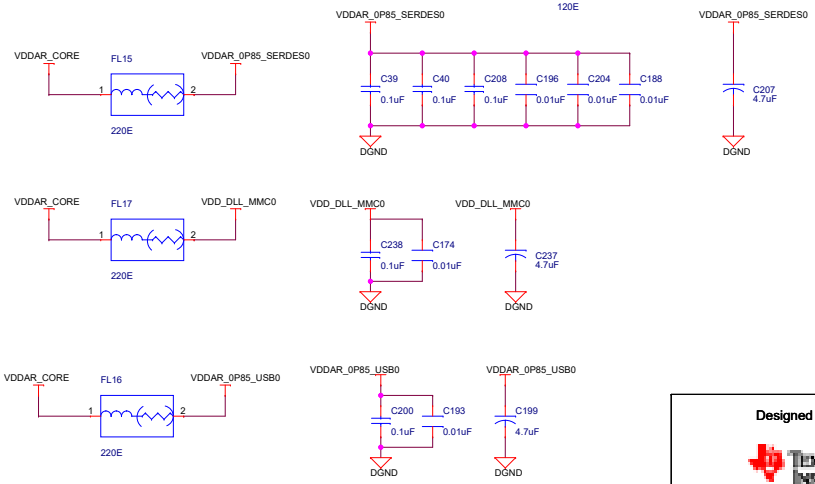
1.8V Analog SUPPLY



1.8V Analog SUPPLY



CORE SUPPLY



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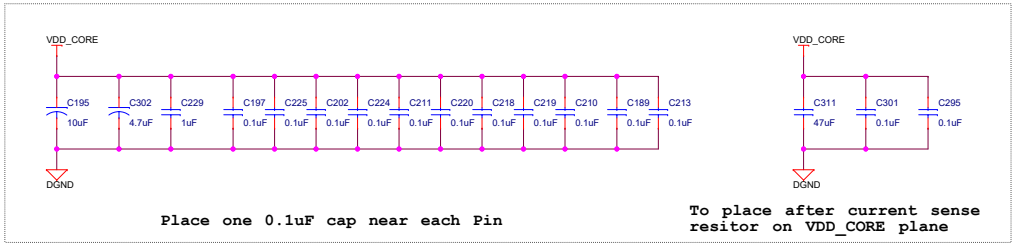
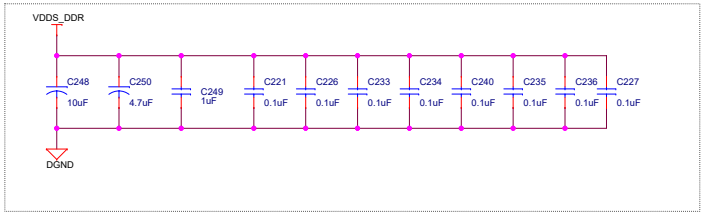
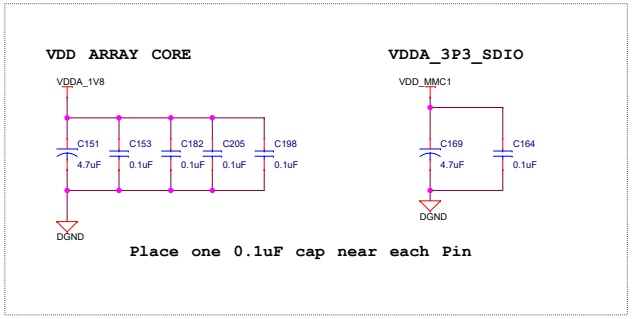
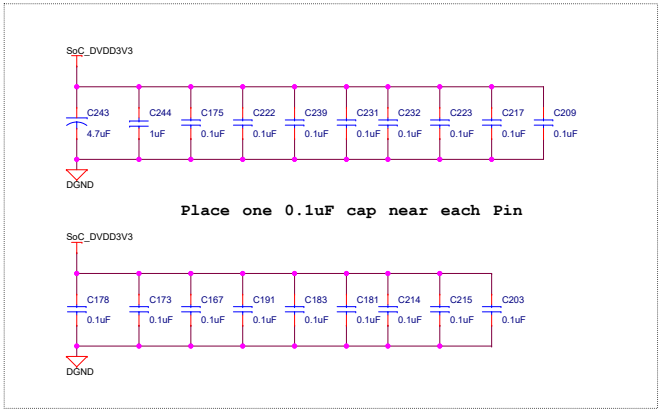
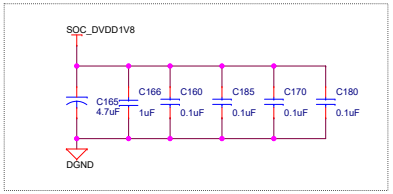
SOC POWER DECAPS

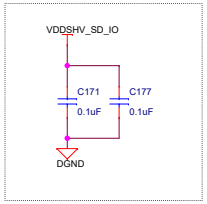




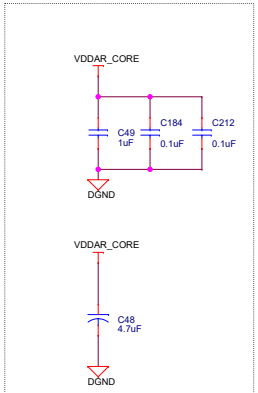








Place one 0.1uF cap near each Pin



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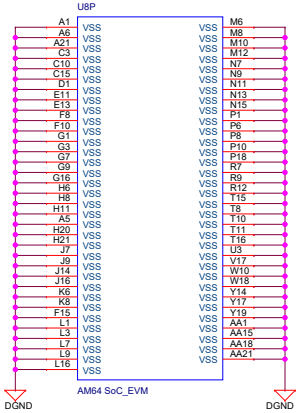
SOC POWER - VSS



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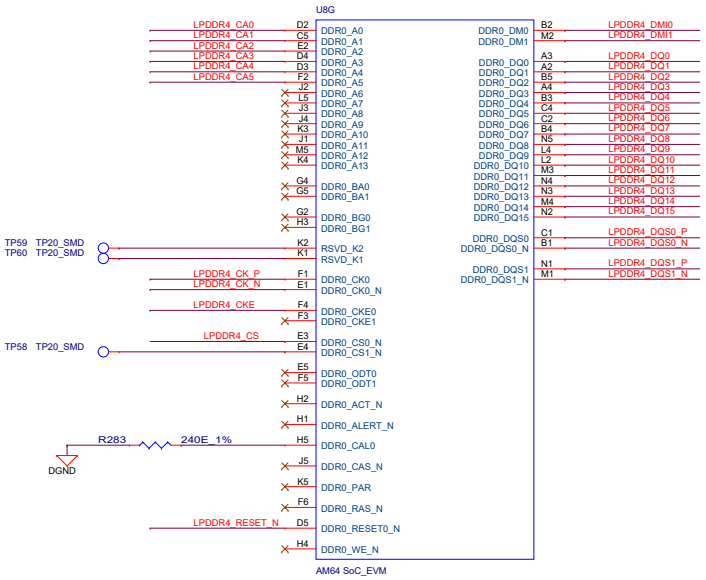
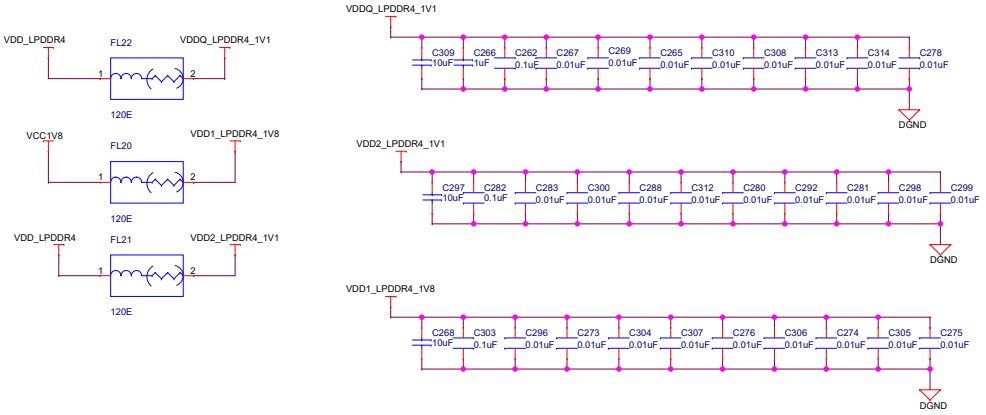
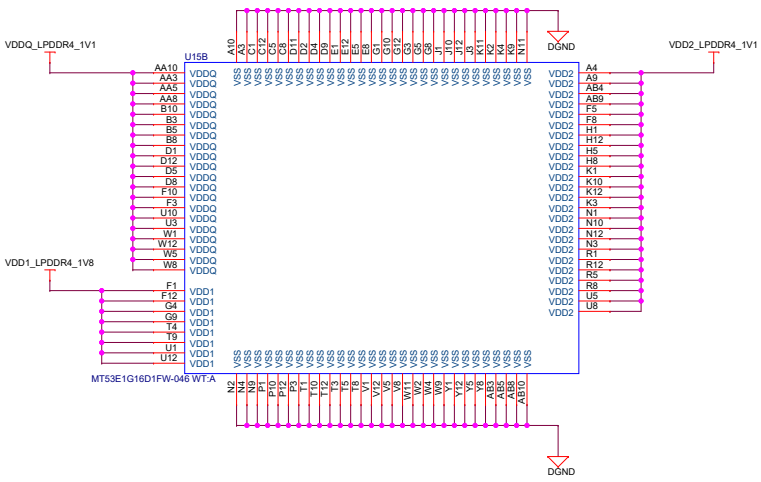
SOC LPDDR4 INTERFACE



LPDDR4 POWER DECAPS



LPDDR4 DEVICE



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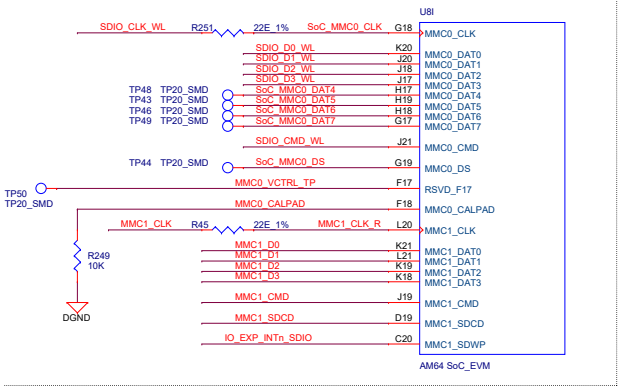
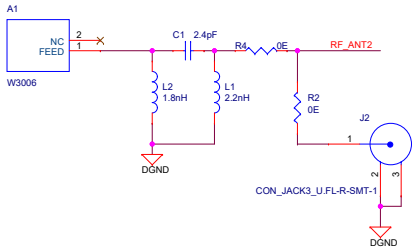
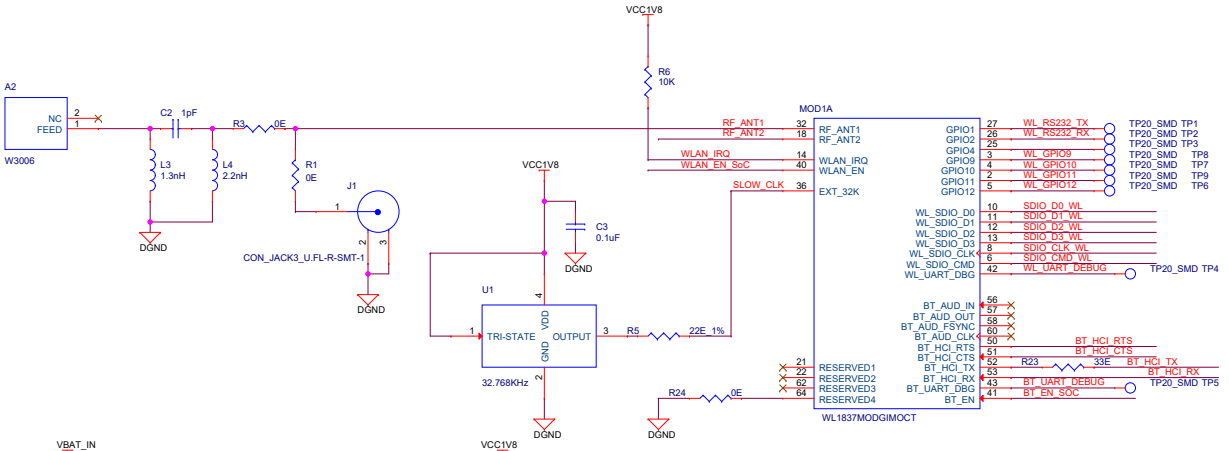
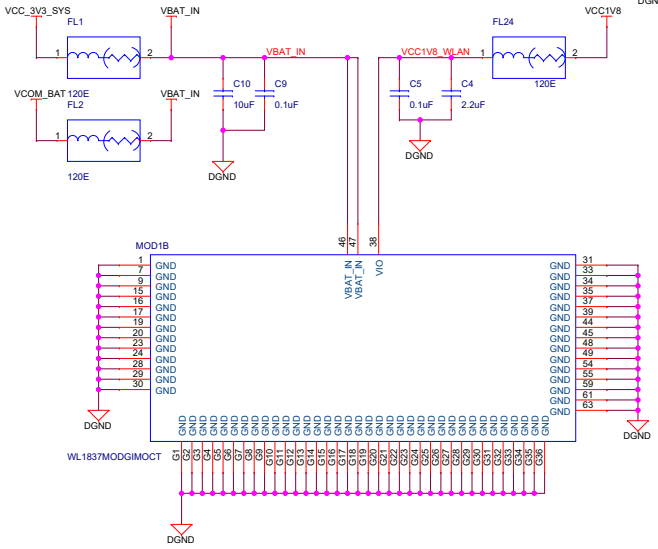
WL1837 MODULE

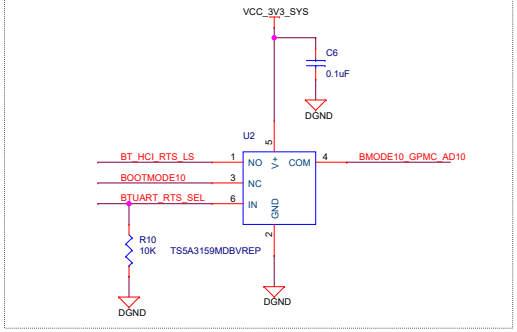




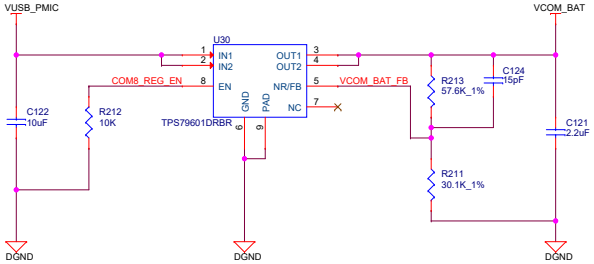




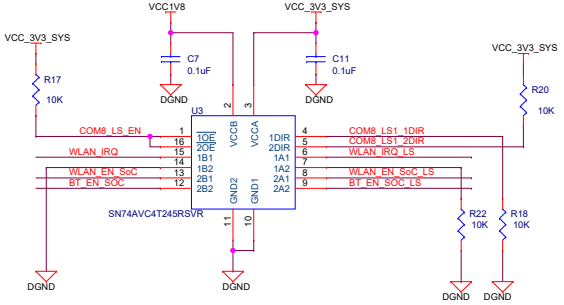
BOOTMODE10/ BTUART RTS SELECT SWITCH



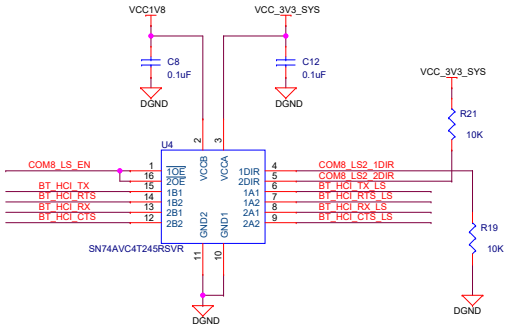
COM8 WILINK POWER

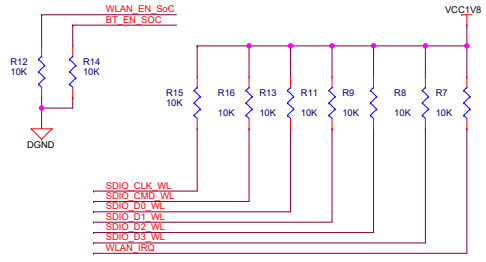


COM8 LEVEL TRANSLATOR-1



COM8 LEVEL TRANSLATOR-2





OFF PAGE CONNECTIONS

27 WLAN_IRQ_LS	WLAN_IRQ_LS
27 WLAN_EN_SoC_LS	WLAN_EN_SoC_LS
27 BT_EN_SOC_LS	BT_EN_SOC_LS
33 BT_HCI_TX_LS	BT_HCI_TX_LS
33 BT_HCI_RX_LS	BT_HCI_RX_LS
28 BT_HCI_CTS_LS	BT_HCI_CTS_LS
27 COM8_LS_EN	COM8_LS_EN
38 IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
18 MMC1_D0	MMC1_D0
18 MMC1_D1	MMC1_D1
18 MMC1_D2	MMC1_D2
18 MMC1_D3	MMC1_D3
18 MMC1_CMD	MMC1_CMD
18 MMC1_SDCD	MMC1_SDCD
18 MMC1_CLK	MMC1_CLK
28 BMODE10_GPMC_AD10	BMODE10_GPMC_AD10
22 BOOTMODE10	BOOTMODE10
27 BTUART_RTS_SEL	BTUART_RTS_SEL
27 COM8_REG_EN	COM8_REG_EN

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Title	WL1837 MODULE	
Size	PROC100 SK-AM64	Rev
C		E2
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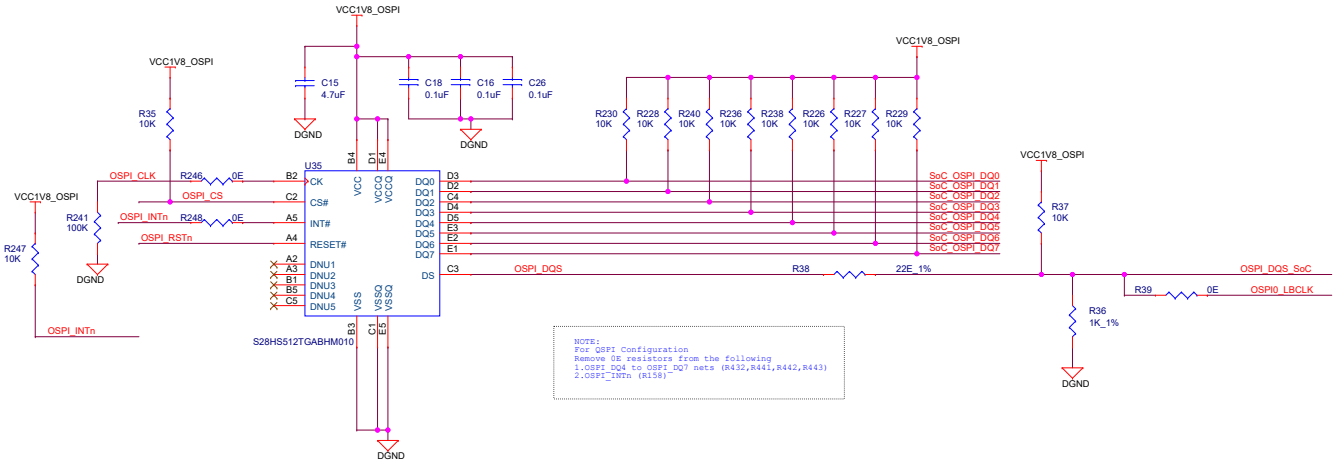
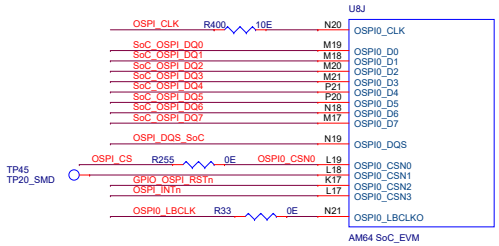
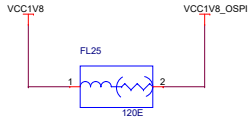
OSPI FLASH

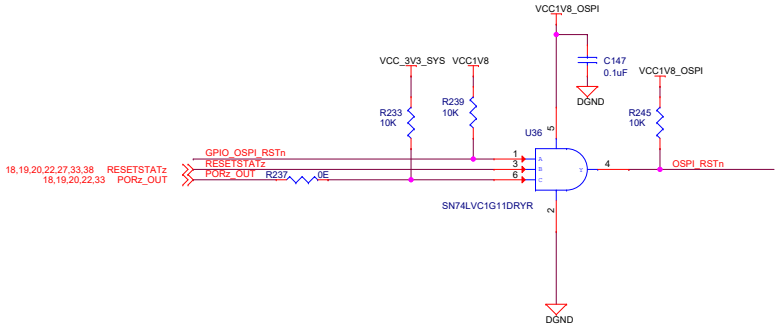


SOC OSPI INTERFACE





OSPI FLASH RESET

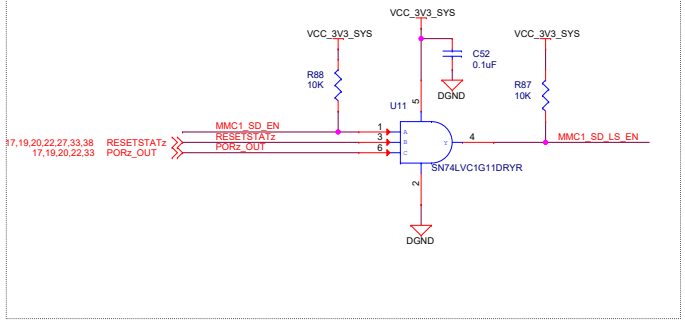


Designed for TI by Mistral Solutions Pvt Ltd

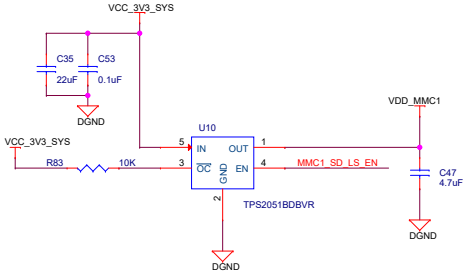
Title	OSPI INTERFACE		
Size	PROC100 SK-AM64		Rev
C			E2
Date:	Tuesday, March 30, 2021	Sheet	17 of 45

SD CARD INTERFACE

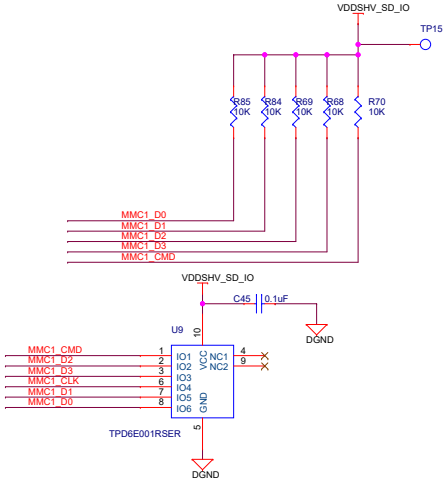
SD CARD RESET

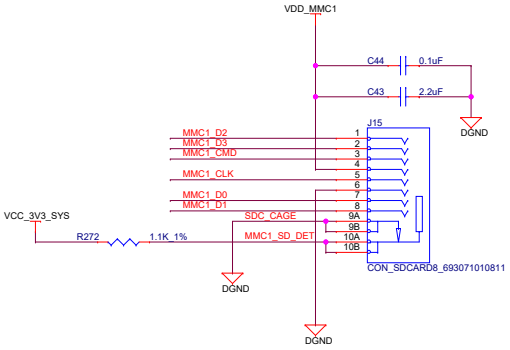


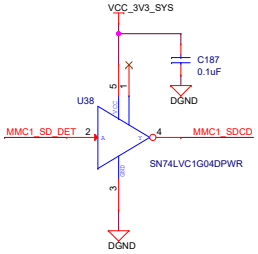
POWER SWITCH



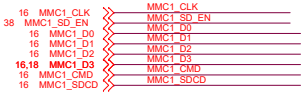
SD CARD CONNECTOR







OFF PAGE CONNECTIONS



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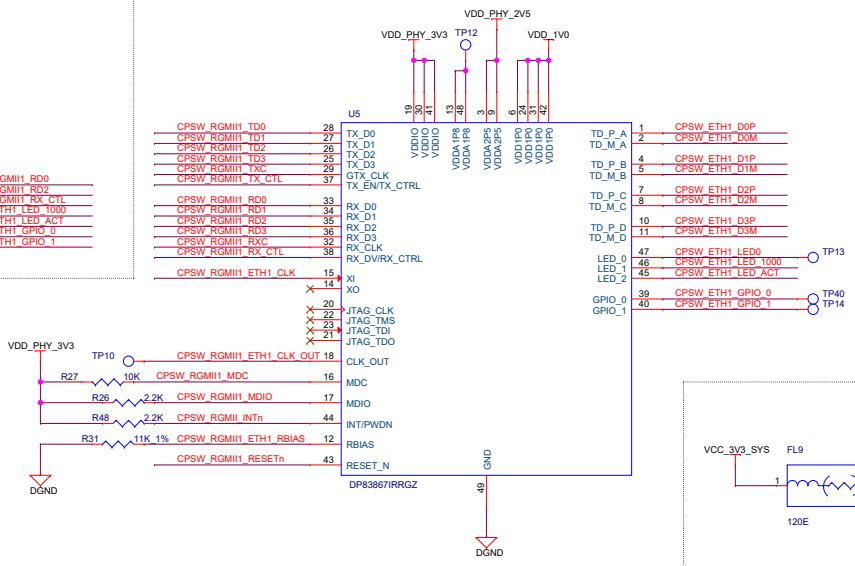
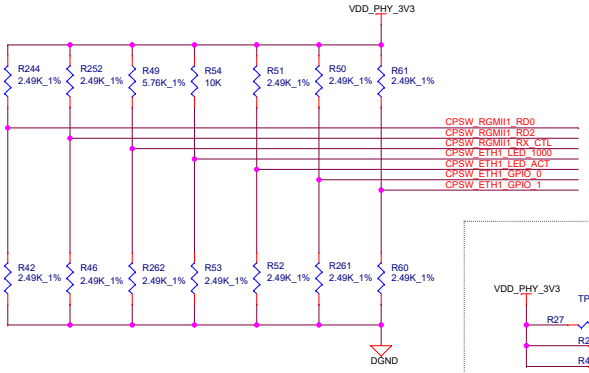
Title	SDCARD INTERFACE	
Size	PROC100 SK-AM64	Rev
C		E2
Date:	Tuesday, March 30, 2021	Sheet 18 of 45

CPSW RGMII 1 - PHY



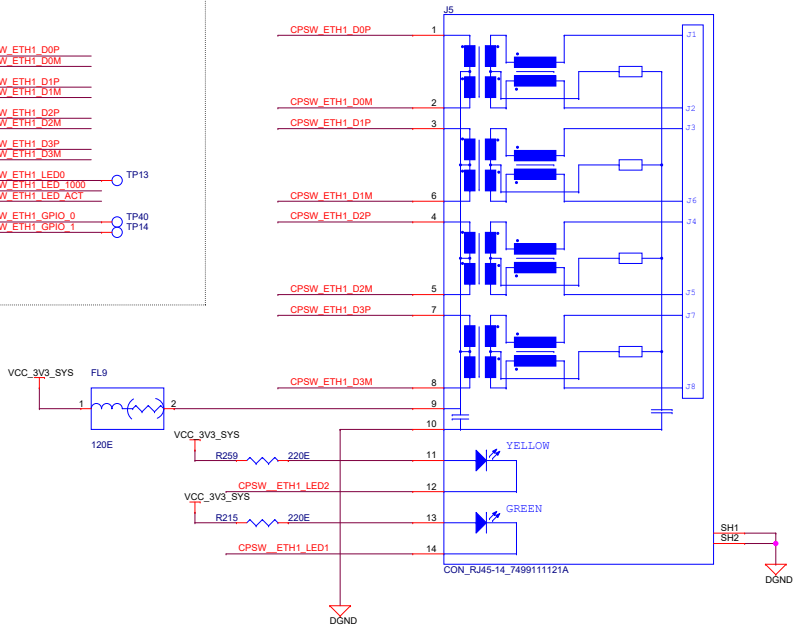
STRAPPING RESISTORS



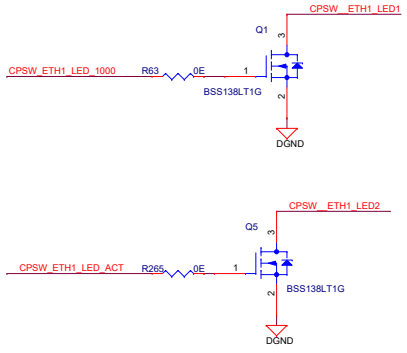

```
PHY ADDRESS = 00000
Auto-negotiation  Enabled
10/100/1000 advertised,  Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
Refer 44 page for strap configuration
```

CPSW_RGMII_INTn/PRU_INTn R295 0E CPSW_RGMII_INTn
CPSW_RGMII2_MDC R28 0E CPSW_RGMII1_MDC
CPSW_RGMII2_MDIO R25 0E CPSW_RGMII1_MDIO

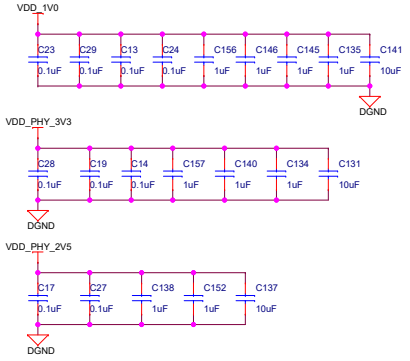
RJ45 CONNECTOR WITH INTEGRATED MAGNETICS



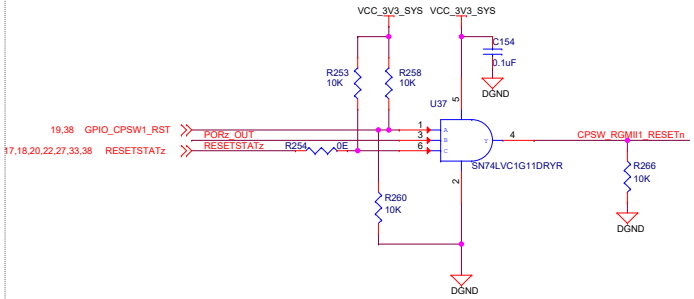
CPSW PHY-1 SPEED AND ACTIVITY LED's DRIVERS



DECAPS



CPSW PHY-1 RESET



OFF PAGE CONNECTIONS

27 CPSW_RGMII1_RD0 — CPSW_RGMII1_RD0
27 CPSW_RGMII1_RD1 — CPSW_RGMII1_RD1
27 CPSW_RGMII1_RD2 — CPSW_RGMII1_RD2
27 CPSW_RGMII1_RD3 — CPSW_RGMII1_RD3
27 CPSW_RGMII1_RXC — CPSW_RGMII1_RXC
27 CPSW_RGMII1_RX_CTL — CPSW_RGMII1_RX_CTL
27 CPSW_RGMII1_TD0 — CPSW_RGMII1_TD0
27 CPSW_RGMII1_TD1 — CPSW_RGMII1_TD1
27 CPSW_RGMII1_TD2 — CPSW_RGMII1_TD2
27 CPSW_RGMII1_TD3 — CPSW_RGMII1_TD3
27 CPSW_RGMII1_TX_CTL — CPSW_RGMII1_TX_CTL
27 CPSW_RGMII1_TXC — CPSW_RGMII1_TXC
17,18,20,22,33 PORz_OUT — PORz_OUT
27,33 CPSW_RGMII_INTn/PRU_INTn — CPSW_RGMII_INTn/PRU_INTn
19,38 GPIO_CPSW1_RST — GPIO_CPSW1_RST
31 CPSW_RGMII1_ETH1_CLK — CPSW_RGMII1_ETH1_CLK
20,27 CPSW_RGMII2_MDC — CPSW_RGMII2_MDC
20,27 CPSW_RGMII2_MDIO — CPSW_RGMII2_MDIO
20 CPSW_RGMII_INTn — CPSW_RGMII_INTn

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_1 ETHERNET PHY	
Size C	PROC100 SK-AM64	Rev E2
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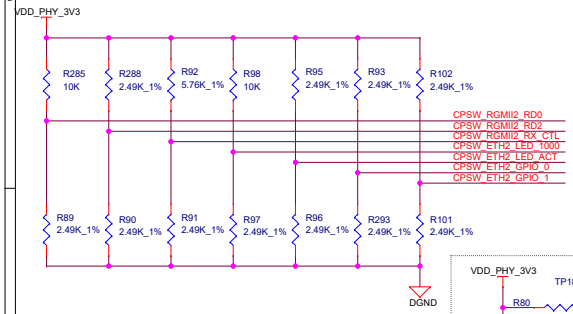
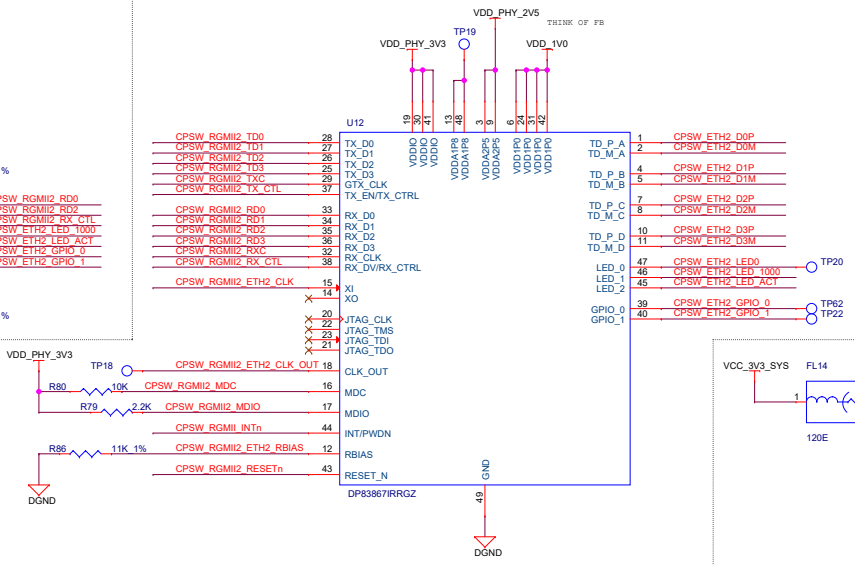
STRAPPING RESISTORS

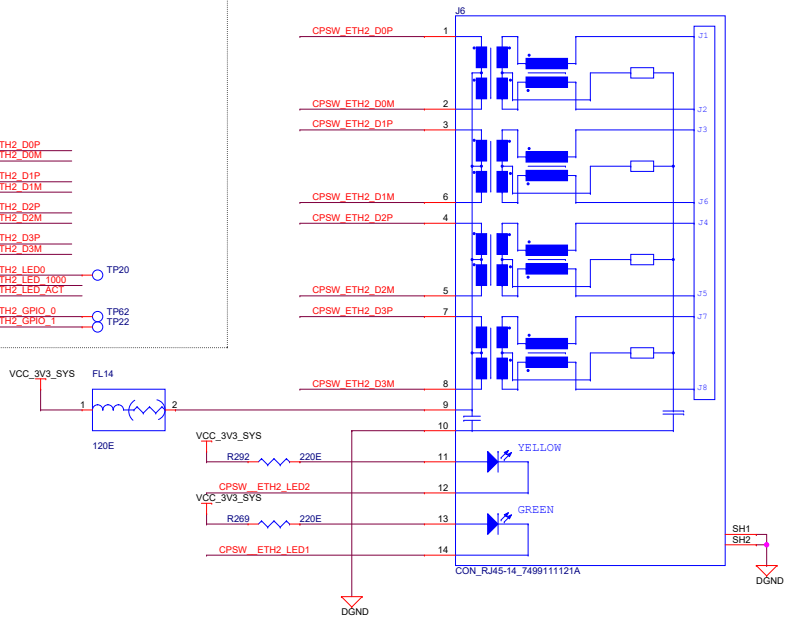


PHY ADDRESS = 00001
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
Refer 44 page for strap configuration

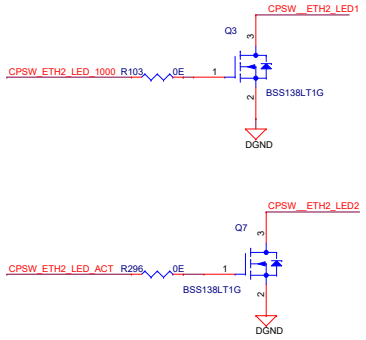
CPSW RGMII 2 - PHY



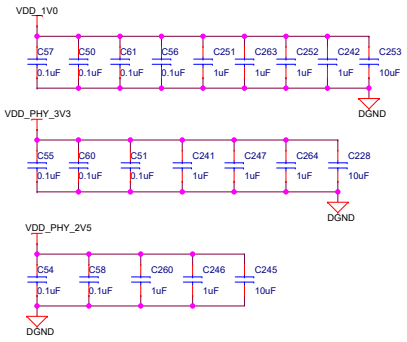
RJ45 CONNECTOR



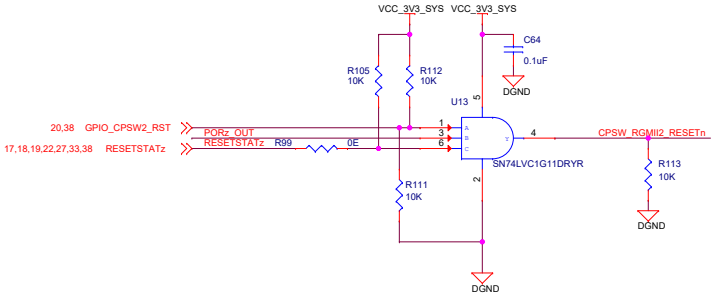
CPSW PHY-2 SPEED AND ACTIVITY LED's DRIVERS



DECAPS



CPSW PHY-2 RESET



OFF PAGE CONNECTIONS

27 CPSW_RGMII2_RD0	CPSW_RGMII2_RD0
27 CPSW_RGMII2_RD1	CPSW_RGMII2_RD1
27 CPSW_RGMII2_RD2	CPSW_RGMII2_RD2
27 CPSW_RGMII2_RD3	CPSW_RGMII2_RD3
27 CPSW_RGMII2_RXC	CPSW_RGMII2_RXC
27 CPSW_RGMII2_RX_CTL	CPSW_RGMII2_RX_CTL
27 CPSW_RGMII2_TD0	CPSW_RGMII2_TD0
27 CPSW_RGMII2_TD1	CPSW_RGMII2_TD1
27 CPSW_RGMII2_TD2	CPSW_RGMII2_TD2
27 CPSW_RGMII2_TD3	CPSW_RGMII2_TD3
27 CPSW_RGMII2_TXC	CPSW_RGMII2_TXC
27 CPSW_RGMII2_TX_CTL	CPSW_RGMII2_TX_CTL
17,18,19,22,33 PORz_OUT	PORz_OUT
20,38 GPIO_CPSW2_RST	GPIO_CPSW2_RST
31 CPSW_RGMII2_ETH2_CLK	CPSW_RGMII2_ETH2_CLK
19,27 CPSW_RGMII2_MDC	CPSW_RGMII2_MDC
19,27 CPSW_RGMII2_MDIO	CPSW_RGMII2_MDIO
19 CPSW_RGMII_INTn	CPSW_RGMII_INTn

Designed for TI by Mistral Solutions Pvt Ltd

Title	CPSW RGMII_2 ETHERNET PHY	
Size	PROC100 SK-AM64	Rev
C		E2
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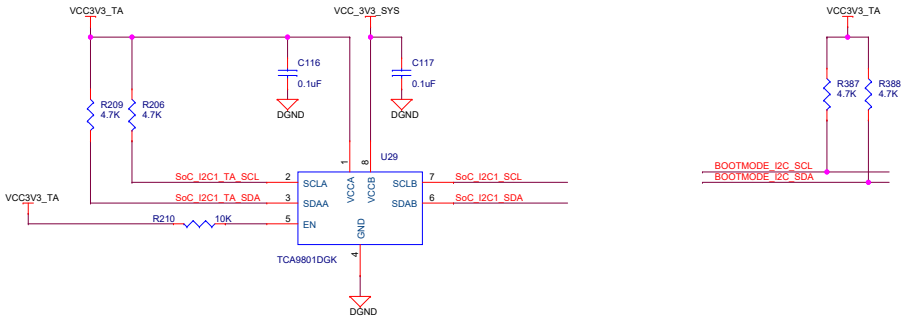
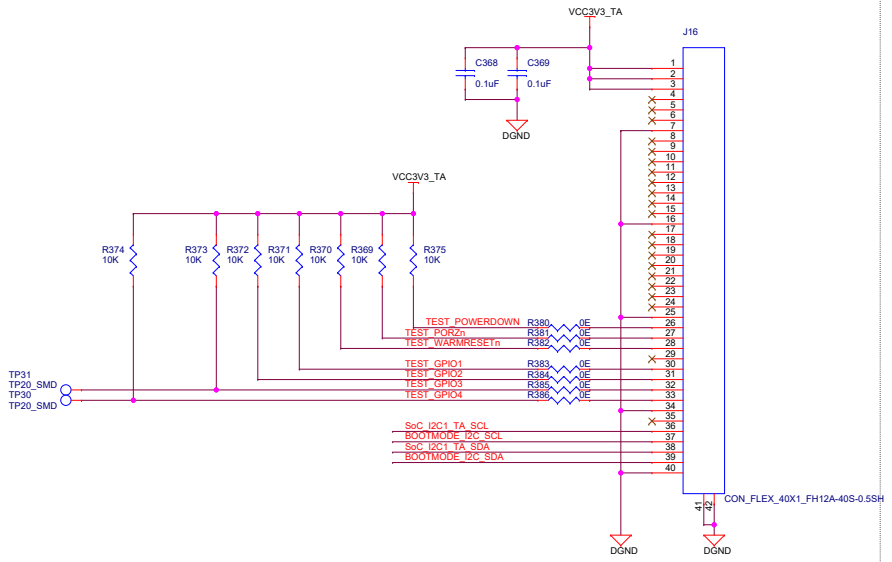
I2C BUS BUFFER



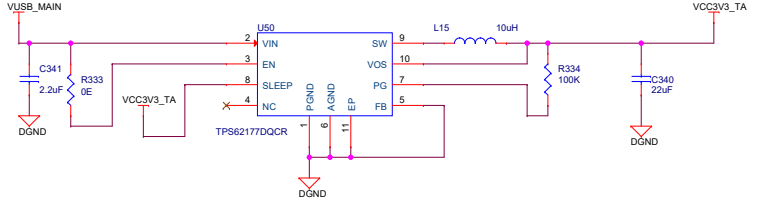
40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO1_59_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to SoC GPIO to Communicate	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

TEST AUTOMATION BOARD POWER



OFF PAGE CONNECTIONS

32,33,36,38	SoC_I2C1_SCL	SoC_I2C1_SCL
32,33,36,38	SoC_I2C1_SDA	SoC_I2C1_SDA
22	BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
22	BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
34	TEST_PORZn	TEST_PORZn
42	TEST_POWERDOWN	TEST_POWERDOWN
34	TEST_WARMRESETn	TEST_WARMRESETn
27	TEST_GPIO2	TEST_GPIO2
22	TEST_GPIO3	TEST_GPIO3
22	TEST_GPIO4	TEST_GPIO4
34	TEST_GPIO1	TEST_GPIO1

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Title	TEST AUTOMATION	
Size	PROC100 SK-AM64	Rev
C		E2
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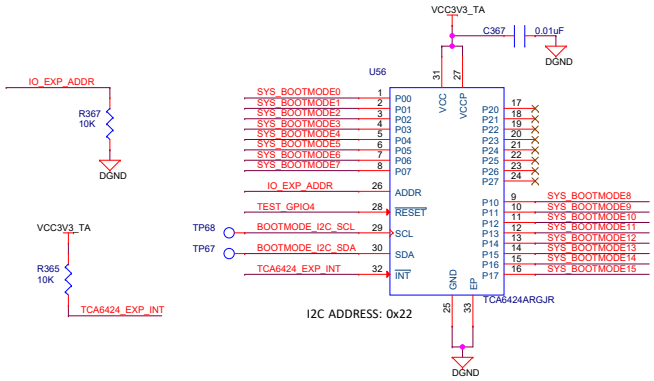
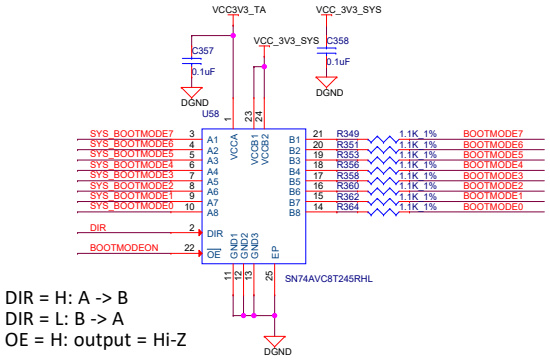
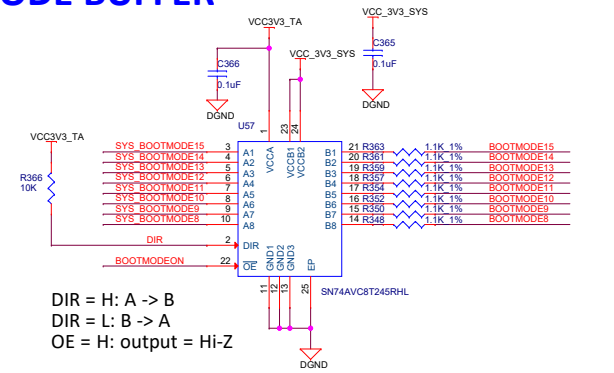
IO EXPANDER



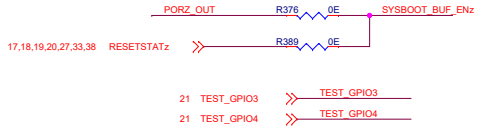
BOOT MODE BUFFER

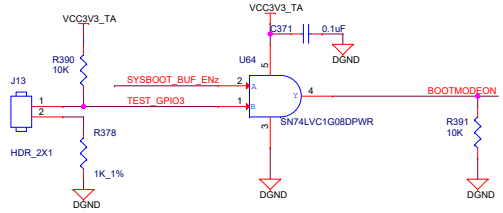


DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z



DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z



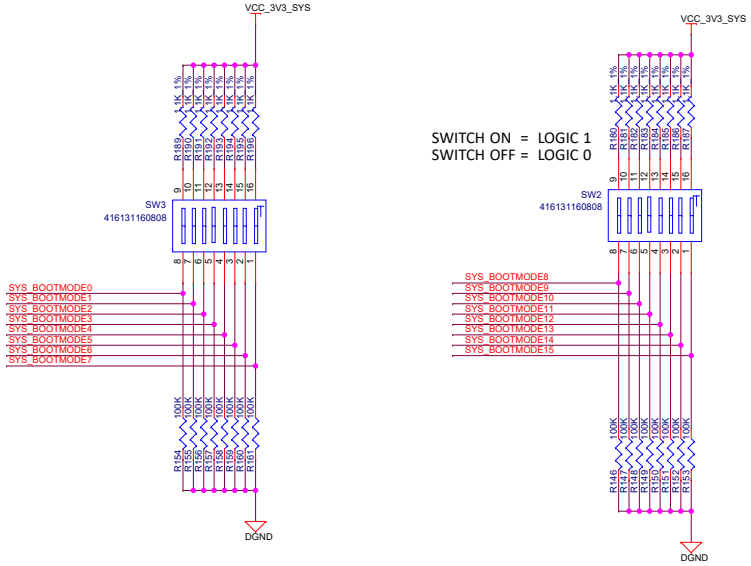


BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. CPSW Ethernet
4. USB Device
5. Ethernet

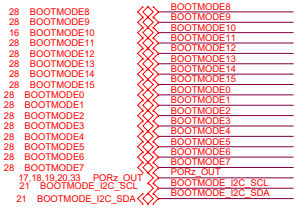
MCU Boot Mode Pins to be Finalized

BOOT MODE SWITCHES



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

OFF PAGE CONNECTIONS



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Title	BOOT MODE BUFFER & SWITCHES	
Size	PROC100 SK-AM64	Rev
C		E2
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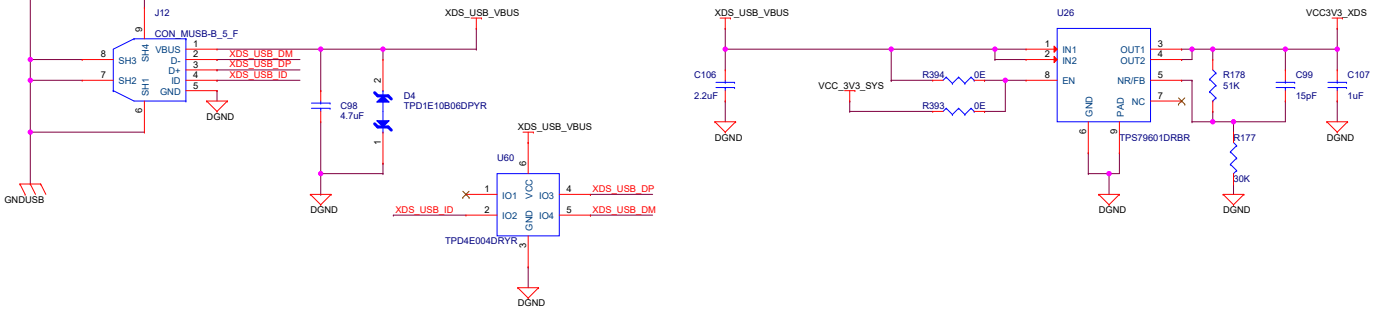
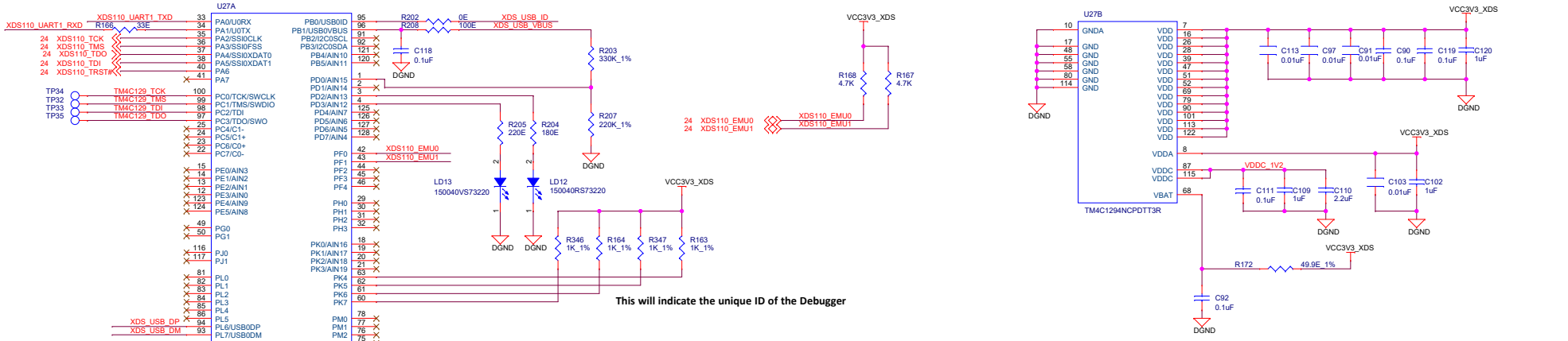
XDS110 POWER

USB Connector

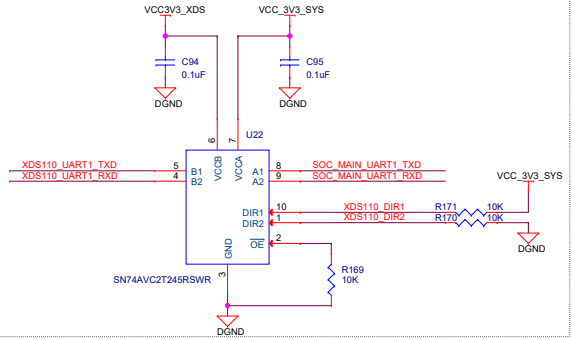


XDS110 DEBUGGER



This will indicate the unique ID of the Debugger

XDS110 LEVEL TRANSLATOR



OFF PAGE CONNECTIONS

SOC_MAIN_UART1_RXD — SOC_MAIN_UART1_RXD 33
SOC_MAIN_UART1_TXD — SOC_MAIN_UART1_TXD 33

Designed for TI by Mistral Solutions Pvt Ltd

Title	XDS110 DEBUGGER		
Size	PROC100 SK-AM64		Rev
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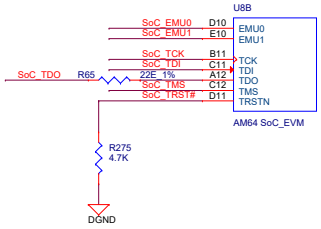
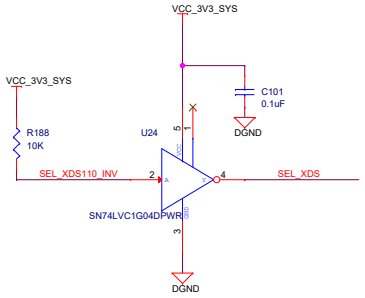
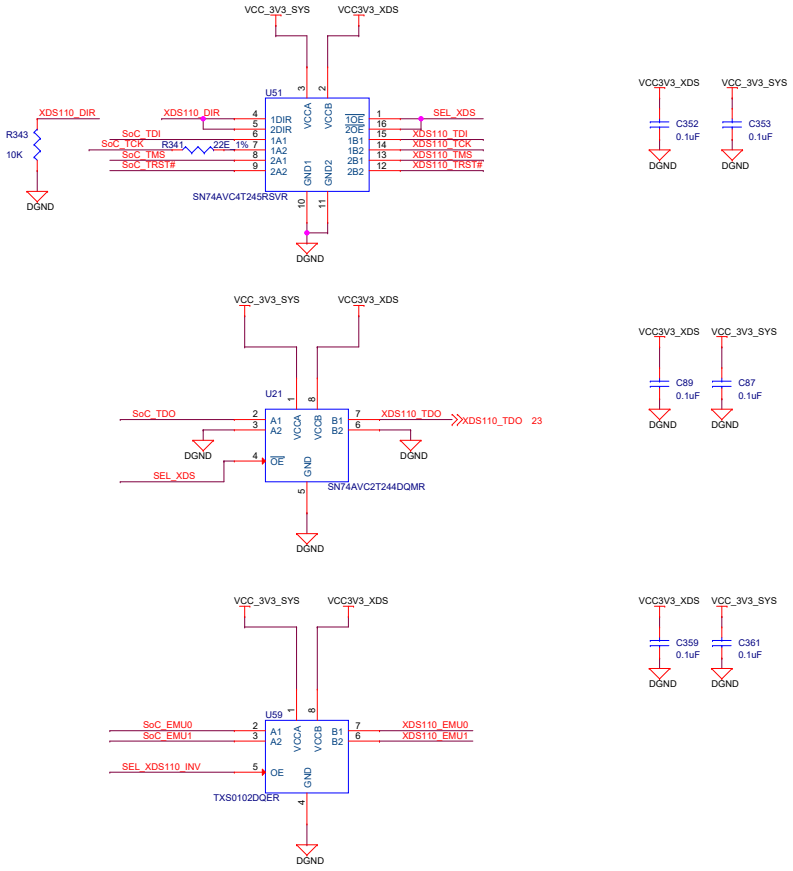
JTAG SoC SECTION



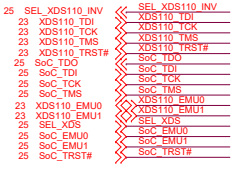
INVERTER



BUFFER XDS110



OFF PAGE CONNECTIONS



Designed for TI by Mistral Solutions Pvt Ltd

Title	JTAG BUFFER	
Size	PROC100 SK-AM64	Rev
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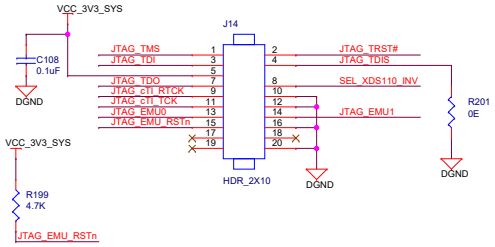
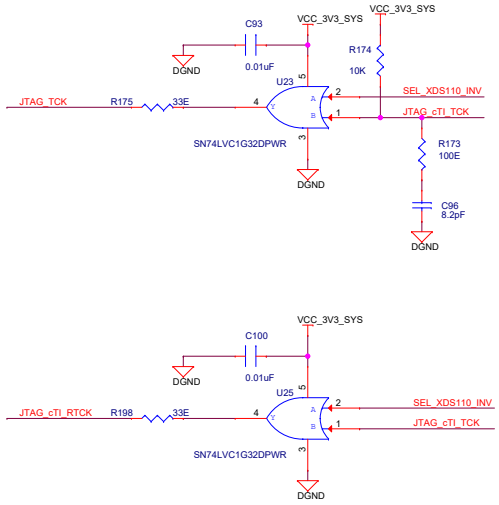
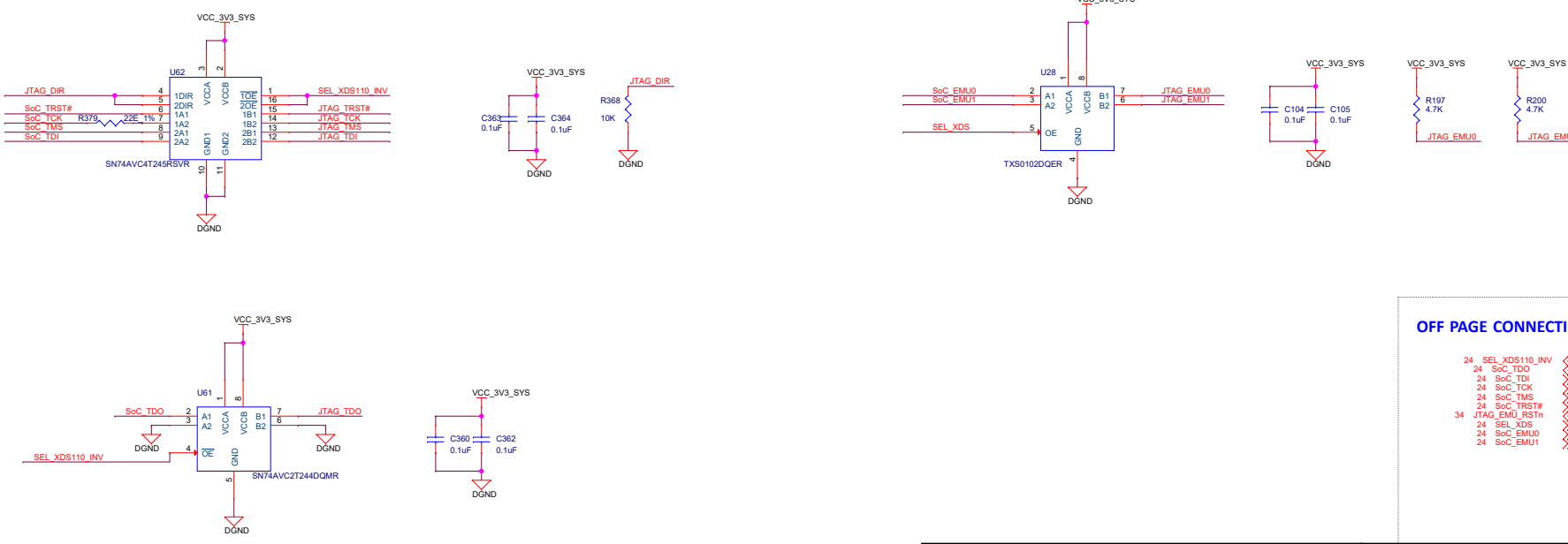
JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER



20 PIN JTAG BUFFERS



OFF PAGE CONNECTIONS

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Title	JTAG 20 PIN cTI CONNECTOR	
Size	PROC100 SK-AM64	Rev
C		E2
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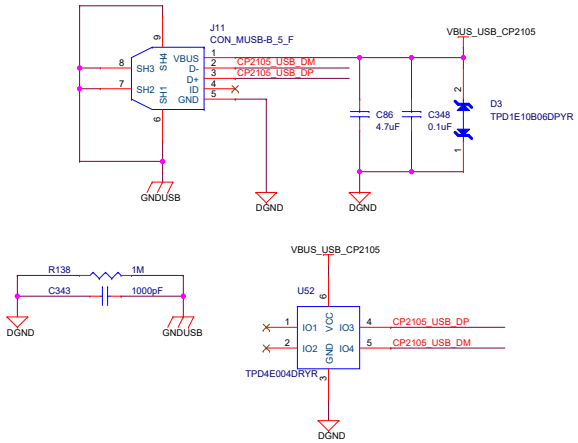
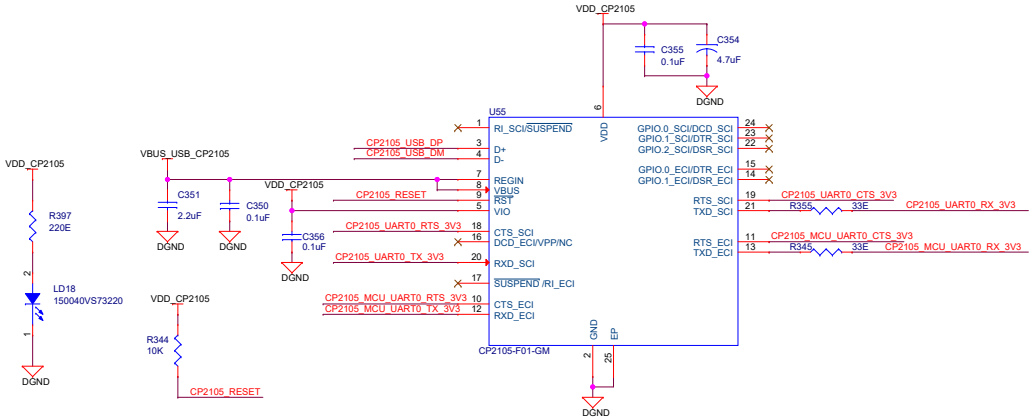
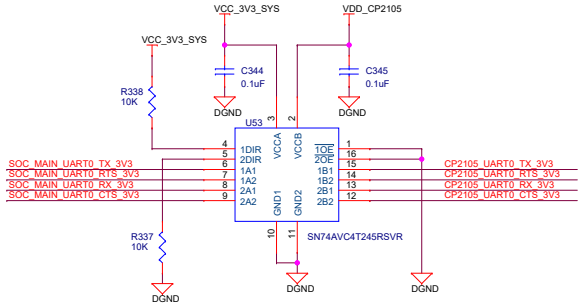
USB Micro B CONNECTOR

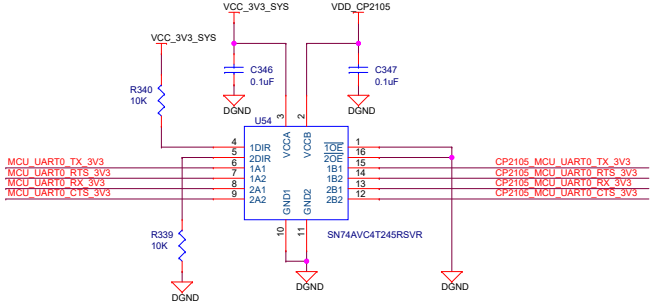


USB TO DUAL UART BRIDGE



CP2105 LEVEL TRANSLATOR





OFF PAGE CONNECTIONS

SOC_MAIN_UART0_RX_3V3 → SOC_MAIN_UART0_RX_3V3 33
SOC_MAIN_UART0_TX_3V3 → SOC_MAIN_UART0_TX_3V3 33
SOC_MAIN_UART0_RTS_3V3 → SOC_MAIN_UART0_RTS_3V3 33
SOC_MAIN_UART0_CTS_3V3 → SOC_MAIN_UART0_CTS_3V3 33

MCU_UART0_RX_3V3 → MCU_UART0_RX_3V3 33
MCU_UART0_TX_3V3 → MCU_UART0_TX_3V3 33
MCU_UART0_RTS_3V3 → MCU_UART0_RTS_3V3 33
MCU_UART0_CTS_3V3 → MCU_UART0_CTS_3V3 33

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Title	CP2105 UART TO USB BRIDGE	
Size	PROC100 SK-AM64	Rev
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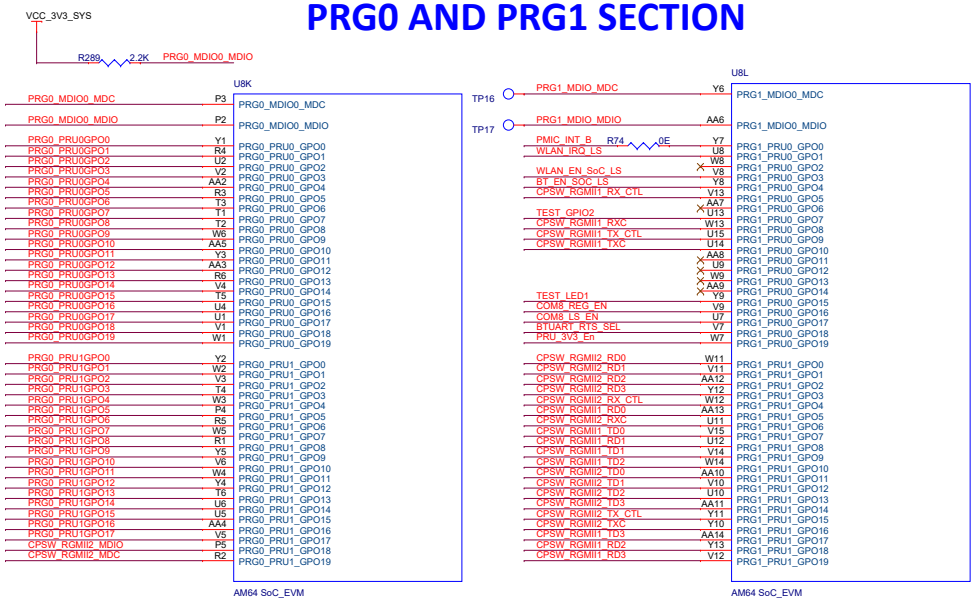
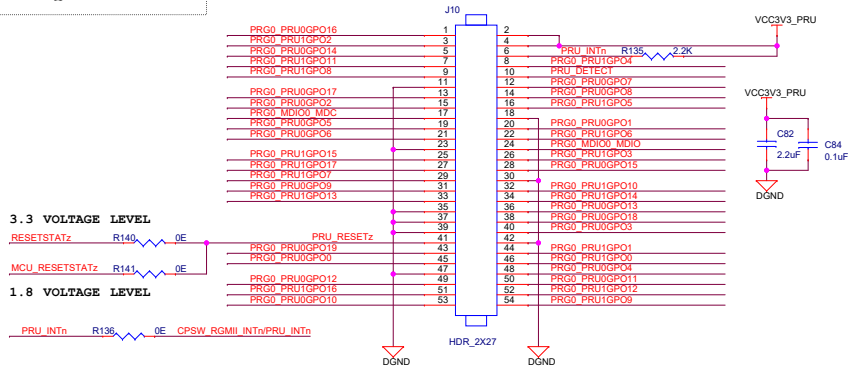
PRG0 AND PRG1 SECTION



PRU CONNECTOR

FOR LAUNCHPAD HEADER
USE PART SSQ-127-23-L-D



OFF PAGE CONNECTIONS

MCU_RESETSTATz
CPSW_RGMII1_RD0
CPSW_RGMII1_RD1
CPSW_RGMII1_RD2
CPSW_RGMII1_RD3
CPSW_RGMII1_RXC
CPSW_RGMII1_RX_CTL
CPSW_RGMII2_RD0
CPSW_RGMII2_RD1
CPSW_RGMII2_RD2
CPSW_RGMII2_RD3
CPSW_RGMII2_RXC
CPSW_RGMII2_RX_CTL
CPSW_RGMII2_TD0
CPSW_RGMII2_TD1
CPSW_RGMII2_TD2
CPSW_RGMII2_TD3
CPSW_RGMII2_TXC
CPSW_RGMII2_TX_CTL
CPSW_RGMII1_TD0
CPSW_RGMII1_TD1
CPSW_RGMII1_TD2
CPSW_RGMII1_TD3
CPSW_RGMII1_TX_CTL
CPSW_RGMII1_TXC
PRU_DETECT
CPSW_RGMII_INTn/PRU_INTn
RESETSTATz
WLAN_IRQ_LS
WLAN_EN_SoC_LS
BT_EN_SOC_LS
PMIC_INT_B
COM8_LS_EN
CPSW_RGMII2_MDC
CPSW_RGMII2_MDIO
COM8_REG_EN
BTUART_RTS_SEL
TEST_LED1
TEST_GPIO2

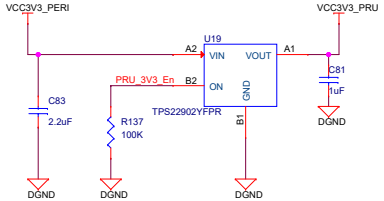
NOTE:

AM64x Starter Kit shall not be powered through the 3V3 pins on the PRU Connector.

PRU Connector I/O are not fail-safe and shall not be driven when AM64x Starter Kit is not powered.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

POWER SWITCH FOR 3.3V TO PRU CONNECTOR



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Title	PRU CONNECTOR	
Size	PROC100 SK-AM64	Rev
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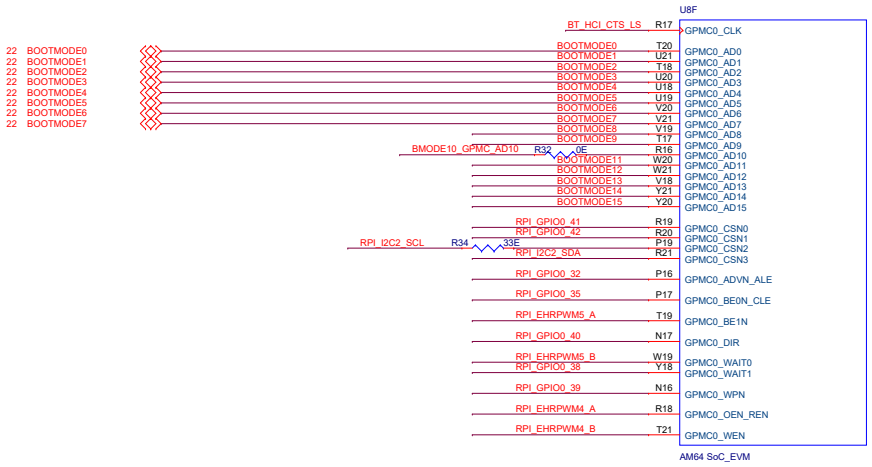
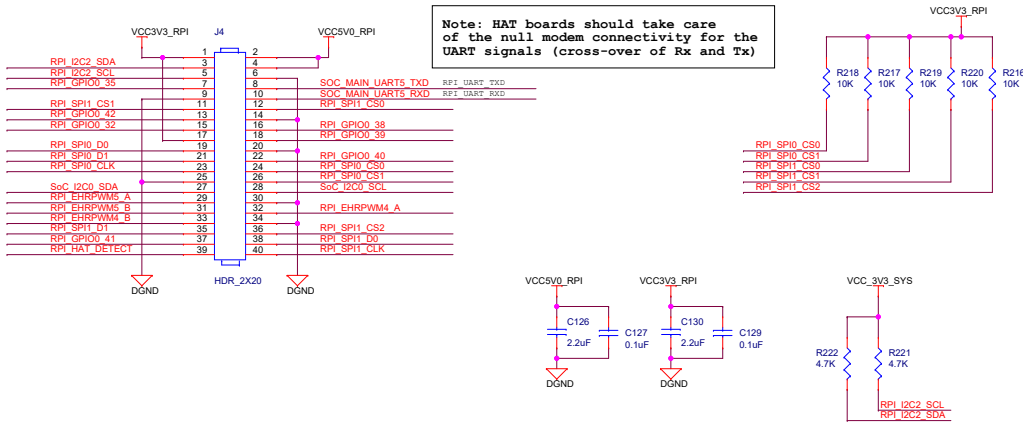
GPMC SECTION



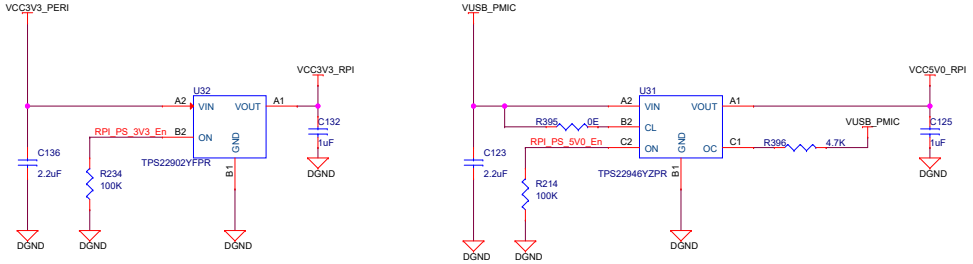
USER EXPANSION CONNECTOR



Note: This connector is compatible to GPIO Expansion Header (J8) found on the Raspberry Pi Boards

Note: Raspberry Pi is the trademark / wordmark of Raspberry Pi Foundation

POWER SWITCH FOR USER EXPANSION CONNECTOR



NOTE:

AM64x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM64x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

OFF PAGE CONNECTIONS

RPI_HAT_DETECT	RPI_HAT_DETECT 38
RPI_SPI1_CLK	RPI_SPI1_CLK 33
RPI_SPI1_D0	RPI_SPI1_D0 33
RPI_SPI1_D1	RPI_SPI1_D1 33
RPI_SPI1_CS0	RPI_SPI1_CS0 33
RPI_SPI1_CS1	RPI_SPI1_CS1 33
RPI_SPI1_CS2	RPI_SPI1_CS2 33
RPI_SPI0_CLK	RPI_SPI0_CLK 33
RPI_SPI0_D0	RPI_SPI0_D0 33
RPI_SPI0_D1	RPI_SPI0_D1 33
RPI_SPI0_CS0	RPI_SPI0_CS0 33
RPI_SPI0_CS1	RPI_SPI0_CS1 33
SoC_I2C0_SCL	SoC_I2C0_SCL 33,37,41,42
SoC_I2C0_SDA	SoC_I2C0_SDA 33,37,41,42
BT_HCI_CTS_LS	BT_HCI_CTS_LS 16
BOOTMODE8	BOOTMODE8 22
BOOTMODE9	BOOTMODE9 22
BOOTMODE11	BOOTMODE11 22
BOOTMODE12	BOOTMODE12 22
BOOTMODE13	BOOTMODE13 22
BOOTMODE14	BOOTMODE14 22
BOOTMODE15	BOOTMODE15 22
SOC_MAIN_UART5_RXD	SOC_MAIN_UART5_RXD 33
SOC_MAIN_UART5_TXD	SOC_MAIN_UART5_TXD 33
RPI_PS_3V3_En	RPI_PS_3V3_En 38
RPI_PS_5V0_En	RPI_PS_5V0_En 38
BMODE10_GPMC_AD10	BMODE10_GPMC_AD10 16

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Title	USER EXPANSION CONNECTOR	
Size	PROC100 SK-AM64	Rev
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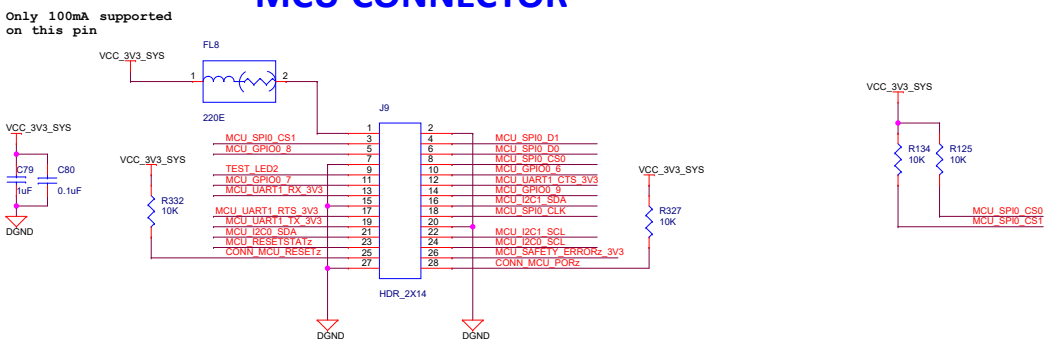
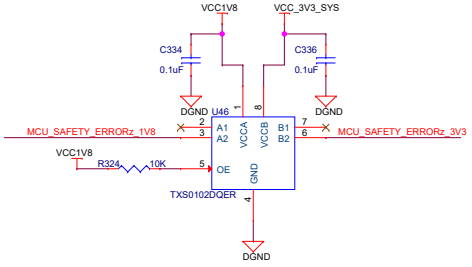
MCU CONNECTOR



LEVEL TRANSLATOR



OFF PAGE CONNECTIONS

34	CONN_MCU_RESETz	CONN_MCU_RESETz
34	CONN_MCU_PORz	CONN_MCU_PORz
33	MCU_SPI0_CS1	MCU_SPI0_CS1
33	MCU_GPIO0_8	MCU_GPIO0_8
33,35	TEST_LED2	TEST_LED2
33	MCU_GPIO0_7	MCU_GPIO0_7
33	MCU_UART1_RX_3V3	MCU_UART1_RX_3V3
33	MCU_UART1_RTS_3V3	MCU_UART1_RTS_3V3
33	MCU_UART1_TX_3V3	MCU_UART1_TX_3V3
33	MCU_I2C0_SDA	MCU_I2C0_SDA
27,33	MCU_RESETSTATz	MCU_RESETSTATz
33	MCU_SPI0_D1	MCU_SPI0_D1
33	MCU_SPI0_D0	MCU_SPI0_D0
33	MCU_SPI0_CS0	MCU_SPI0_CS0
33,34	MCU_GPIO0_6	MCU_GPIO0_6
33	MCU_UART1_CTS_3V3	MCU_UART1_CTS_3V3
33	MCU_GPIO0_9	MCU_GPIO0_9
33	MCU_I2C1_SDA	MCU_I2C1_SDA
33	MCU_SPI0_CLK	MCU_SPI0_CLK
33	MCU_I2C1_SCL	MCU_I2C1_SCL
33	MCU_I2C0_SCL	MCU_I2C0_SCL
33	MCU_SAFETY_ERRORz_1V8	MCU_SAFETY_ERRORz_1V8

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Title	MCU CONNECTOR	
Size	PROC100 SK-AM64	Rev
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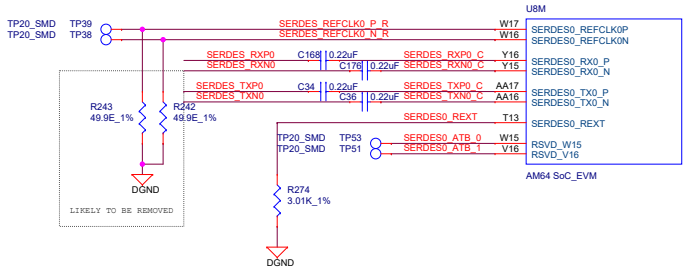
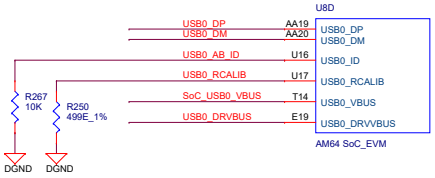
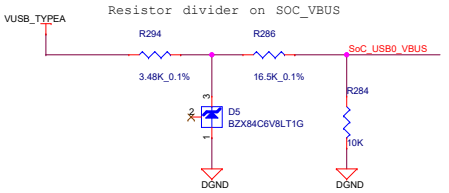
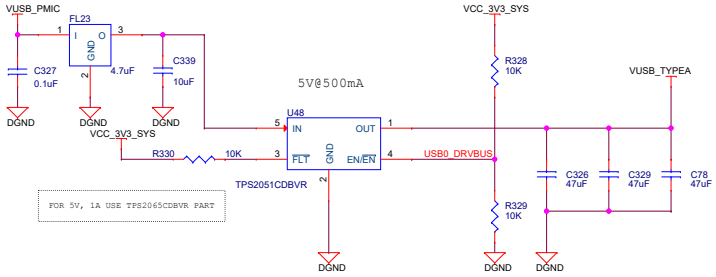
USB 3.0 INTERFACE



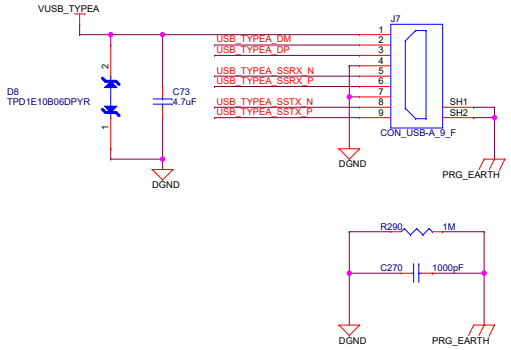




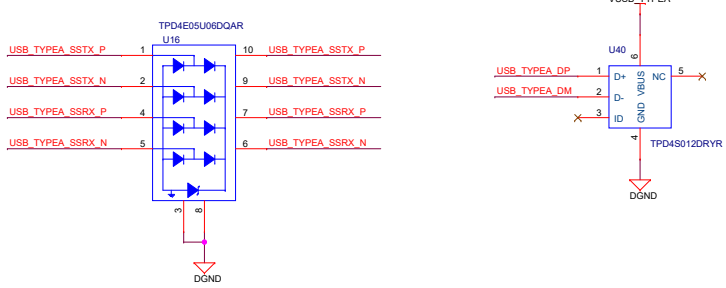
5V Power switch for USB 3.0 Device



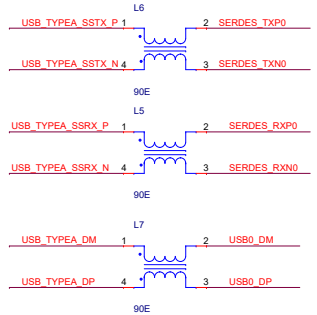
Type-A Connector



ESD DIODES



CHOKE



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Title	USB 3.0 INTERFACE	
Size C	PROC100 SK-AM64	Rev E2
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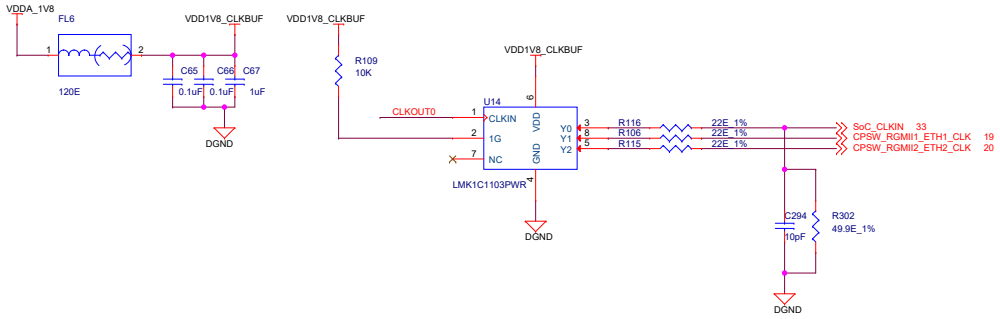
ETHERNET PHY CLOCK BUFFER



OFF PAGE CONNECTIONS

33,39 CLKOUT0 <<— CLKOUT0

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Title	ETHERNET PHY CLOCK BUFFER	
Size: C	PROC100 SK-AM64	Rev: E2
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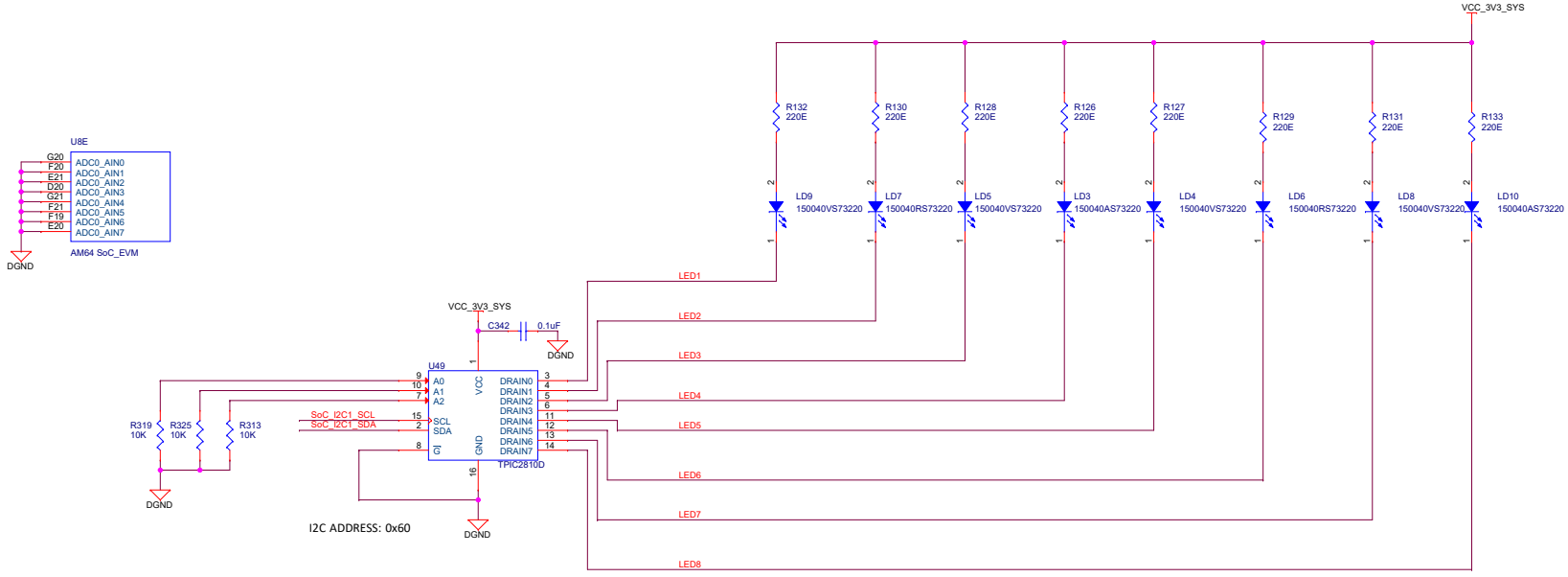
INDUSTRIAL COMMUNICATION LED's



OFF PAGE CONNECTIONS

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Title	INDUSTRIAL COMMUNICATION LED's	
Size C	PROC100 SK-AM64	Rev E2
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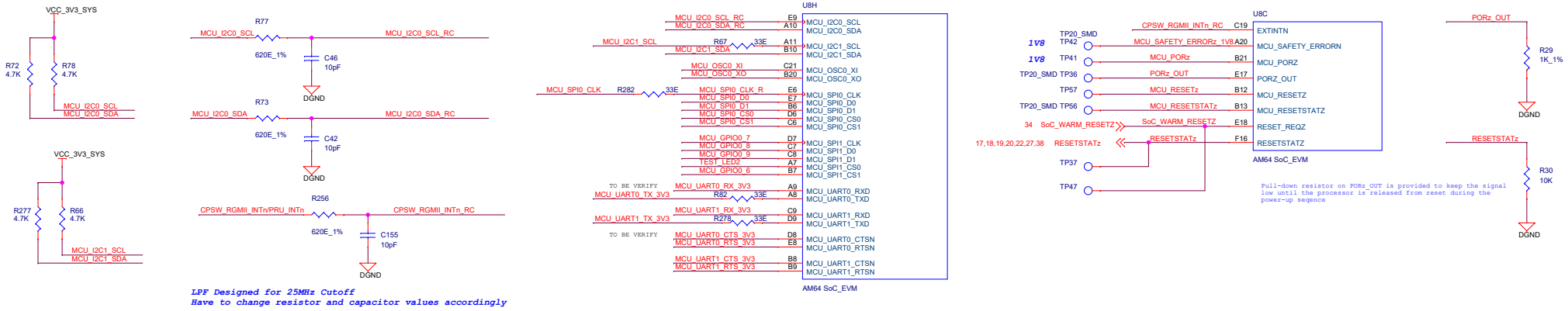
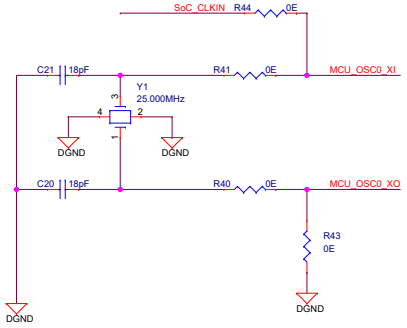
MCU_GENERAL

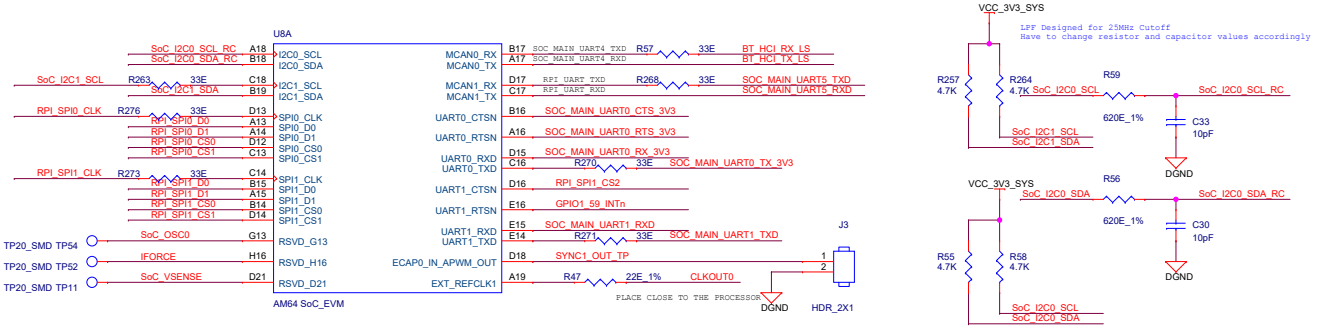


CRYSTAL

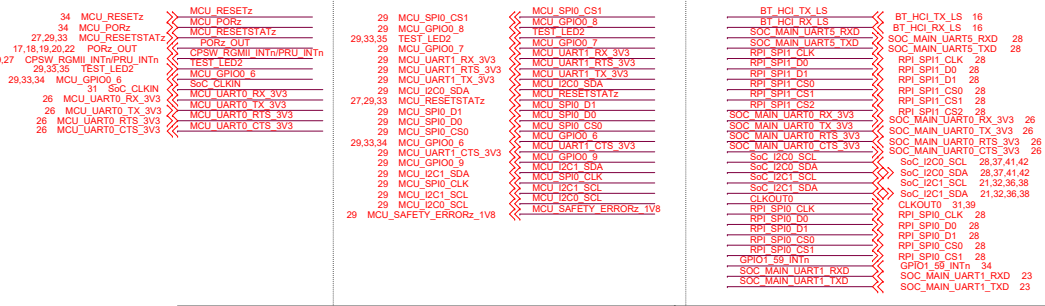
Only Footprint option to mount the Oscillator is provided.
By default the part is not mounted on the board.



SoC MAIN DOMAIN



OFF PAGE CONNECTIONS



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Title	SoC MAIN AND MCU DOMAIN	
Size C	PROC100 SK-AM64	Rev E2
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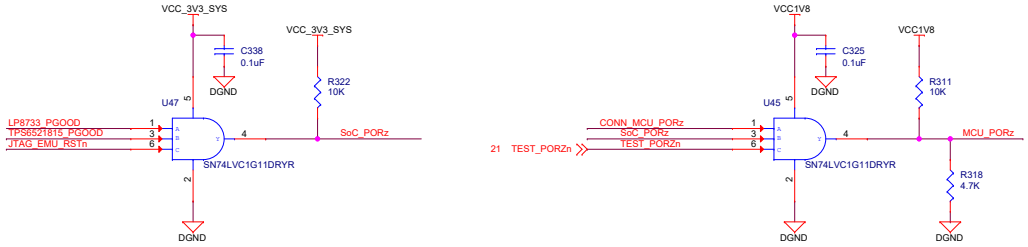
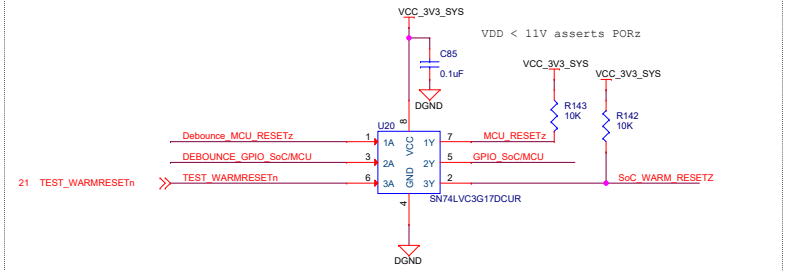
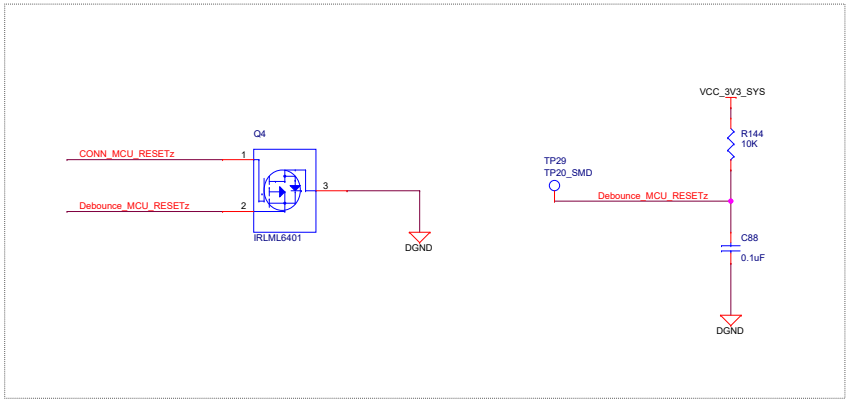
POR

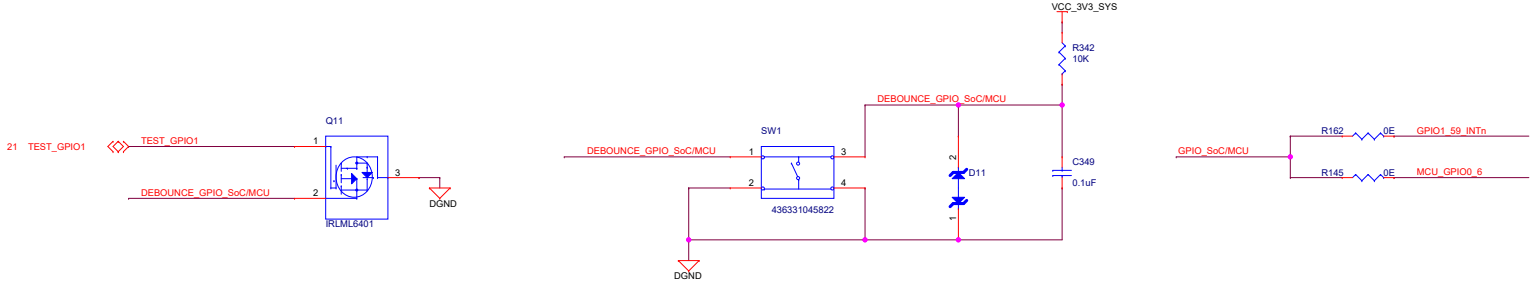


DEBOUNCE CIRCUIT

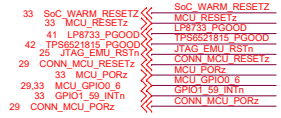




USER SWITCH BUTTON



OFF PAGE CONNECTIONS



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Title	RESET CIRCUIT	
Size	PROC100 SK-AM64	Rev
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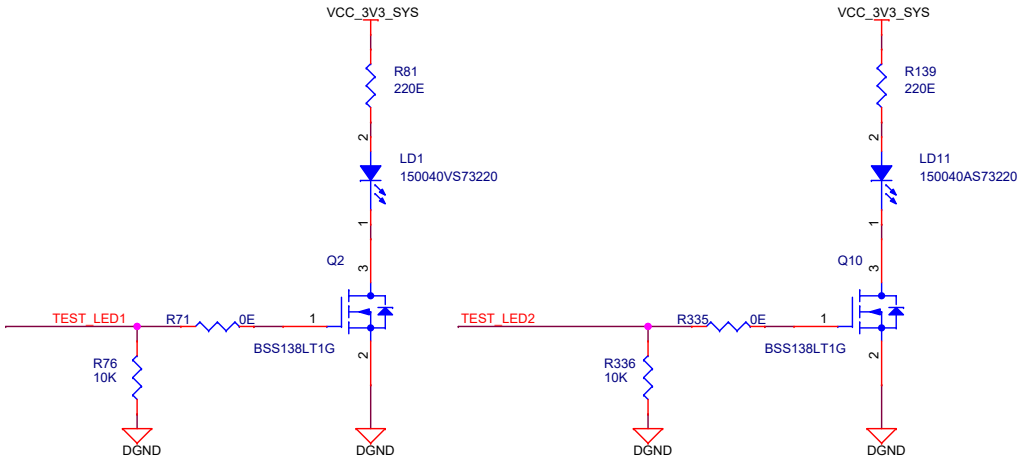
USER TEST LED's



OFF PAGE CONNECTIONS

TEST_LED1
TEST_LED2

TEST_LED1 27
TEST_LED2 29,33

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Title	USER TEST LED's	
Size: B	PROC100 SK-AM64	Rev: E2
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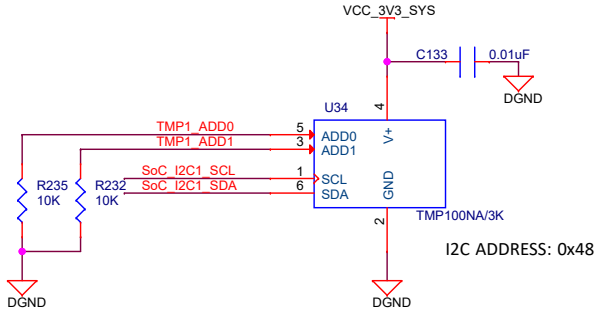
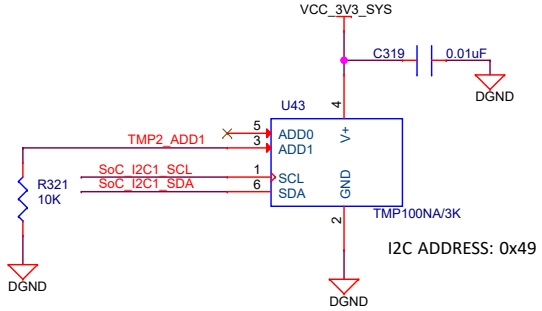
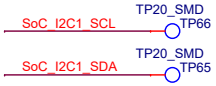
TEMPERATURE SENSORS



NOTE: PLACE TEMP SENSOR CLOSE TO SoC



NOTE: PLACE TEMP SENSOR CLOSE TO LPDDR4



OFF PAGE CONNECTIONS

Designed for TI by Mistral Solutions Pvt Ltd

Title	TEMPERATURE SENSORS	
Size: B	PROC100 SK-AM64	Rev: E2
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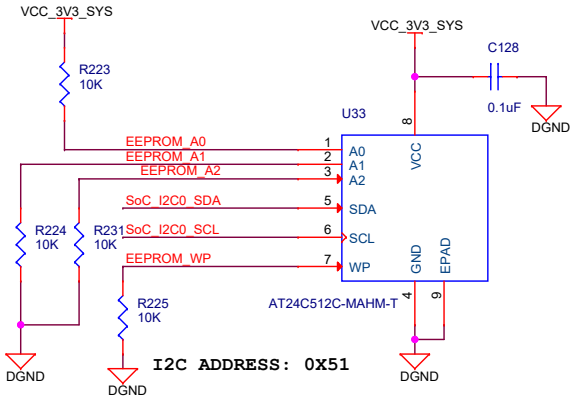
BOARD ID EEPROM



OFF PAGE CONNECTIONS

SoC_I2C0_SDA
SoC_I2C0_SCL

SoC_I2C0_SDA 28,33,41,42
SoC_I2C0_SCL 28,33,41,42

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOARD ID EEPROM	
Size: B	PROC100 SK-AM64	Rev: E2
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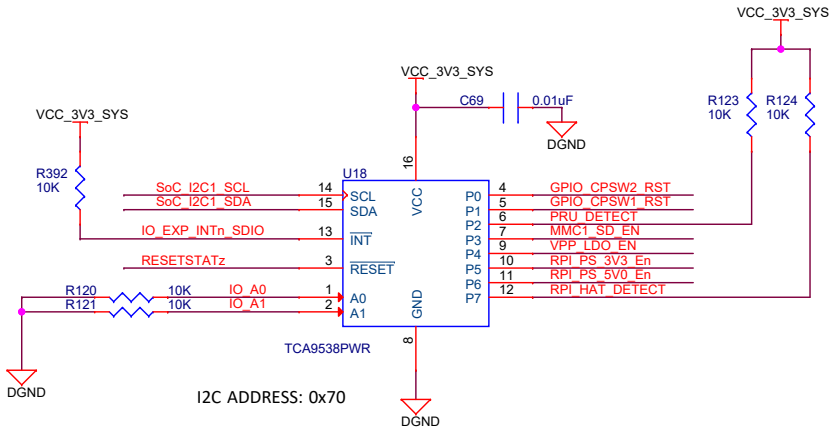
IO EXPANDER



OFF PAGE CONNECTIONS

RPI_PS_3V3_En	RPI_PS_3V3_En 28
RPI_PS_5V0_En	RPI_PS_5V0_En 28
GPIO_CPSW2_RST	GPIO_CPSW2_RST 20
GPIO_CPSW1_RST	GPIO_CPSW1_RST 19
MMC1_SD_EN	MMC1_SD_EN 18
VPP_LDO_EN	VPP_LDO_EN 43
RESETSTATz	RESETSTATz 17,18,19,20,22,27,33
IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO 16
SoC_I2C1_SCL	SoC_I2C1_SCL 21,32,33,36
SoC_I2C1_SDA	SoC_I2C1_SDA 21,32,33,36
RPI_HAT_DETECT	RPI_HAT_DETECT 28
PRU_DETECT	PRU_DETECT 27

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Title	IO EXPANDER	
Size: B	PROC100 SK-AM64	Rev: E2
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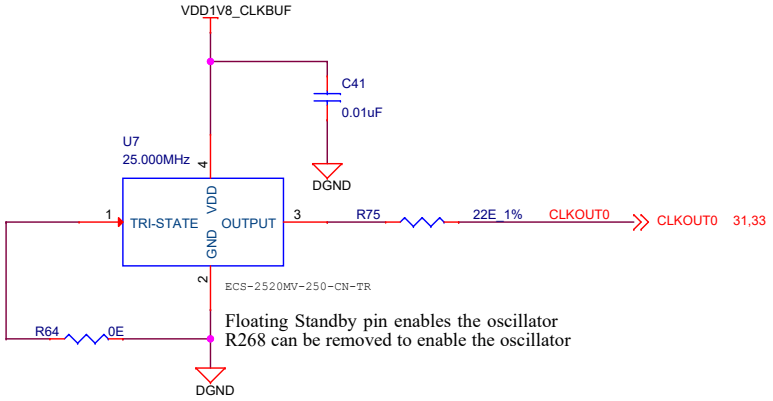
OSCILLATOR



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Title	OSCILLATOR	
Size: B	PROC100 SK-AM64	Rev: E2
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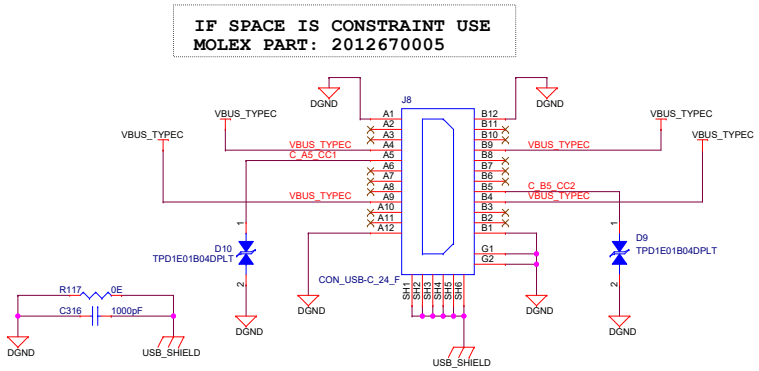
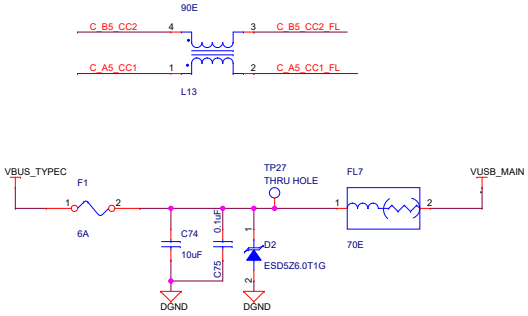
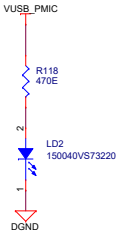
TYPE-C CONNECTOR



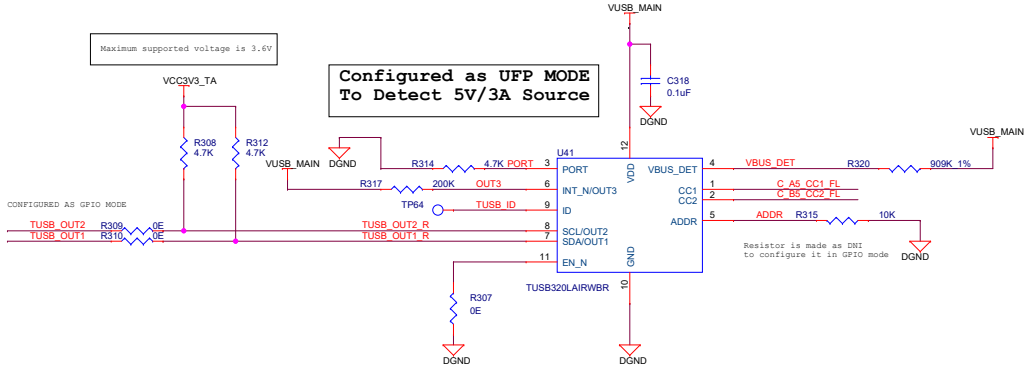
USB MAIN INPUT 5V DC



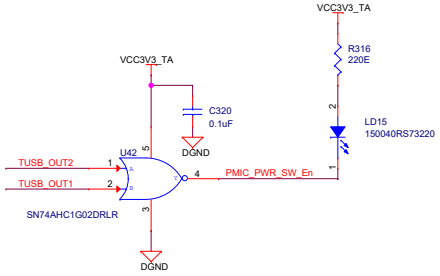
POWER INDICATION LED: USB VBUS



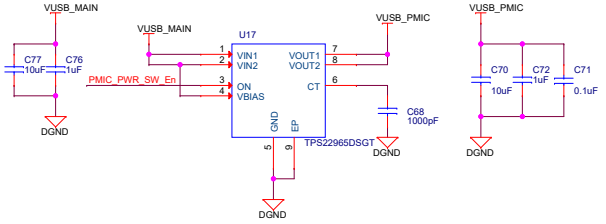
USB TYPE C CONFIGURATION CHANNEL LOGIC AND PORT CONTROLLER



Enable Logic for Power Switch



POWER SWITCH ON USB VBUS MAIN SUPPLY



TEST POINT

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Title	USB MAIN 5V POWER SUPPLY	
Size	PROC100 SK-AM64	Rev
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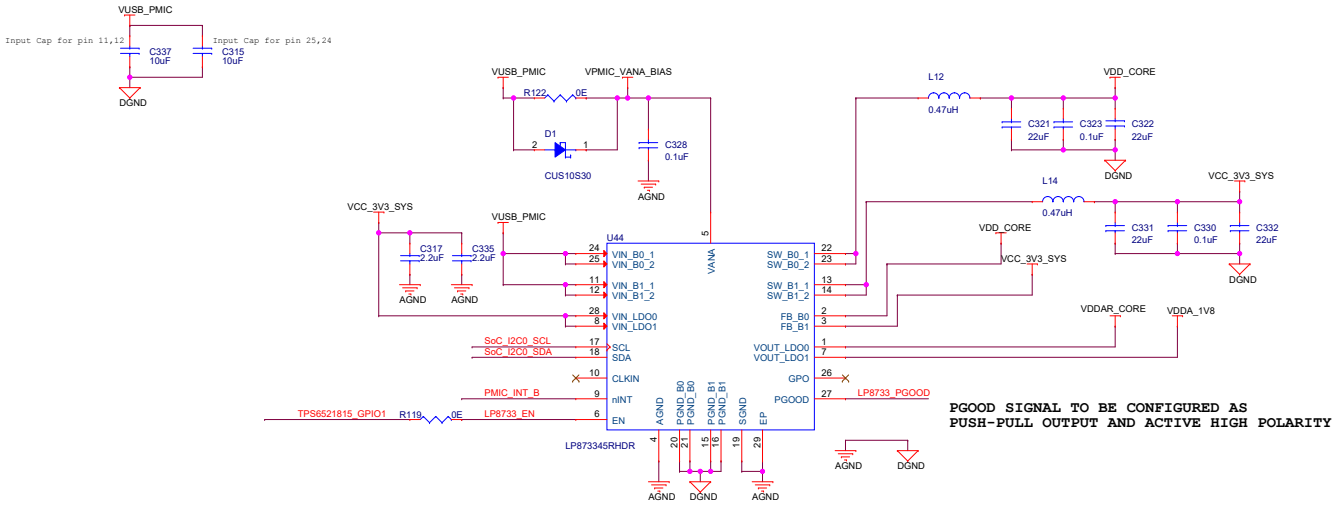
PMIC-1 POWER SUPPLY

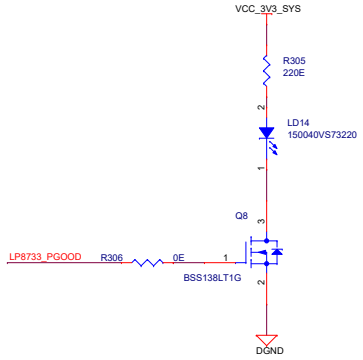
NOTE:
This power solution should not be used for a production system.



NOTE: The Voltage for the following AM64x power supplies should be 0.85V typical (0.81V minimum, 0.895V maximum)
1."VDDR_CORE"
2."VDDA_CORE, VDD_MMC0, VDD_DLL_MMC0, VDDAR_0P85_SERDES0, VDDAR_0P85_SERDES0_C, VDDAR_0P85_USB0"

But VOUT_LDO0 (VDDAR_CORE) of LP873345 is programmed to 0.9V

POWER INDICATION LED



OFF PAGE CONNECTIONS

28,33,37,42	SoC_I2C0_SCL	SoC_I2C0_SCL
28,33,37,42	SoC_I2C0_SDA	SoC_I2C0_SDA
34	LP8733_PGOOD	LP8733_PGOOD
27,42	PMIC_INT_B	PMIC_INT_B
42	TPS6521815_GPIO1	TPS6521815_GPIO1

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Title	PMIC-1 POWER SUPPLY	
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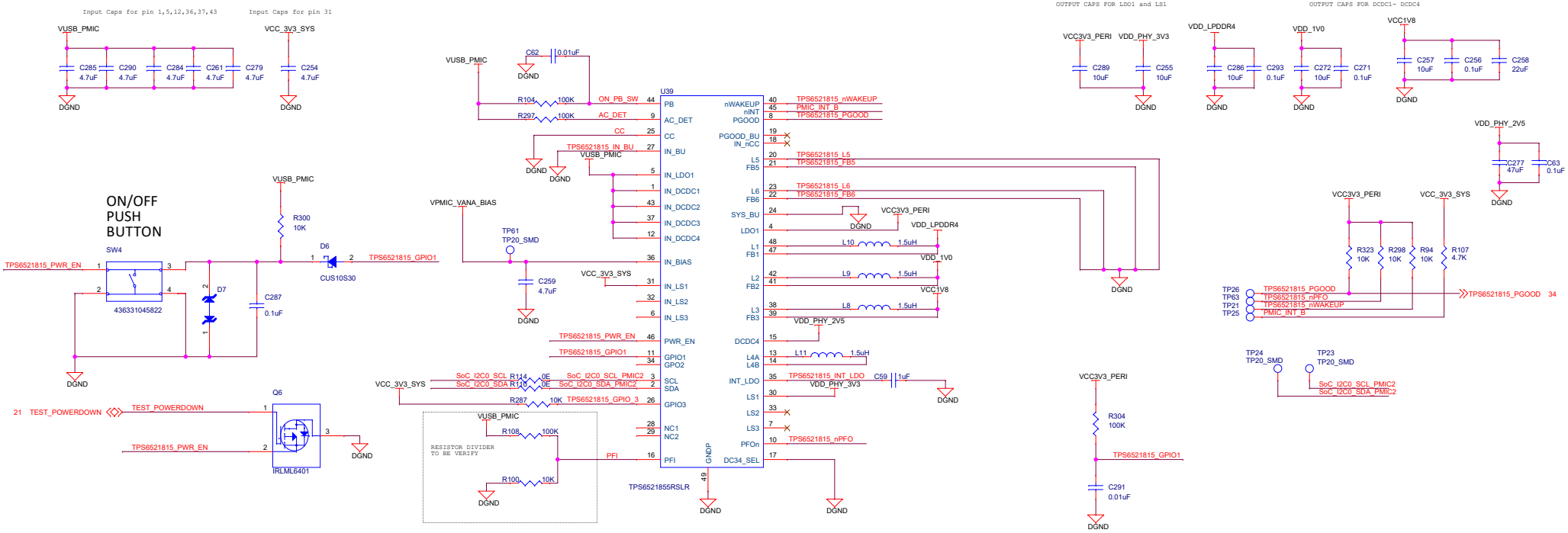
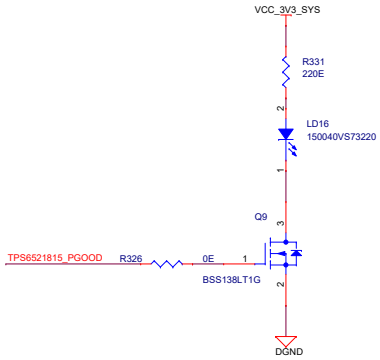
PMIC-2 POWER SUPPLY



POWER INDICATION LED



OFF PAGE CONNECTIONS

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Title	PMIC-2 POWER SUPPLY	
Size	PROC100 SK-AM64	Rev
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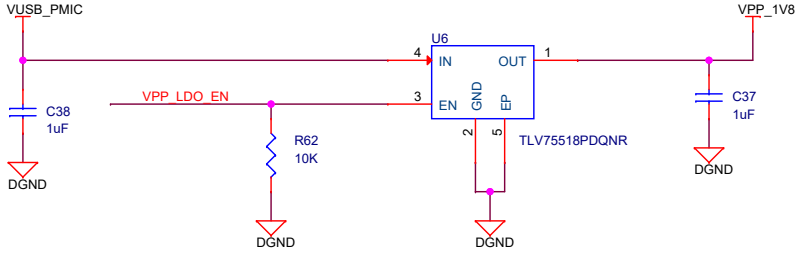
eFUSE PROGRAMMING VOLTAGE TO SoC



1.8V VPP, 0.15AMPS SUPPLY

OFF PAGE CONNECTIONS

38 VPP_LDO_EN <<< VPP_LDO_EN

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Title	eFUSE PROGRAMMING PWR SOC	
Size: B	PROC100 SK-AM64	Rev: E2
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STRAP CONFIGURATION OF ETHERNET PHYS

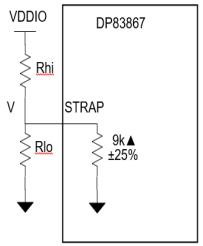

Figure 25. Strap Circuit

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

Level Strap Resistor Ratios

PIN NAME	64 HTQFP PIN #	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
RX_D0	44	33	[00]	MODE	PHY_ADD1	PHY_ADD0
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D2	46	35	[00]	MODE	PHY_ADD3	PHY_ADD2
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D4	48		[00]	MODE	ANEG_SEL1	PHY_ADD4
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D5	49		[00]	MODE	Force MDI/X	Half-Duplex Enable (FD/HD)
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D6	50		[00]	MODE	RGMII Disable	AMDIX Disable
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_D7	51		[00]	MODE	Speed Optimization Enable	Clock Out Disable
				1	0	0
				2	0	1
				3	1	0
				4	1	1
RX_DV/RX_CTRL (1) (Straps Required)	53	38	[0]	MODE		Autoneg Disable
				1		N/A
				2		N/A
				3		0
				4		1
CRS(2)	56		[0]	MODE		Fast Link Drop (FLD)
				1		0
				2		1
				3		N/A

Level Strap Pins

PIN NAME	64 HTQFP PIN #	48 QFN PIN #	DEFAULT	STRAP FUNCTION		
LED_2(3)		45	[00]	MODE	RGMII Clock Skew TX[1]	RGMII Clock Skew TX[0]
				1	0	0
				2	0	1
				3	1	0
				4	1	1
LED_1 (RGZ)		46	[00]	MODE	ANEG_SEL	RGMII Clock Skew TX[2]
				1	0	0
				2	0	1
				3	1	0
				4	1	1
LED_1 (PAP)	62		[0]	MODE	ANEG_SEL0	
				1	0	
				2	0	
				3	1	
				4	1	
LED_0(4)	63	47	[0]	MODE	Mirror Enable	
				1	0	
				2	N/A	
				3	1	
				4	N/A	
GPIO_0 (3)		39	[00]	MODE	RGMII Clock Skew RX[0]	
				1	0	
				2	Not Applicable	
				3	1	
				4	Not Applicable	
GPIO_1		40	[00]	MODE	RGMII Clock Skew RX[2]	RGMII Clock Skew RX[1]
				1	0	0
				2	0	1
				3	1	0
				4	1	1

Level Strap Pins

MODE	ANEG_SEL	REMARKS
10/100/1000	0	advertise ability of 10/100/1000
100/1000	1	advertise ability of 100/1000 only

MODE	RGMII CLOCK SKEW TX[2]	RGMII CLOCK SKEW TX[1]	RGMII CLOCK SKEW TX[0]	RGMII TX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

MODE	RGMII CLOCK SKEW RX[2]	RGMII CLOCK SKEW RX[1]	RGMII CLOCK SKEW RX[0]	RGMII RX CLOCK SKEW
1	0	0	0	2.0 ns
2	0	0	1	1.5 ns
3	0	1	0	1.0 ns
4	0	1	1	0.5 ns
5	1	0	0	0 ns
6	1	0	1	3.5 ns
7	1	1	0	3.0 ns
8	1	1	1	2.5 ns

RGMII Clock Skew Details

HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB

PCB1

PROC100

JUMPERS

ACC1

SPC02SYAN

LOGOs

PCB LOGO
Texas Intruments
Texas Intruments

PCB LOGO
For Evaluation only; not FCC approved for resale
For Evaluation only; not FCC approved for resale

PCB LOGO
WEEE Mark
WEEE Mark

PCB LOGO
CE Mark
CE Mark

FIDUCIALS

FID1 FID_40X80
FID2 FID_40X80
FID3 FID_40X80
FID4 FID_40X80
FID5 FID_40X80
FID6 FID_40X80

LABELS

Board Serial No.

LBL1
PCB LABEL
THT-103-423-10

Assembly Revision

LBL3
PCB LABEL
THT-103-423-10

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Title	HARDWARE SCHEMATICS	
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