**TIXU_MX6Y**

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**Revision Notes**

A1-01
1) Made R13=200E, R14=300E to avoid loading of DCDC6 feedback.
2) Made R221 NM, R248 M to make uSDHC1 as default boot source.
3) Made R77 NM, So that SD connector can control SD_CD# state.
4) Made R233 NM, since the PGODC_BU voltage is of 1V8 and PU is 3V.
5) Made R250 NM, R219 M to select 4 bit bus width boot.
6) Made R231 NM, R235 M to disable powercycle during boot.
7) Made R571 NM to disable extender mode in ethernet PHY.
8) Made R773 NM, R779 NM to avoid the distortion of RMII reference clock.
9) Made R771 NM to make PMIC_PWR_EN High always.

A1-02
1) R771 Mounted

A1-03
1) Mounted R190, R191, R261 with 0E; Made R192, R193, R262 NM for LCD Rework.

A1-04
1) Mounted R773, R779 with 510E for avoiding the dip in reference clock voltage.
2) Mounted R872, R873 with 49.9E and R208, R204 with 47K for clearing push button deglitch.

A2
A2 Release

**TIDA-050043**

**Title:** COVER_PAGE

**Pub No:** 581-016161

**Rev:** A2

**Asy No:** 701-00380

**Sheet:** 1 of 21
Note: Over-voltage protection is designed to withstand up to +20V.
LOAD SWITCH & COINCELL

VDD_PERI_3V3 SWITCH (LS5)

Make the status of GPIO1 low before the power up.

LOAD SWITCH & COINCELL

5V LOAD SWITCH (LS4)

Please mount all 3 res together in case of using this option.

COIN CELL

SD CARD VOLTAGE SELECTION SWITCH

Remove DCDC6 connection to VDD_SNVS_IN if we use this option.
Place 22 uF cap and one of the 0.22uF caps next to the ball G9. Place others within 50 mils of via. Do not connect any loads to VDDARM_CAP.

Diode Is recommended in i.MX6ULL Hardware userguide.

LDO_ARM_SOC
LDO_2P5
LDO_1P1
LDO_SNVS
Place R738 & 739 in tripad

**IMX-LCD, ENET, eMMC, SDIO**

Place R773 & 779 close to processor (Parallel termination)

3V3 and 1.8V options are given since there is a small confusion in datasheet
Mount 2.2M res close to XTALI pin.
Pull up Resistors on SD2_DATA, SD2_CMD lines are for avoiding bus floating.

Layout note: Decoupling capacitor should connect close to power and ground.

U15 intended to use in HS200 mode. For that VCCQ need to maintain as 1V8.
The minimum low pulse needed for RESET# is 1us.

RESET need to assert during 3v3 rise up time to meet max Rise time limit on 3v3 rail.

I2C ADDR=0x2C

The min low pulse needed for RESET# is 1us.
LCD IO & CORE POWER SWITCHES

- Place FB3 & FB4 in tripad
- Place FB5 & FB6 in tripad

VDD_LCD = 2V8 for the part NHD-2.8-240320AF-CSX
VDD_LCD = 3V3 for the part NHD-2.4-240320CF-CSXV#-F

VDDIO for LCD = 1V8.3V3 option is given only because of mismatch in datasheet. Please refer to data sheet to mount FB6.

NM

TOUCH CONTROLLER

- TSC2046
- VDD_PERI_3V3

Current Design is for the part NHD-2.4-240320CF-CSXV#-F (No touch)
BOOT CONFIGURATION

NOTE: To select boot device as eMMC along with the DIP switch change mount R221 with 10K and no mount R248.
MISCELLANEOUS

MOUNTING HOLES

GLOBAL FIDUCIALS

GND TEST POINT

LOCAL FIDUCIALS

LCD MOUNTING HOLES
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