

REV	DESCRIPTION	DATE	Author
A	INITIAL RELEASE	07/31/2020	TNYC

**\*\*\* DISCLAIMER \*\*\***

The SoC Reference Design Study provides SCH & PCB source files that can be used as a good starting point for new designs. Please be aware that the SCH & PCB are NOT 100% complete for implementing an End Product. An End Product's feature set will define additional required signaling and SoC interfaces. As a result, a majority of signals in this SCH are "single-pin" / "unconnected" nets.

The SoC's schematic symbol has been organized based upon each ball's "primary signaling interface". For End Products, unused primary interface signals can then be re-defined by SoC's internal muxmode controll (see Data Manual for details) to use "alternate functions" (i.e. GPIOs) to support other key system needs (i.e. interrupts, debug, etc.).

Primary objectives of this Ref Design are to demonstrate:

1. 100% signal & power breakout routing of SoC using recommended PCB design rules & strategies.
2. Key high-speed signals with controlled impedance PCB routing (i.e. DDR & SERDES).
3. Power Distribution Network (PDN) with the following:
  - a) Recommended SoC power solution components (2nd stage) showing preferred SoC voltage domain to power resource mapping.
  - b) Optimized decoupling capacitor scheme per key power rail using only automotive qualified caps to meet SoC recommended power integrity (PI) parameters based on this specific PCB design (stack-up, placement, routing, via types, etc).
  - c.) A typical 1st stage power conversion interfaced directly to input battery has been captured as an example.

REVISION STATUS OF SHEETS

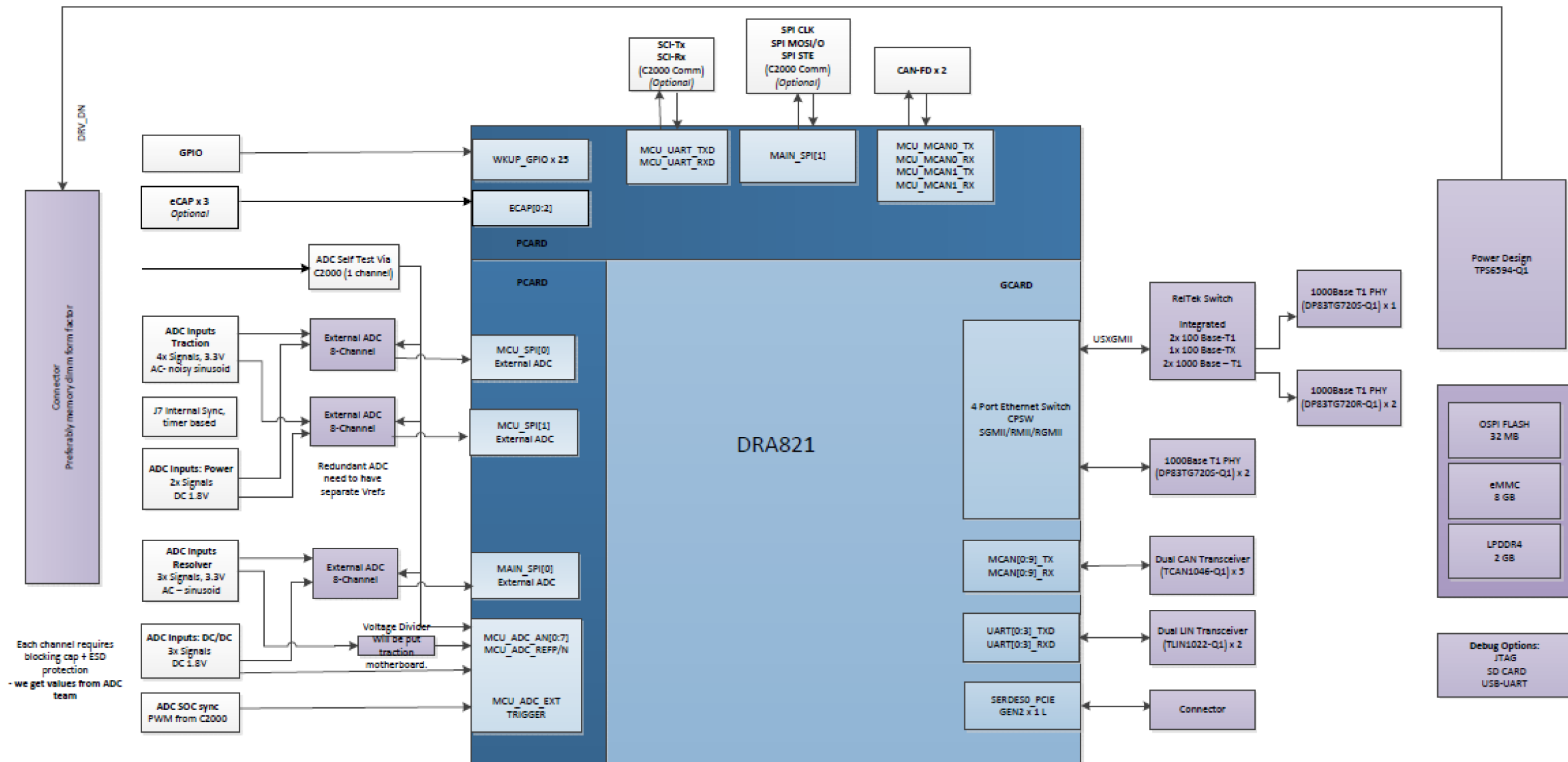
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REV	1.0	1.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0
SH	21	22	23	24	25	26	27	28	29	30
REV	1.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0	2.0	1.0
SH	11	12	13	14	15	16	17	18	19	20
REV	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
SH	1	2	3	4	5	6	7	8	9	10

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# REVISION HISTORY

REV B, 10/19/2020
SHEET 12, UART2 RX/TX SWAP
SHEET 19, VSYS_5V0 TO ALWAYS ON
SHEET 26, ADD R-MUX FOR MCAN1/MCU_MCAN1 AT U5
SHEET 23, MOVE R303 IN FRONT OF R302, ADD R327 TO MMC_PWR_ON. ROUTE MMC1_SDCD(ECAP1) AND MMC_PWR_ON(ECAP2) TO J11/J18.

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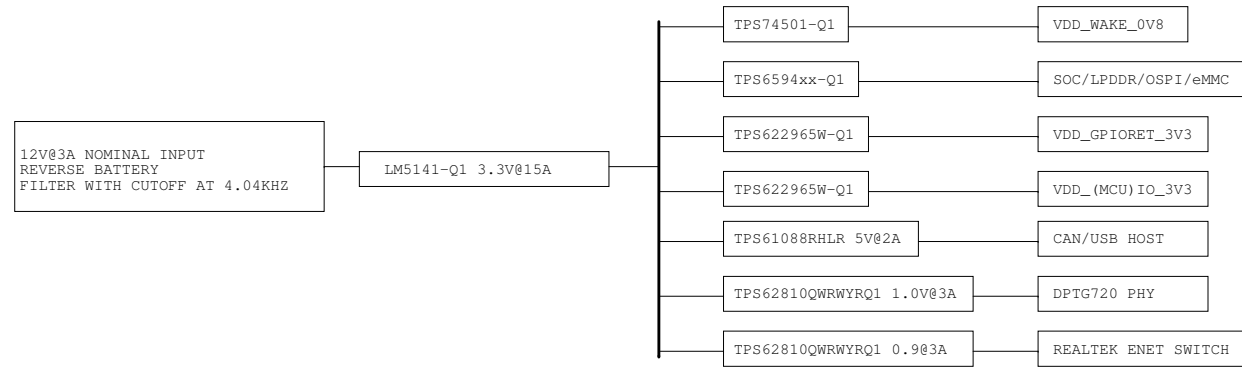


Each channel requires blocking cap + ESD protection - we get values from ADC team

**NOTES:**

- 1) C2000 INTERFACE SUPPORTS BOARD TO BOARD AND BOARD TO CABLE WITH SAMTEC TFM/SFM/SFSD COMPONENTS.  
[http://suddendocs.samtec.com/catalog\\_english/tfm.pdf](http://suddendocs.samtec.com/catalog_english/tfm.pdf)  
[http://suddendocs.samtec.com/catalog\\_english/sfm.pdf](http://suddendocs.samtec.com/catalog_english/sfm.pdf)  
[http://suddendocs.samtec.com/catalog\\_english/sfsd.pdf](http://suddendocs.samtec.com/catalog_english/sfsd.pdf)
- 2) T1 INTERFACE USES TE MATENET SINGLE PORT AUTOMOTIVE GRADE CONNECTORS.  
<https://www.te.com/usa-en/products/connectors/automotive-connectors/intersection/matenet.html?tab=pgp-story>
- 3) CAN/LIN INTERFACE USES MOLEX MINI150 AUTOMOTIVE GRADE CONNECTORS.  
[https://www.molex.com/molex/products/part-detail/pcb\\_headers/0348260124](https://www.molex.com/molex/products/part-detail/pcb_headers/0348260124)
- 4) USB INTERFACES USE MINI A/B CONNECTORS.
- 5) INPUT POWER IS STANDARD 2.5mm EVM STYLE.
- 6) 3.3V IO RETENTION ON CAN/LIN TIED TO VDDSHV2 FOR GATEWAY INTERFACE.
- 7) 3.3V IO RETENTION ON SPI/GPIO TIED TO VDDSHV2 FOR C2000 INTERFACE. THIS IS MINIMAL NUMBER OF PINS.
- 8) HIGH SECURITY DEVICE EPUSE PROGRAMMING NOT SUPPORTED.
- 9) EXTERNAL PMIC PROGRAMMING VIA USB2ANY.
- 10) SD CARD SUPPORT IS FIXED 3.3V.
- 11) SUBSET OF BOOTMODES ARE SWITCH SELECTABLE.

# POWER BLOCK DIAGRAM



CAN/LIN WAKEUP SUPPORTED ON GATEWAY VIA VDDSHV2@3.3V.  
 THE 5V CAN BOOST REGULATOR IS ENABLED WITH  
 VDD\_GPIORET\_3V3 CONTROL. 5V TO THE USB POWER SWITCH IS  
 ALSO SUPPLIED BUT DISABLED. NOT ISOLATING 5V TO USB FOR  
 COST AND ITS OPTIONAL.

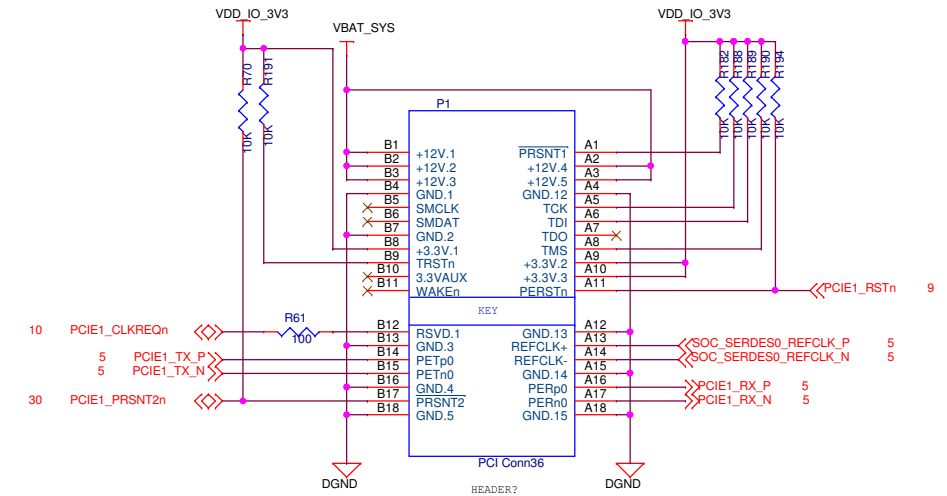
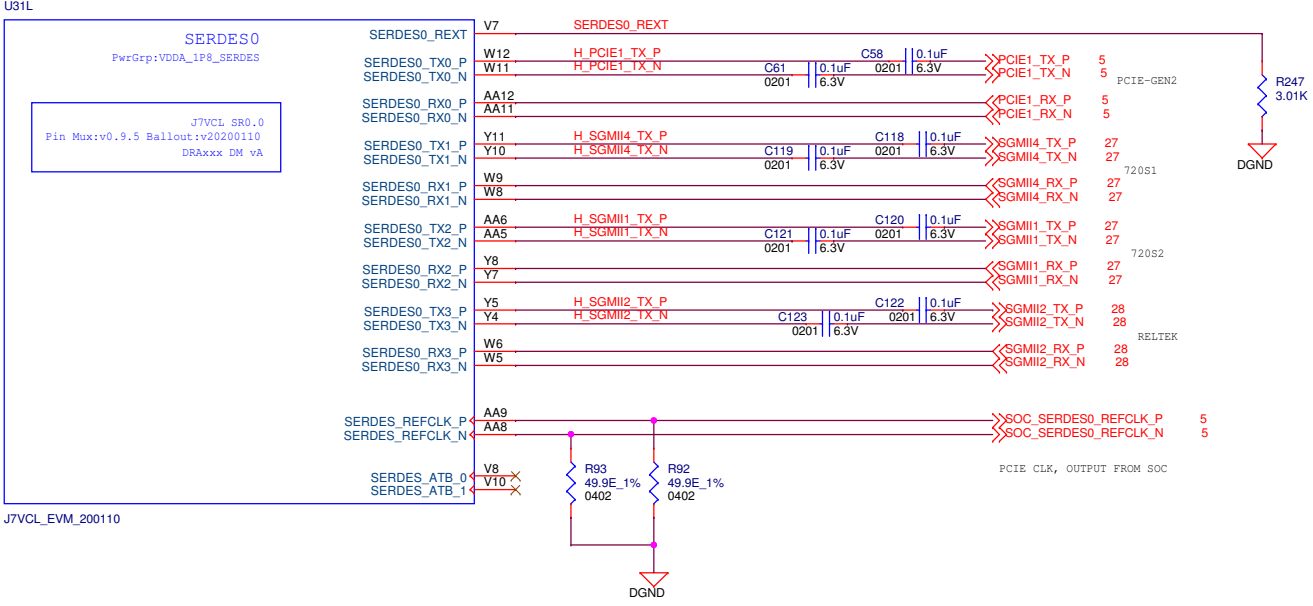
# ON BOARD GPIO ASSIGNMENTS

INDEX	BALL	SIGNAL	GPIO	IPU/IPD	SCHEMATIC NET	XPU/XPD
1	U17	MCAN10_TX	GPIO0_29		MCAN0_1_STB	10K PU
2	V17	RMII1_TX_EN	GPIO0_7		MCAN2_3_STB	10K PU
3	Y16	RMII1_TXD0	GPIO0_6		MCAN4_5_STB	10K PU
4	AA19	RMII1_TXD1	GPIO0_8		MCAN6_7_STB	10K PU
5	Y17	RMII1_RX_ER	GPIO0_5		MCAN8_9_STB	10K PU
6	V15	MCAN16_TX	GPIO0_45		LIN1_2_EN	10K PD
7	W20	MCAN15_RX	GPIO0_38		LIN3_4_EN	10K PD
8	U6	EXTINTn	GPIO0_0		ENET_INTSn	3.32K PU
9	U5	SPI0_CS1	GPIO0_52		ENET_WAKE	3.32K PD
10	W1	TIMER_IO1	GPIO0_61		MMC_PWR_ON	10K PU
11	C6	MCU_OSPIO_CS2	WKUP_GPIO0_30		WKUP_1V8_GPIO0_30	10K PU
12	C8	MCU_OSPIO_LBCLKO	WKUP_GPIO0_17		WKUP_1V8_GPIO0_17	10K PU

# MDx MAPPING

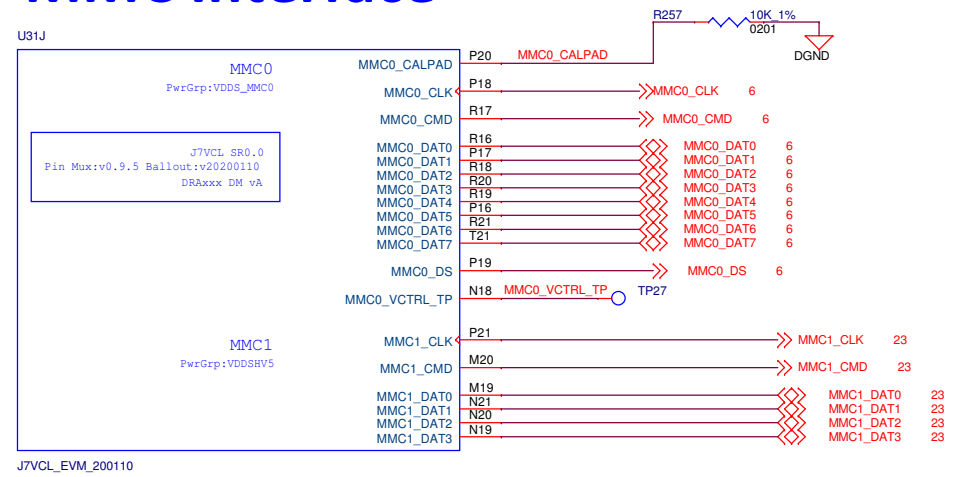
PHY/SWITCH	PORT	MDX ADDR	RX_CTRL	STRP_1
DP83TG720S	SGMII_1	0x04	10K	OPEN
DP83TG720S	SGMII_4	0x05	4.5K	OPEN
RTL9068	SGMII_2	0x18	NA	NA

# SERDES - PCIE-GEN2, SGMII, USXGMII ALL 100-OHM DIFF PAIRS.

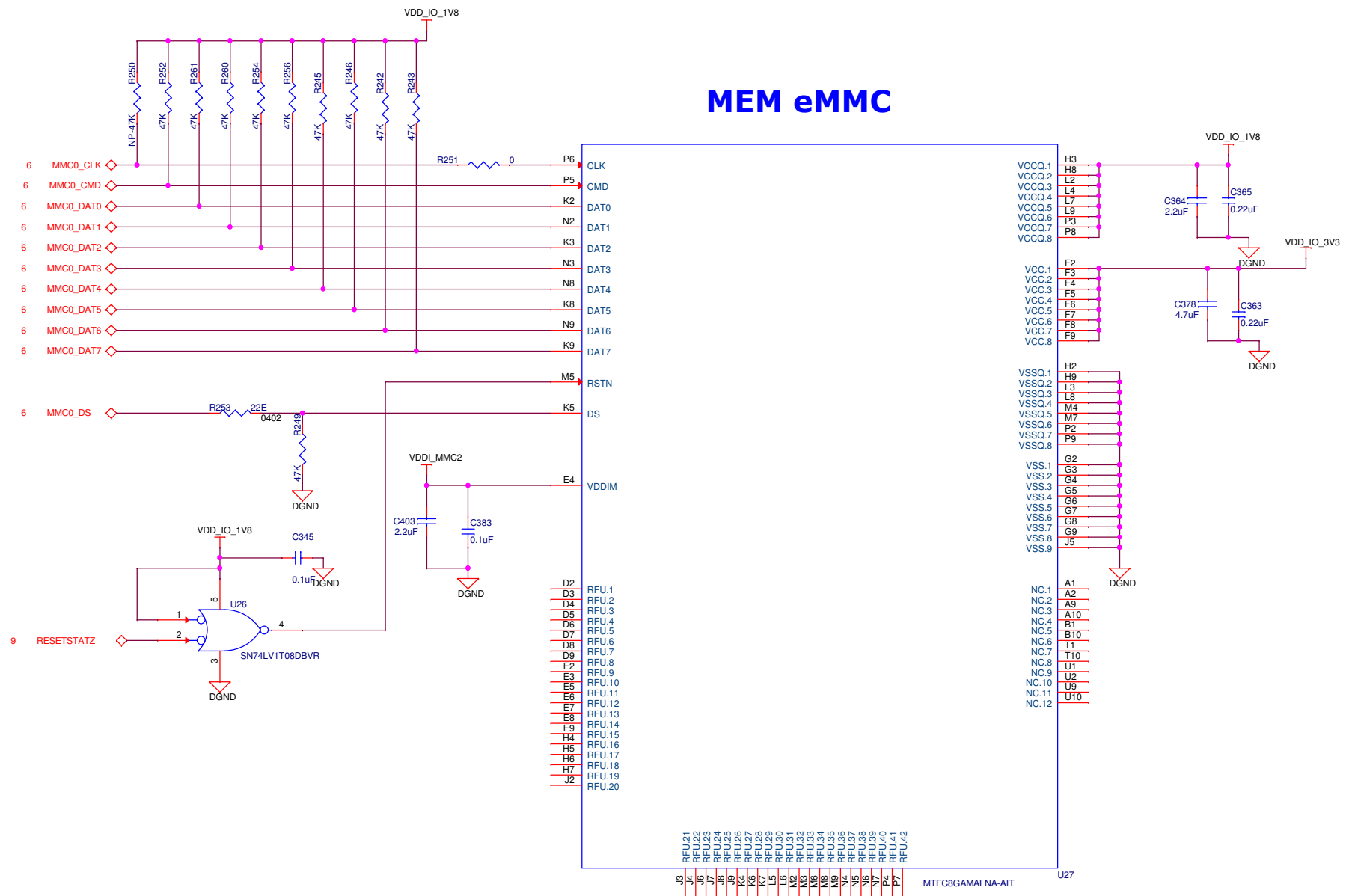


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# MMC Interface



# MEM eMMC



100BALL BGA 14mmX18mm, 1mm BALL PITCH  
 MTF32GAKAEDQ-AIT - V5.0  
 MTF32GAPALNA-AIT - V5.1  
 MTF32GAPALNA-AAT - V5.1  
 MTF32GAPALNA-AIT - V5.1 (8G)

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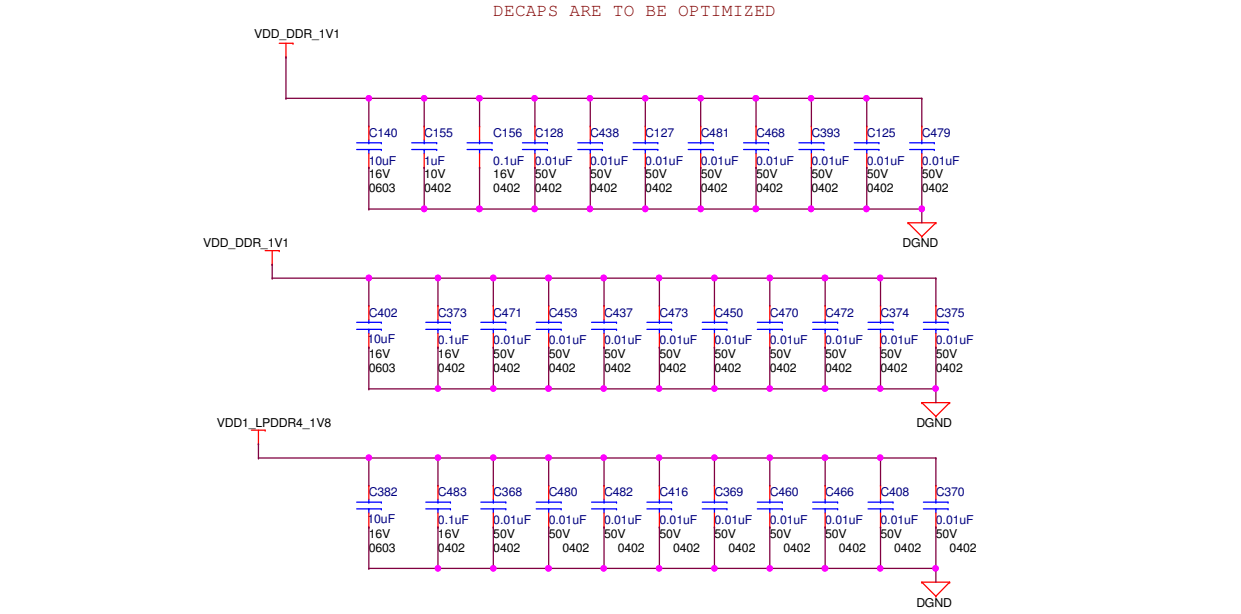
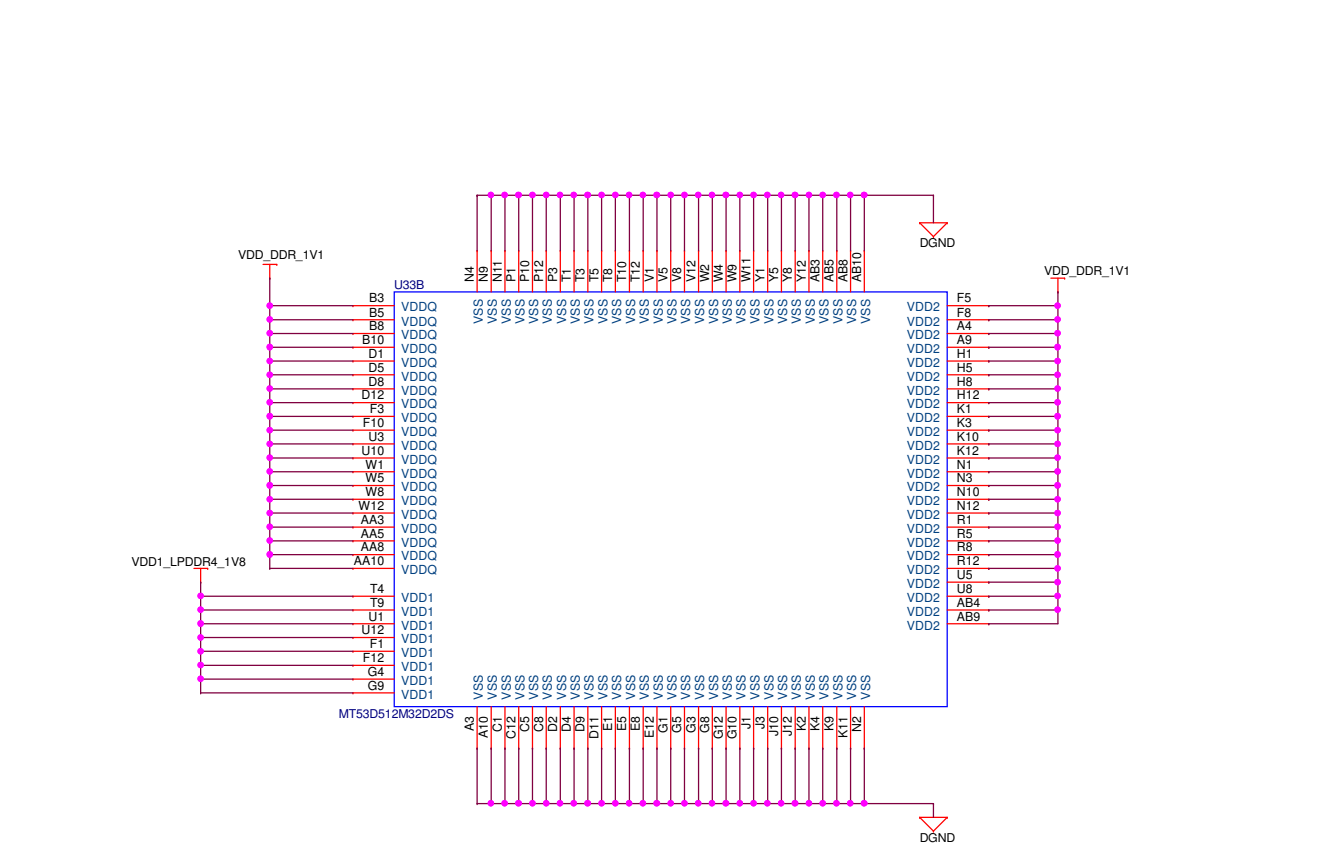
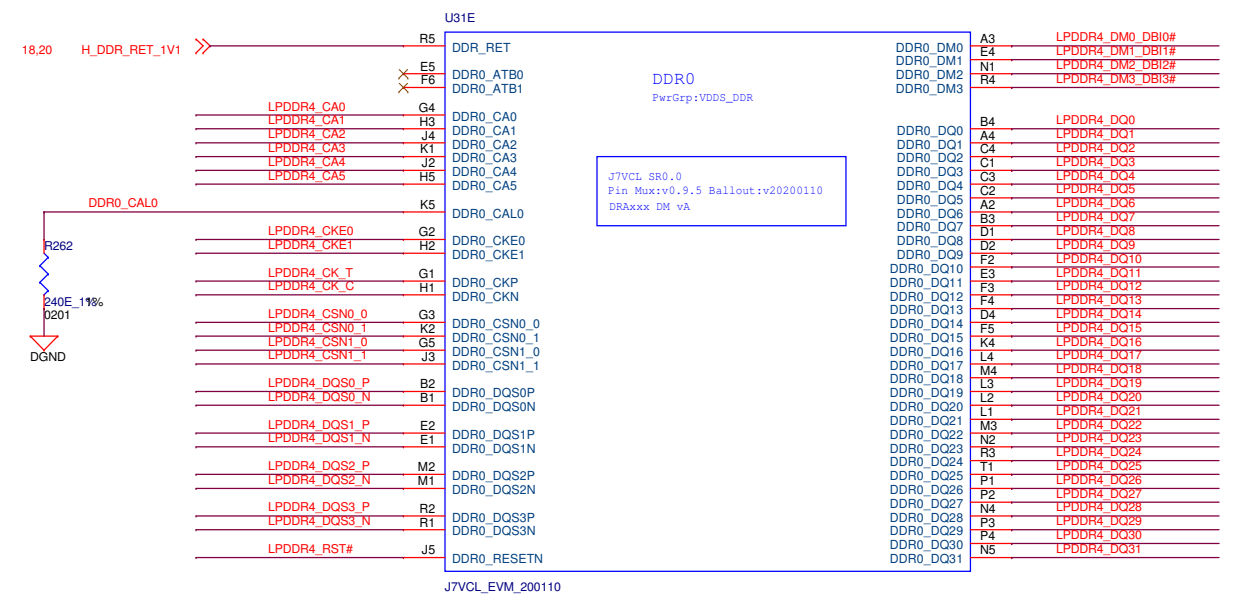
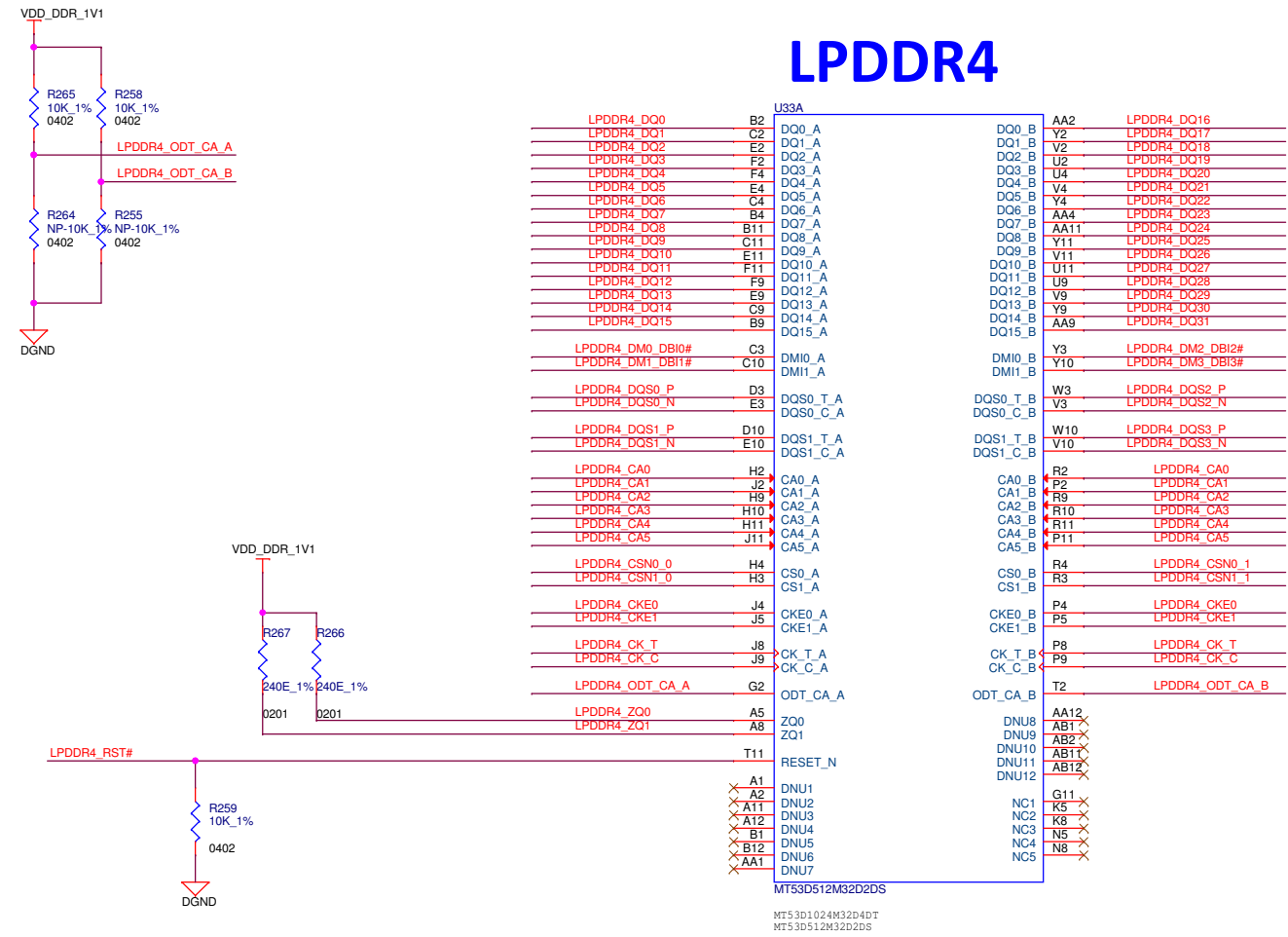
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# LPDDR4

# EMIF



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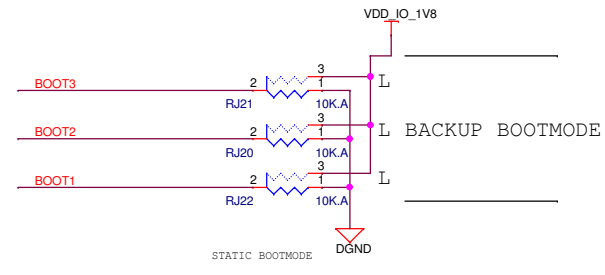
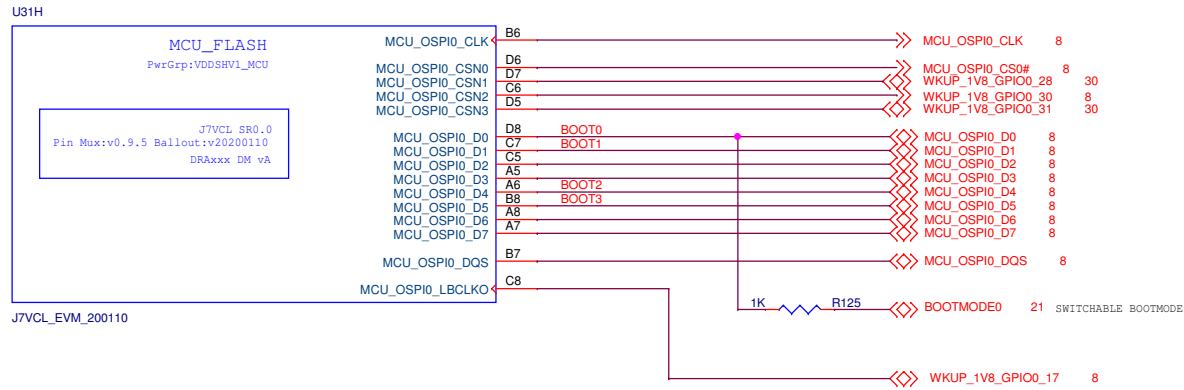
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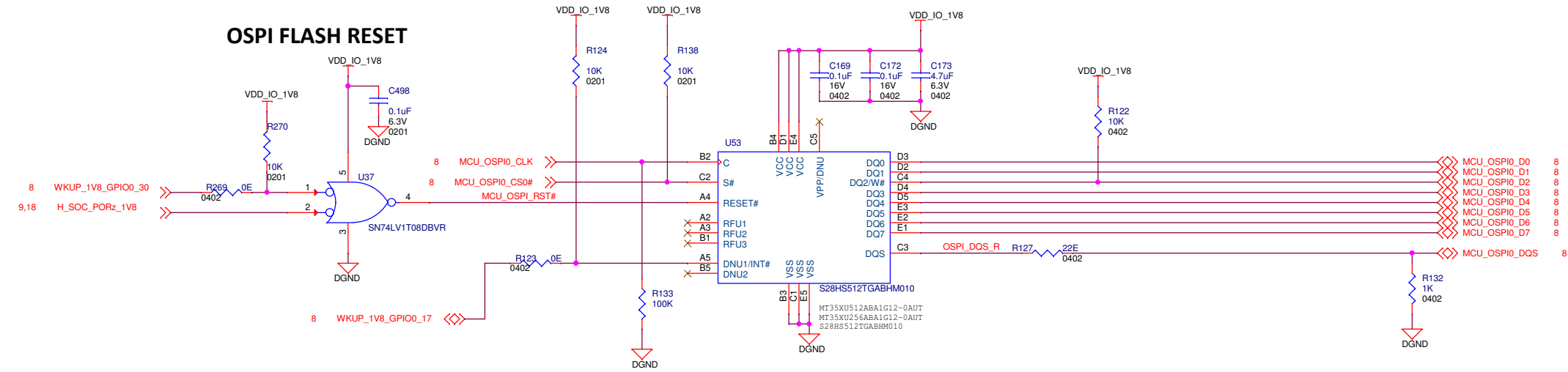
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# MCU FLASH

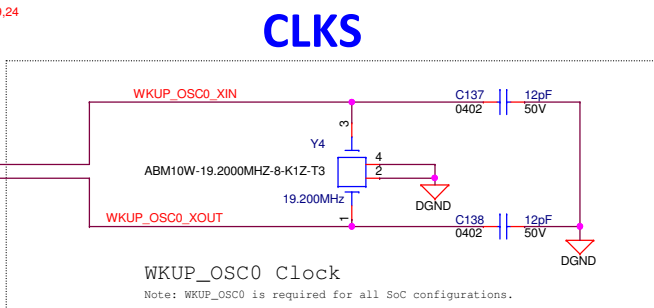
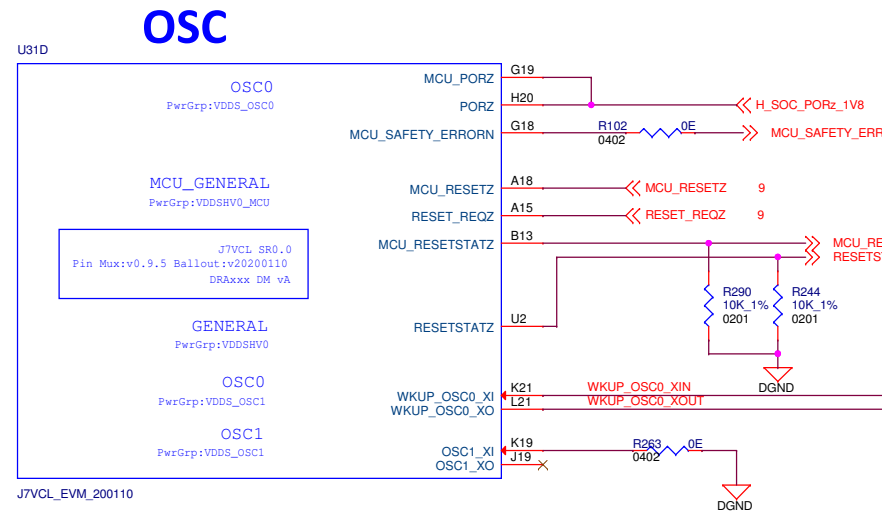
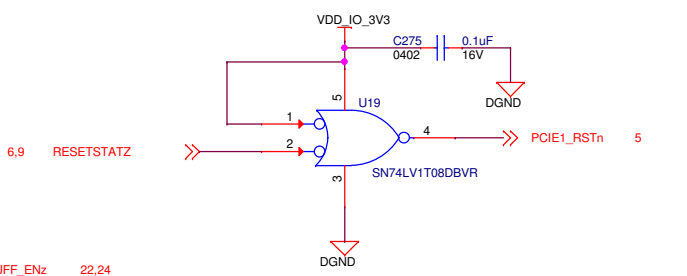
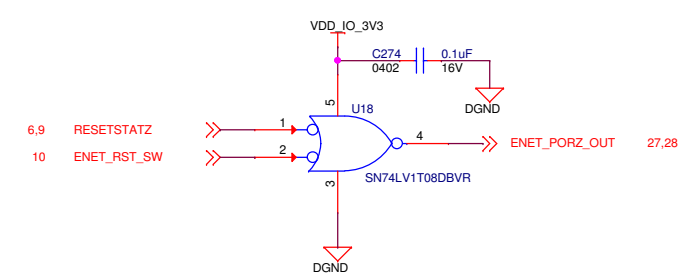
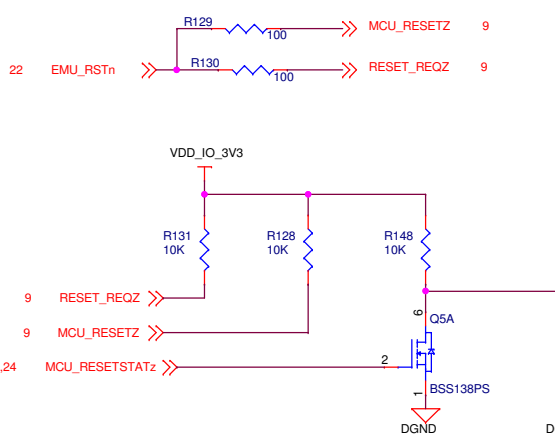
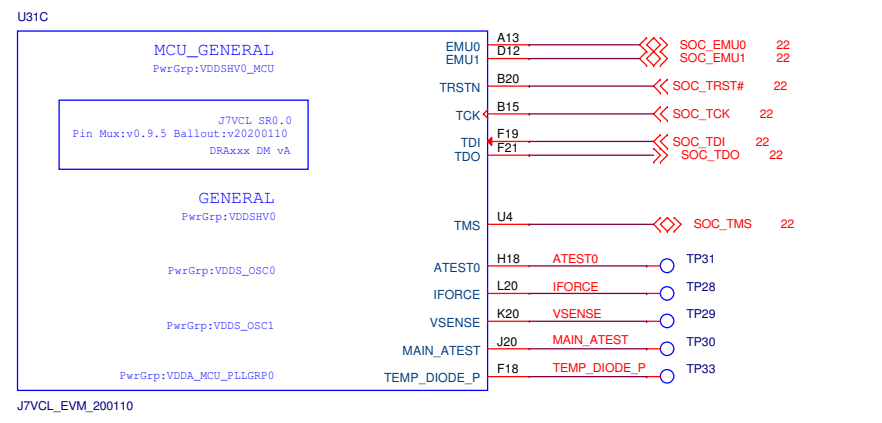
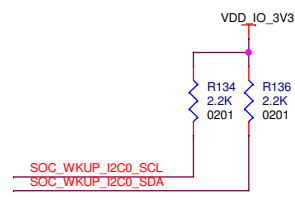
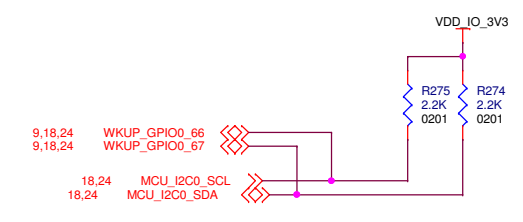
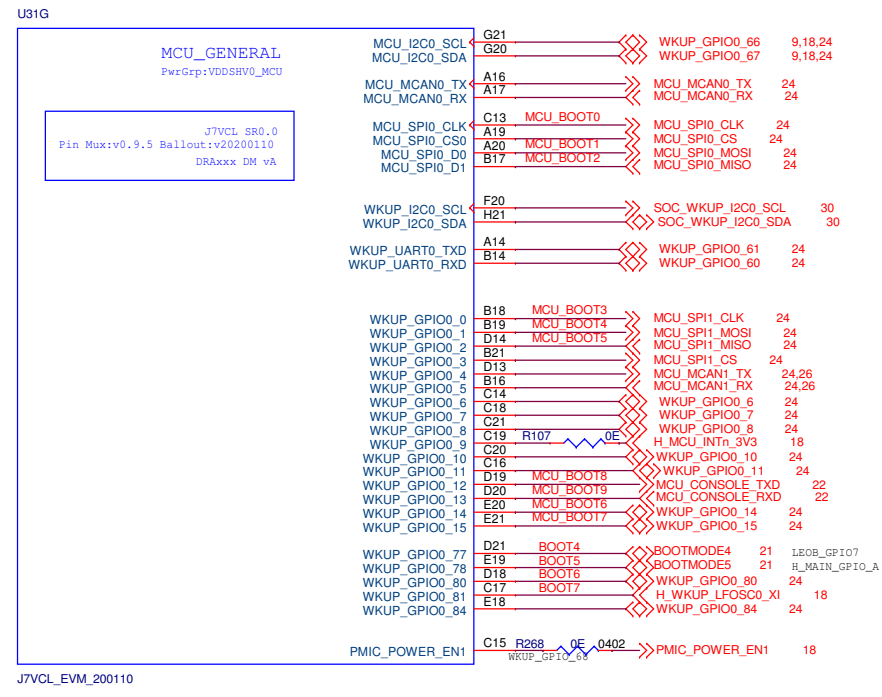


# OSPI FLASH



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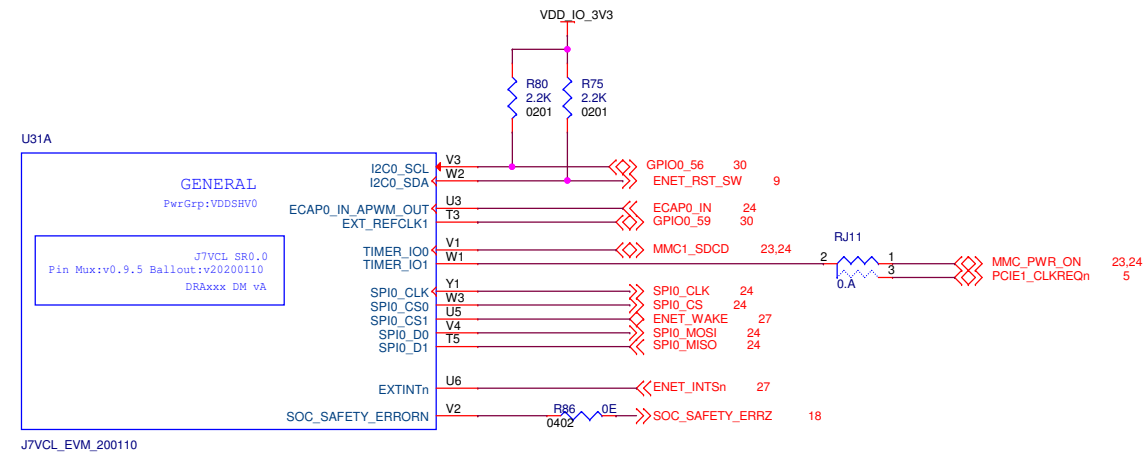
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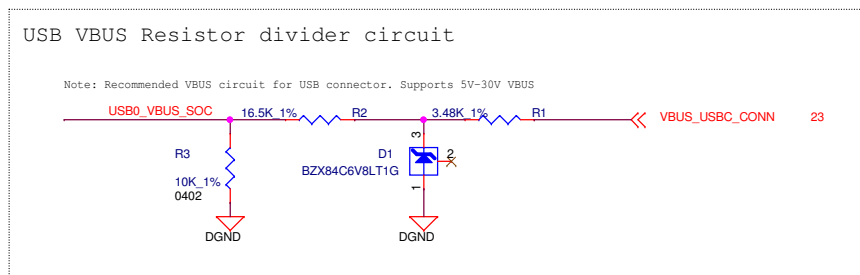
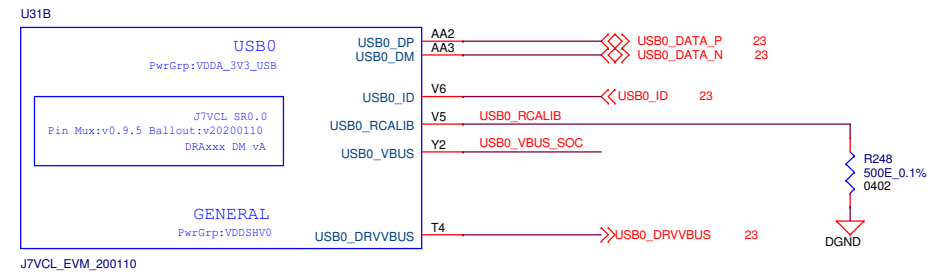
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# GENERAL

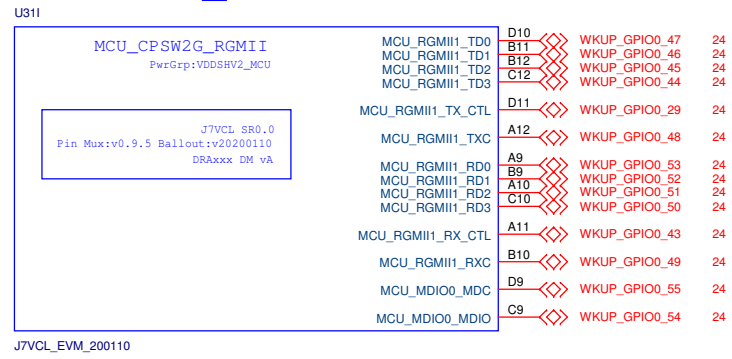


# USB

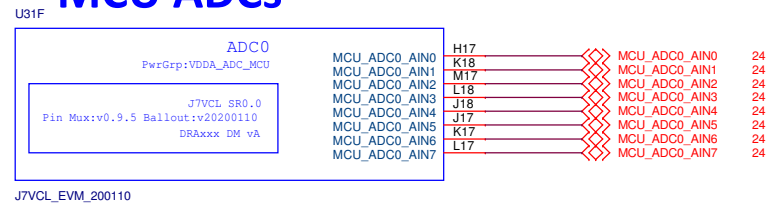


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## MCU\_RGMII

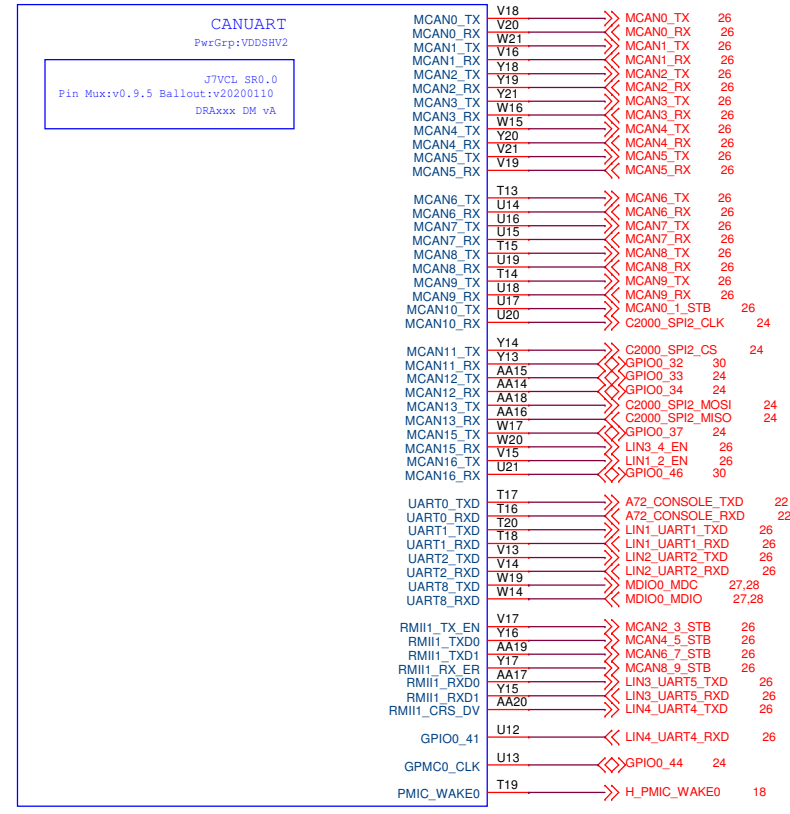


## MCU ADCs



# CAN/UART IO

U31K



IN GPIO RETENTION MODE NON-CAN/LIN SOC OUTPUTS SHOULD BE DRIVEN LOW. THIS PREVENTS DRIVING LOGIC HIGH INTO UNPOWERED PHER. PRIMARY SIGNALS TO PROTECT:  
 -C2000\*  
 -A72\_CONSOLE\_TXD  
 -MDIO\_MDC

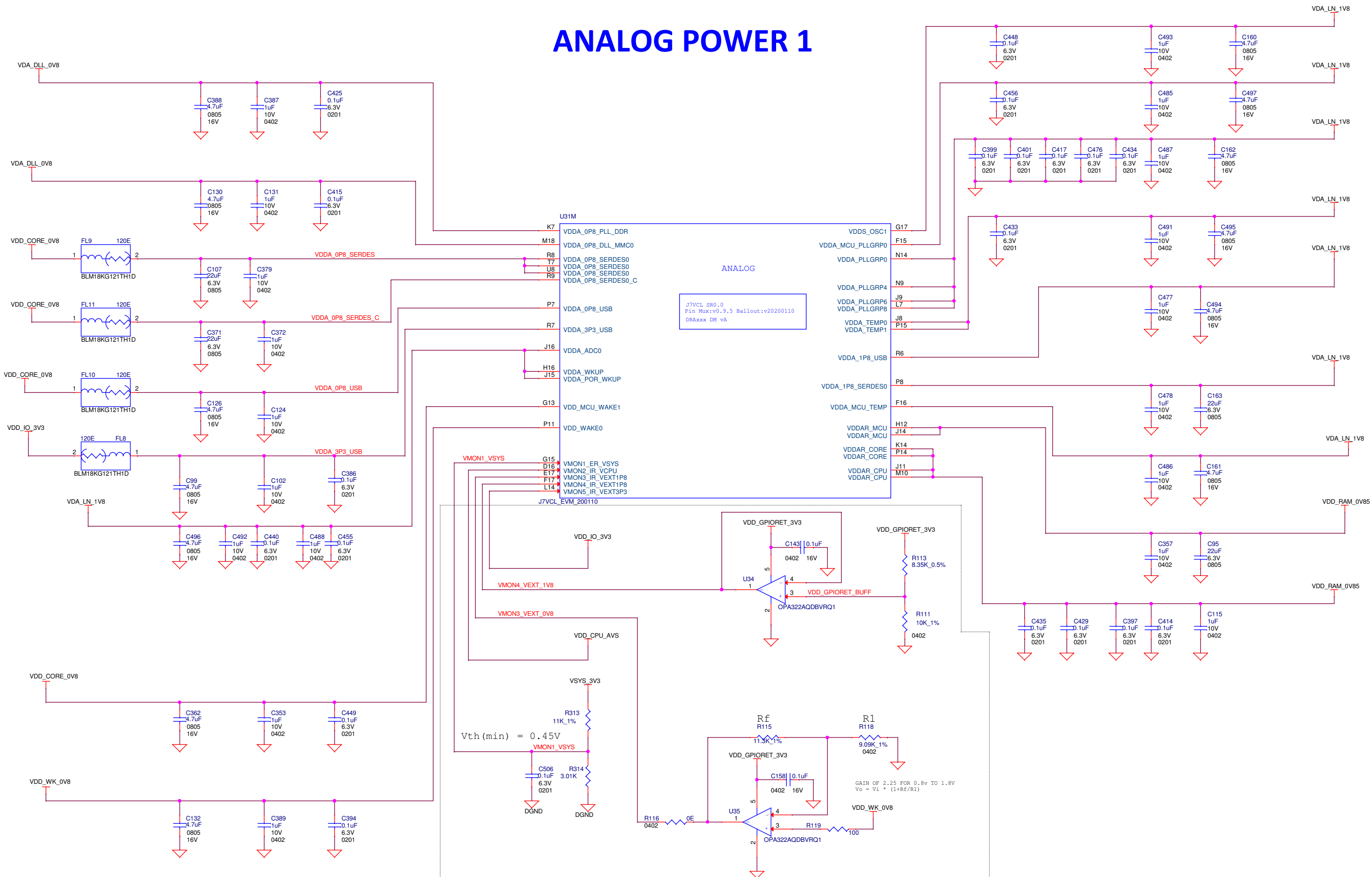
REV-B, UART2 RX/TX SWAP

J7VCL\_EVM\_200110

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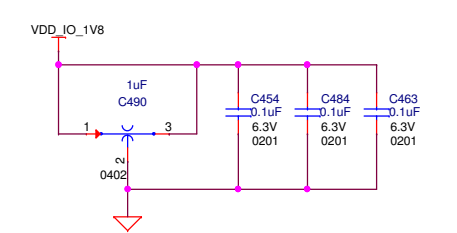
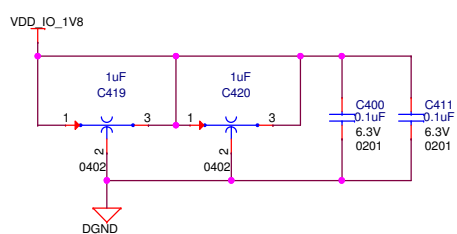
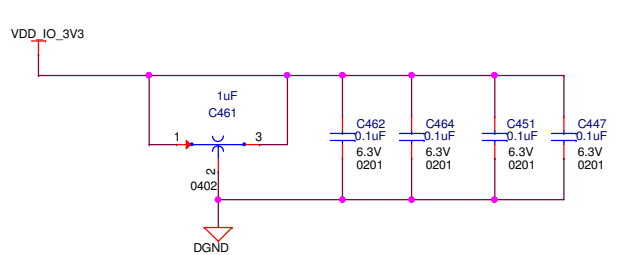
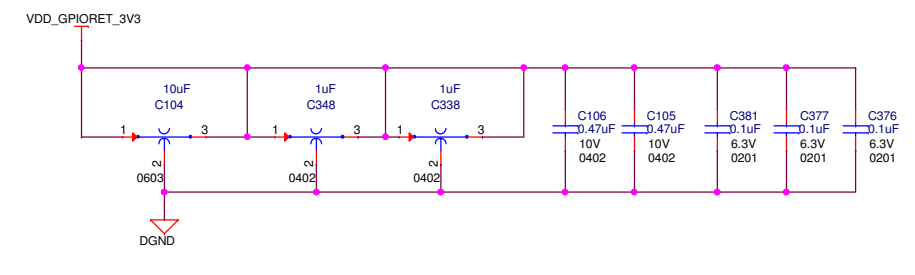
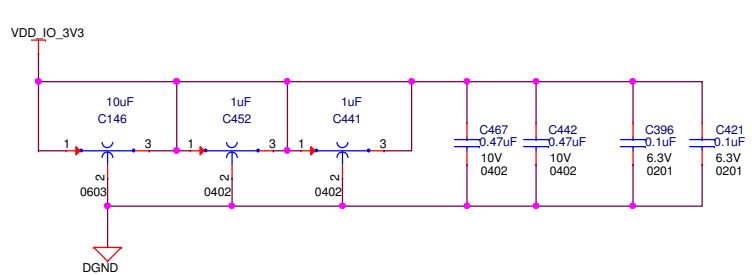
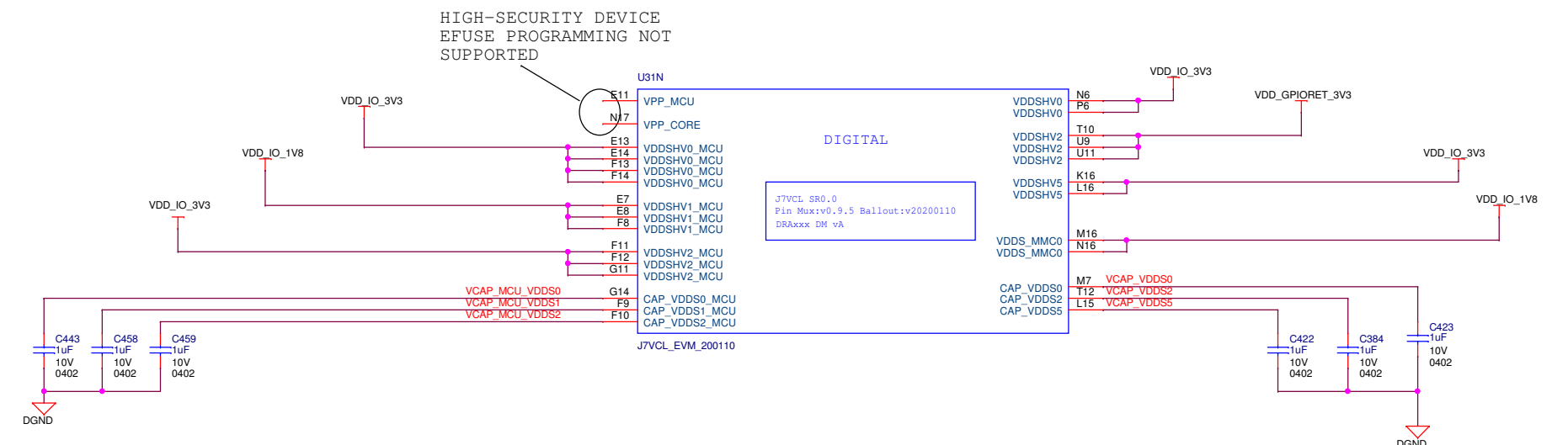
# ANALOG POWER 1



Note:  
 o VMON1\_ER\_VSYS: Voltage Monitor, fixed 0.45V (+/-3%) threshold.  
 Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.  
 o VMON2\_IR\_VCPU: Must be externally connected directly to VDD\_CPU  
 o VMON3\_IR\_VEXT1P8: General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor Divider.  
 o VMON4\_IR\_VEXT1P8: General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor Divider.  
 o VMON5\_IR\_VEXT3P3: General purpose voltage monitor for external supplies, 3.3V threshold. With internal resistor Divider.

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# DIGITAL POWER 2



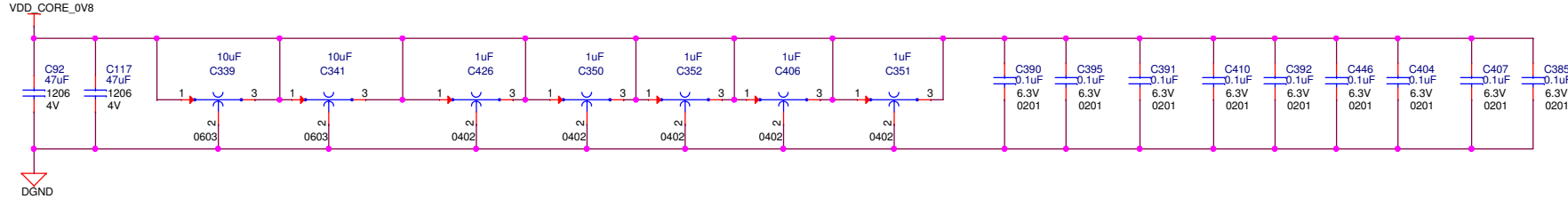
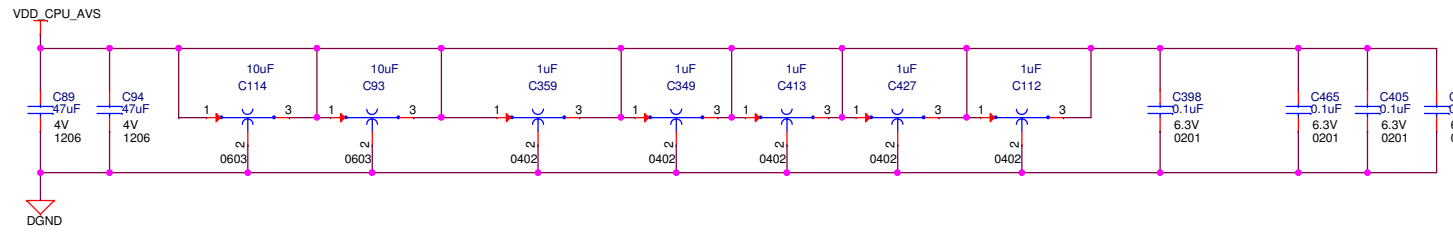
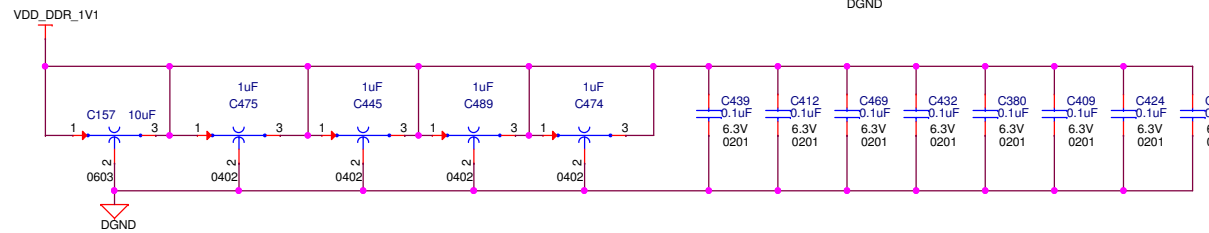
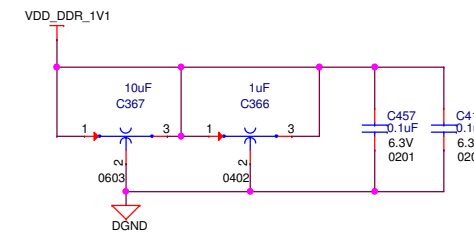
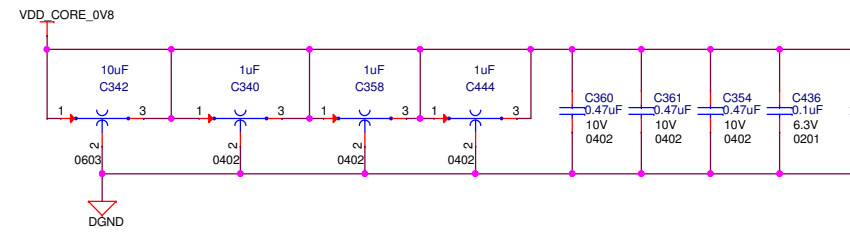
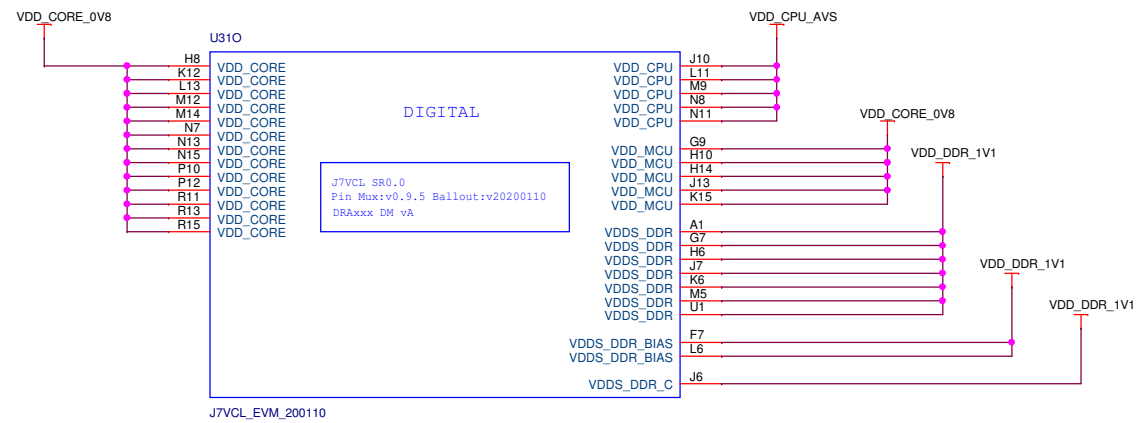
**Note:**

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance ( $Z_t$ ).

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# DIGITAL POWER 3



**Note:**

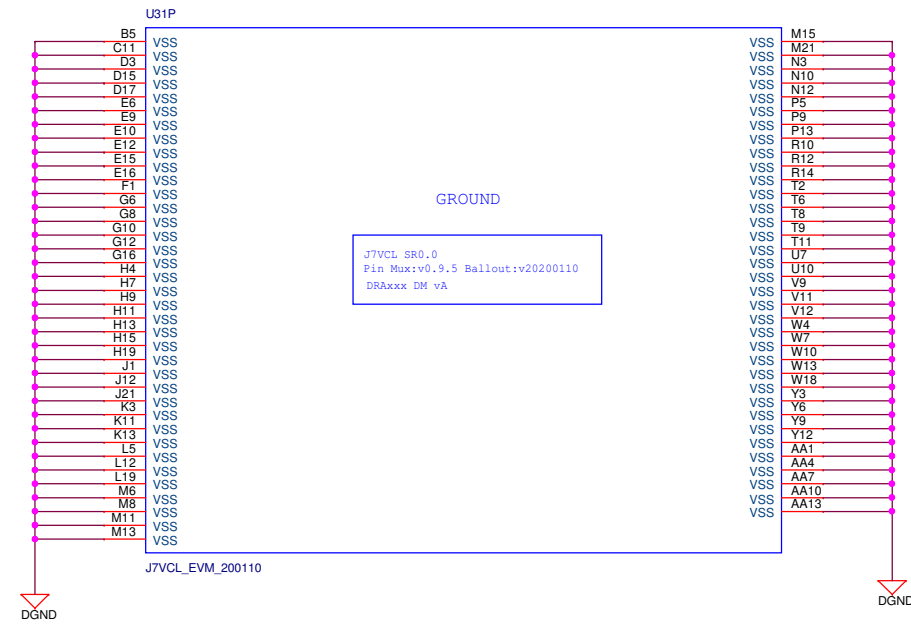
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Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

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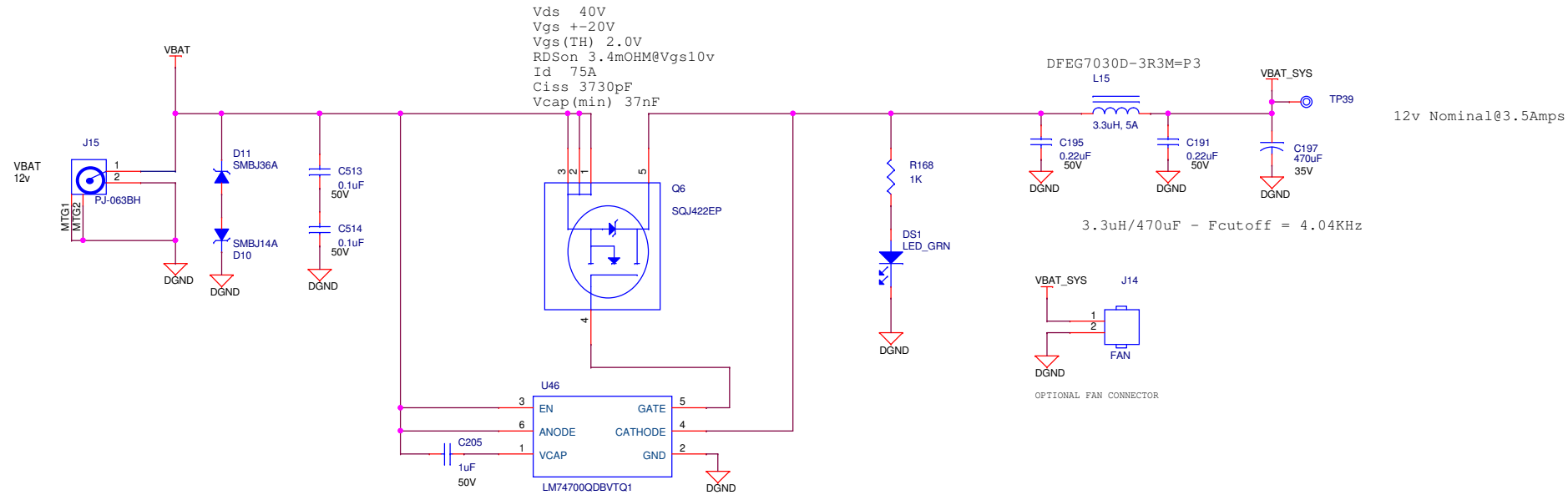
# SOC GROUND



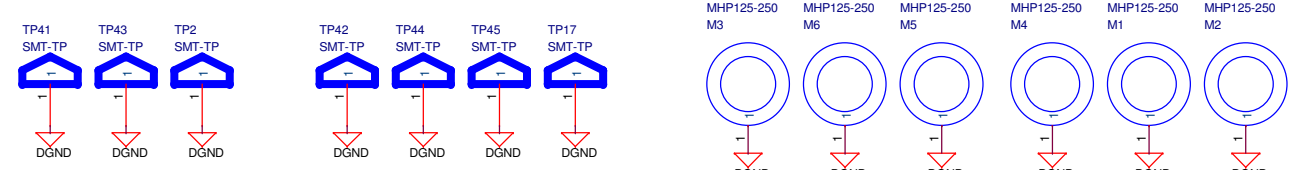
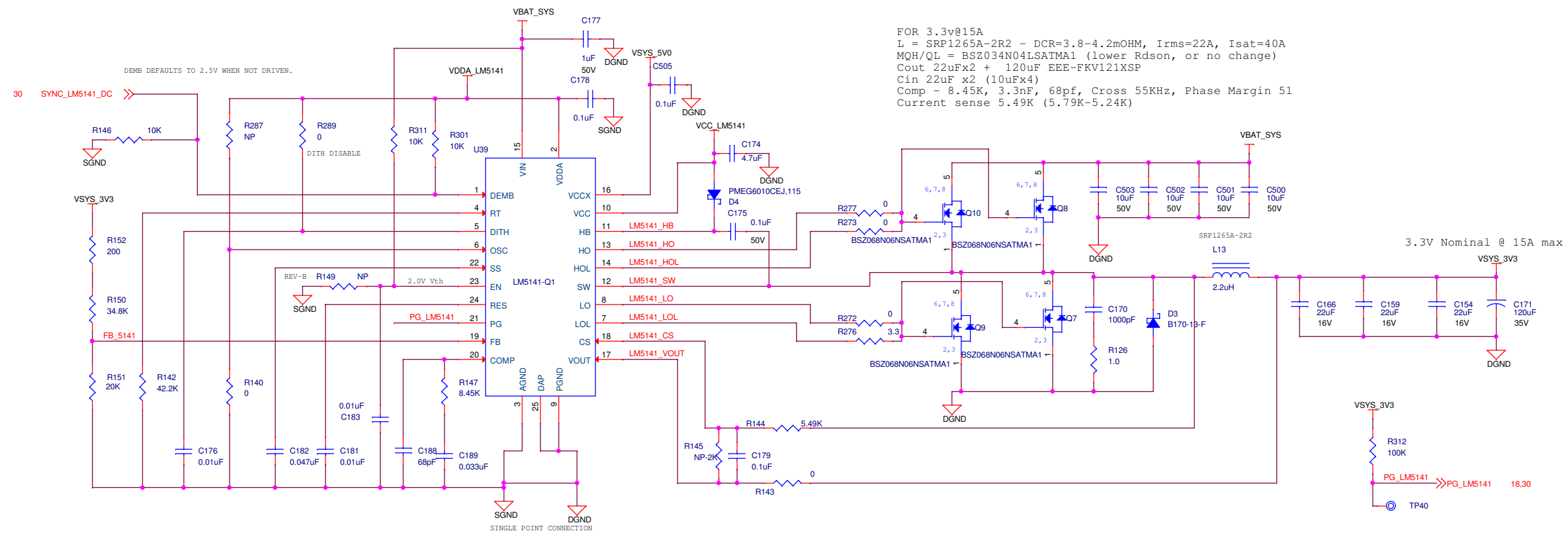
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# INPUT PROTECTION AND FILTER

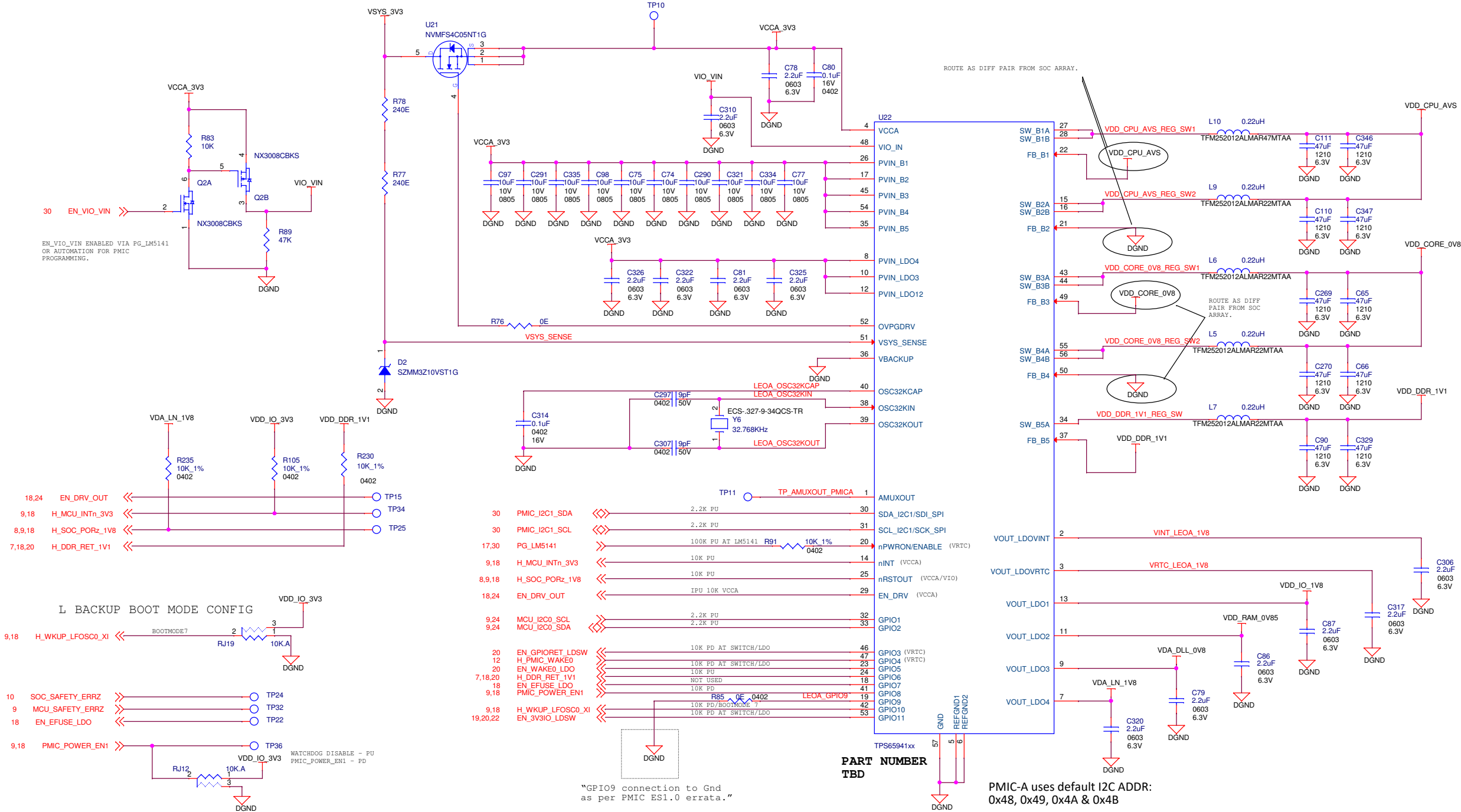


# STAGE-1 3.3V POWER



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# PMIC- A



"GPIO9 connection to Gnd as per PMIC ES1.0 errata."

PART NUMBER TBD

PMIC-A uses default I2C ADDR: 0x48, 0x49, 0x4A & 0x4B

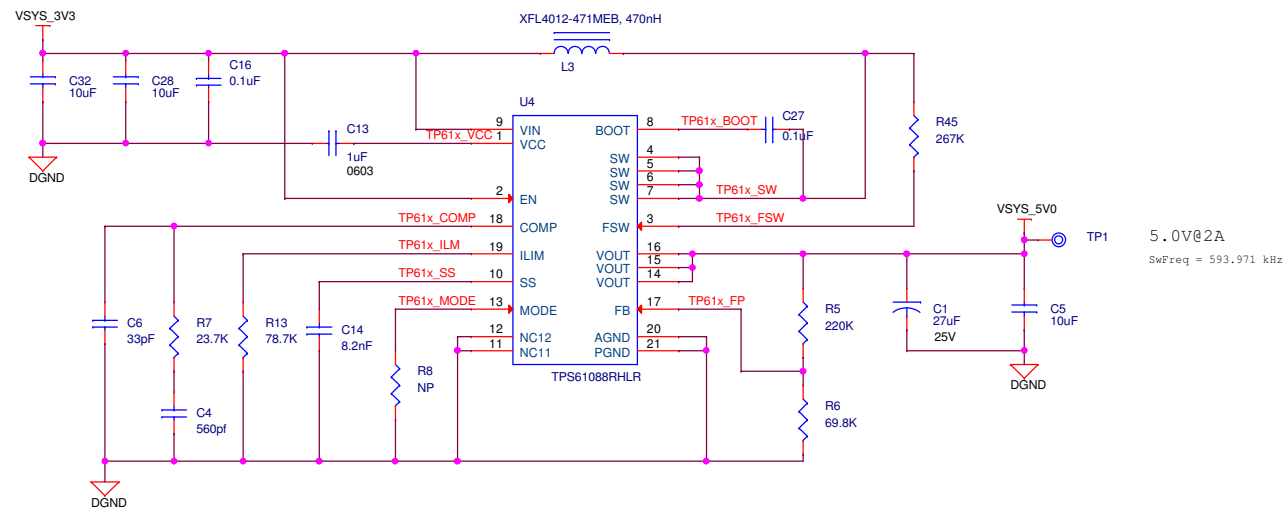
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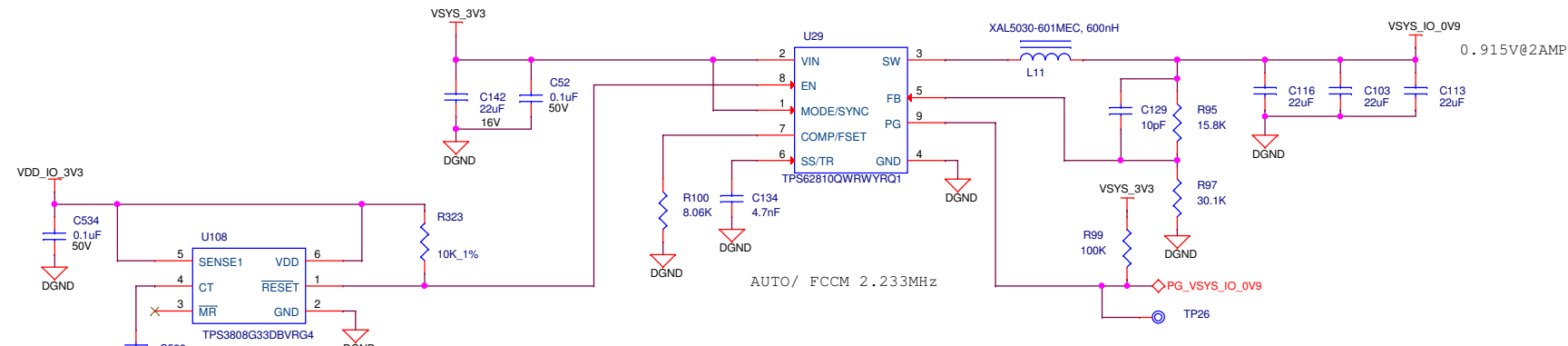
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CAN/USB-HOST (OPTIONAL)



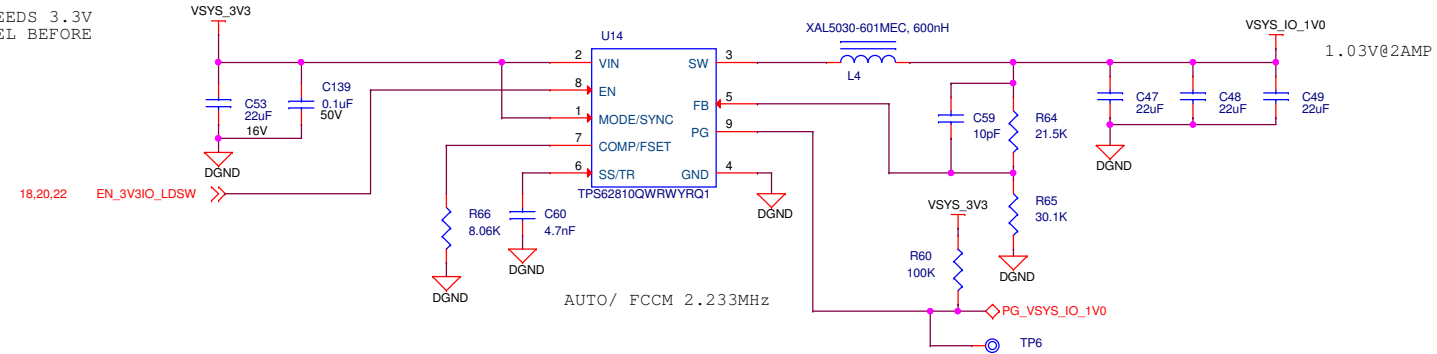
VSYS\_5V0 HAS TO BE ON WITH VDD\_GPIORET\_3V3 TO SUPPORT CAN WAKE UP. OR IT COULD BE ALWAYS ON.  
REV-B, VSYS\_5V0 TO ALWAYS ON.

RTL9068ABD SWITCH



RTL9xx NEEDS 3.3V FULL LEVEL BEFORE 0.9V.

DP83TG720 PHY



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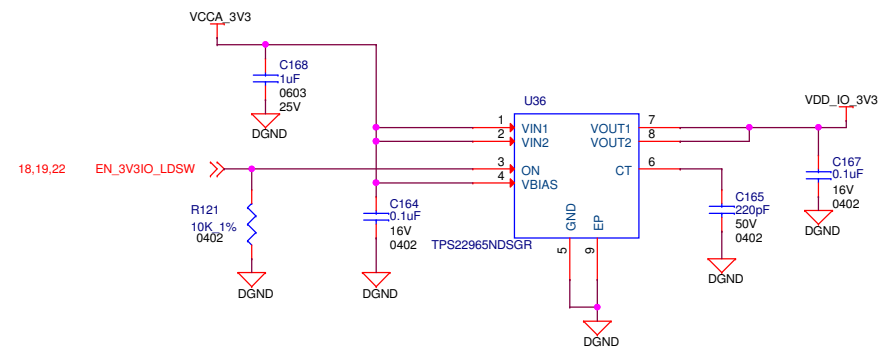
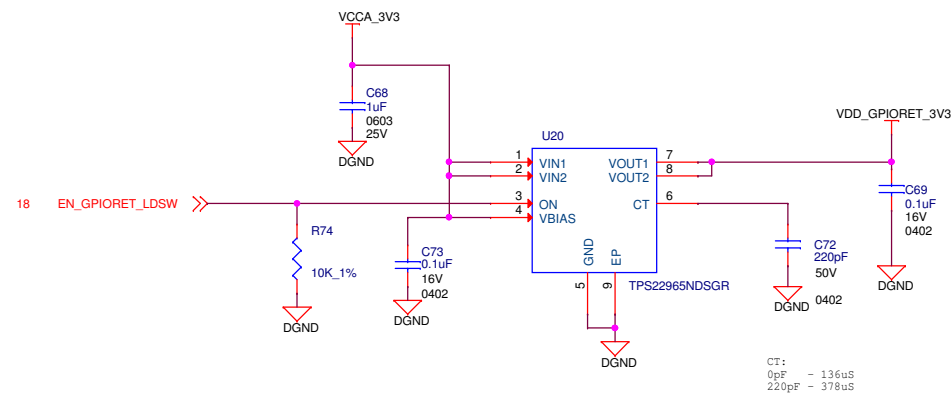
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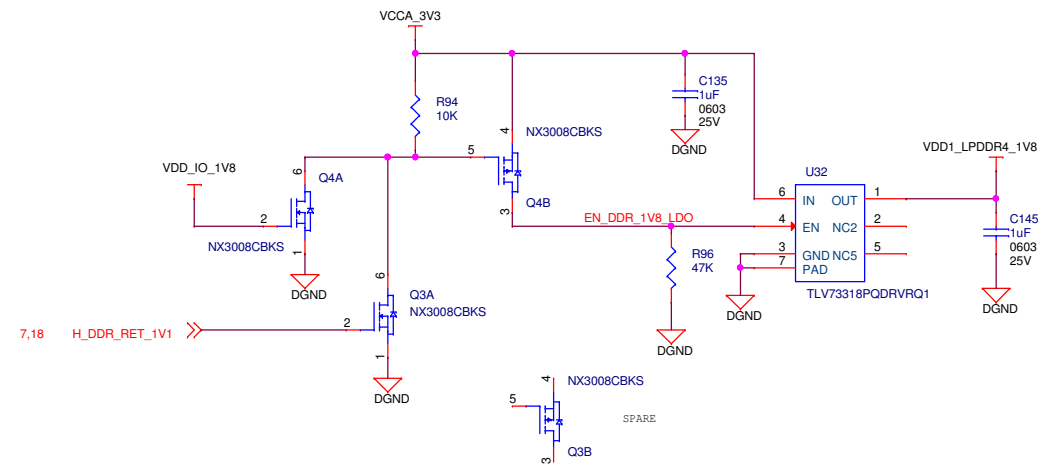
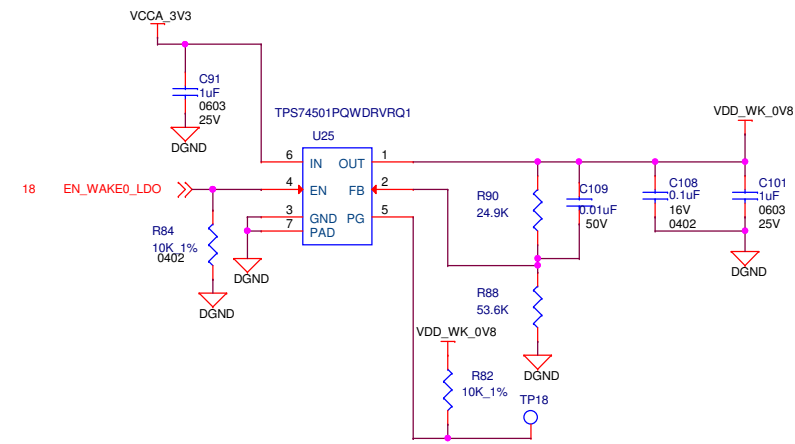
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# LOAD SWITCHES

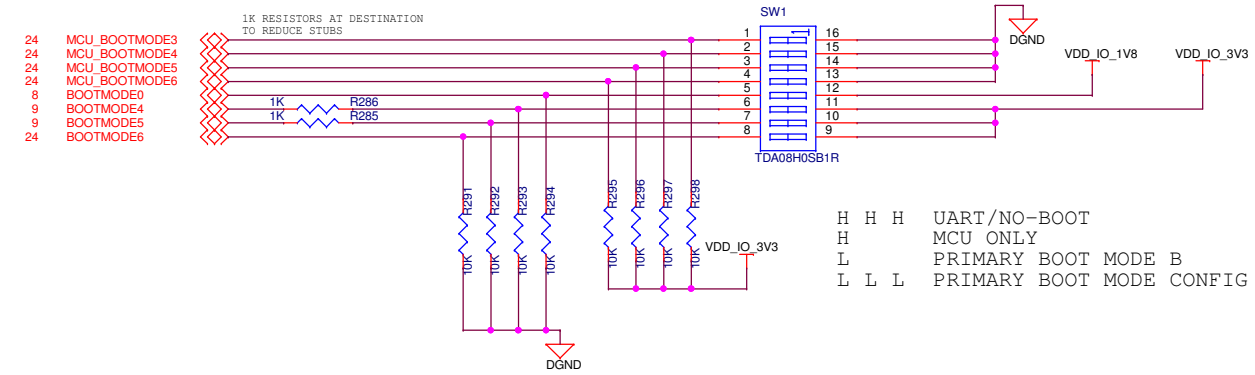


# LDO's



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# BOOT MODE SELECTION



BOOTMODE [7:0]								MCU_BOOTMODE[9:0]										
7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	
BACKUP BOOT MODE CONFIG		PRIMARY BOOT MODE CONFIG			BACKUP BOOT MODE			Prim Boot Mode B	POST CONFIG		RSV	MMC ONLY	PRIMARY BOOT MODE A			PLL CONFIG		
NA	NA	NA	NA	NA	NA	NA	NA	1	1	0	1	0	0	1	0	0	0	OSPI
NA	NA	NA	NA	NA	NA	NA	NA	1	1	0	1	1	1	1	0	0	0	UART/NO-BOOT( default )
0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	OSPI
0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0	UART/NO-BOOT
0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	EMMC
0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	USB

PRIMARY BOOT MODE CONFIG		
OSPI		
6	SPEED	33HMz
5	ICLK	EXTERNAL
4	CSEL	CS 0
USB		
6	PORT	0
5	MODE	DFU
4	LANE SWAP	NO
UART		
6	RSV	
5	RSV	
4	PORT	MCU-0
EMMC		
6	PORT	0
5	BUS WIDTH	MAX
4	VOLTAGE	1.8V

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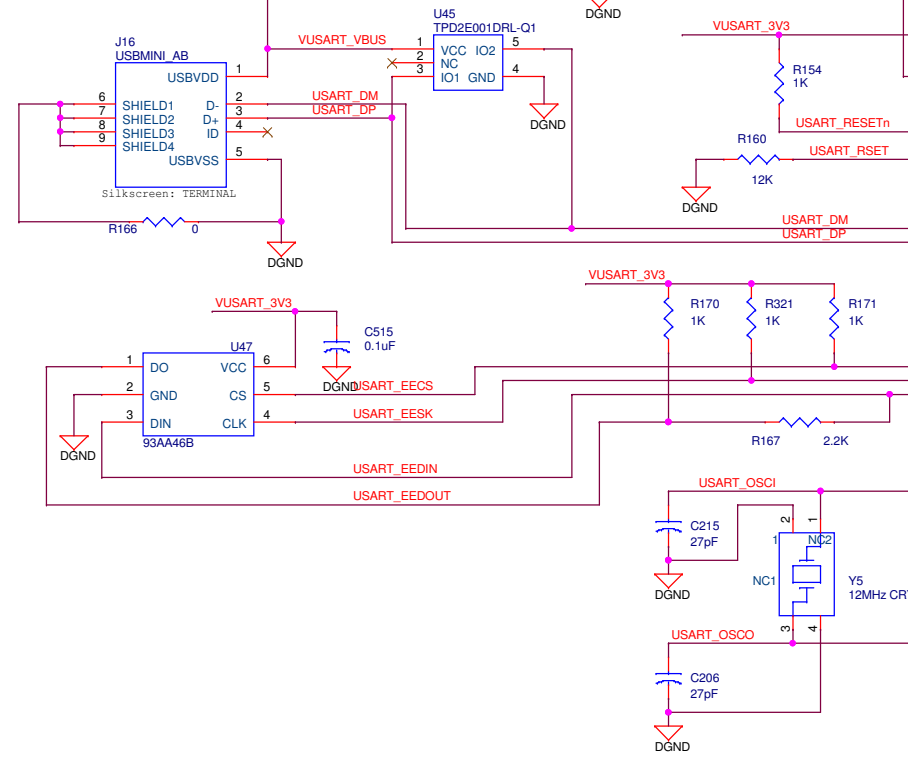
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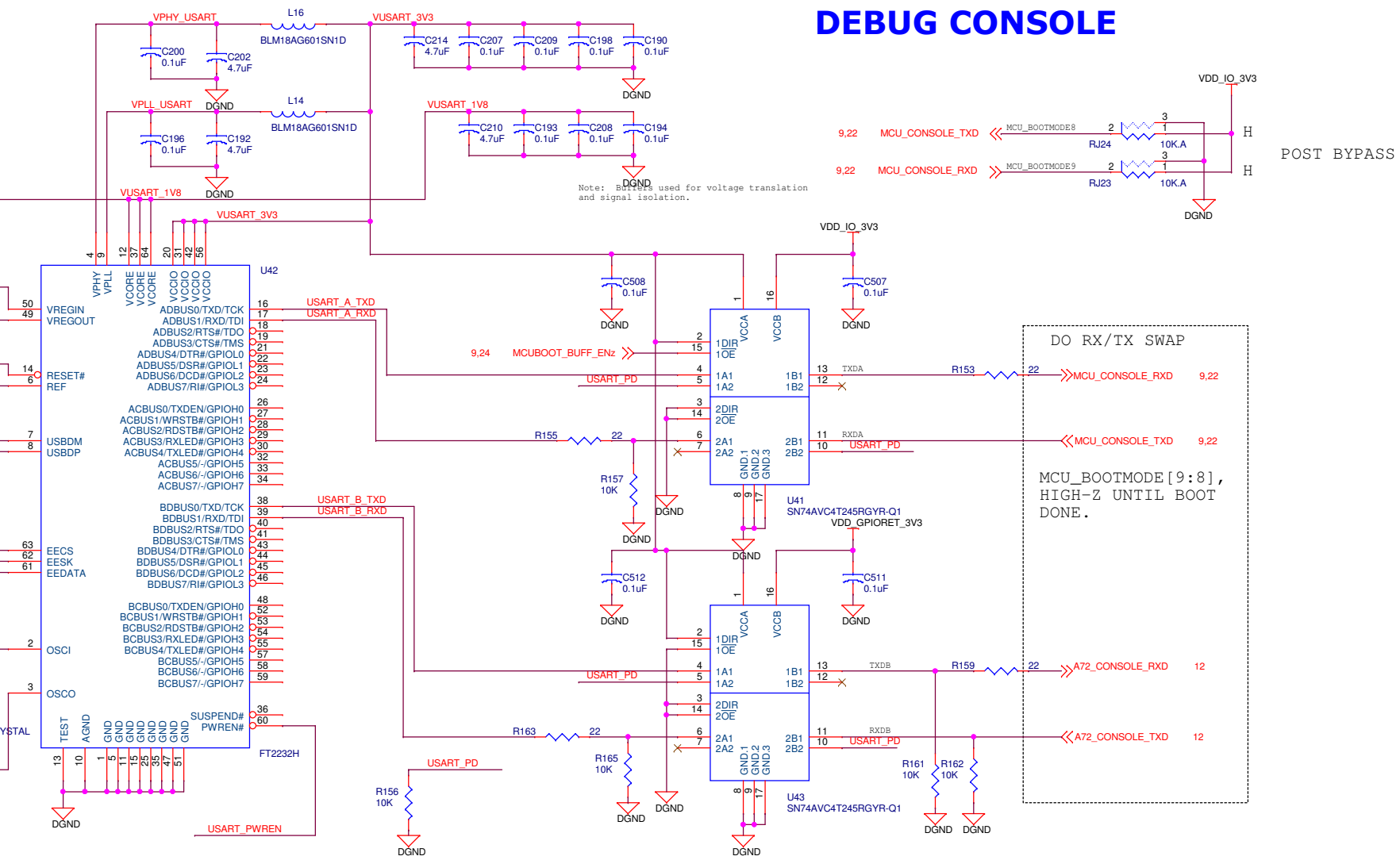
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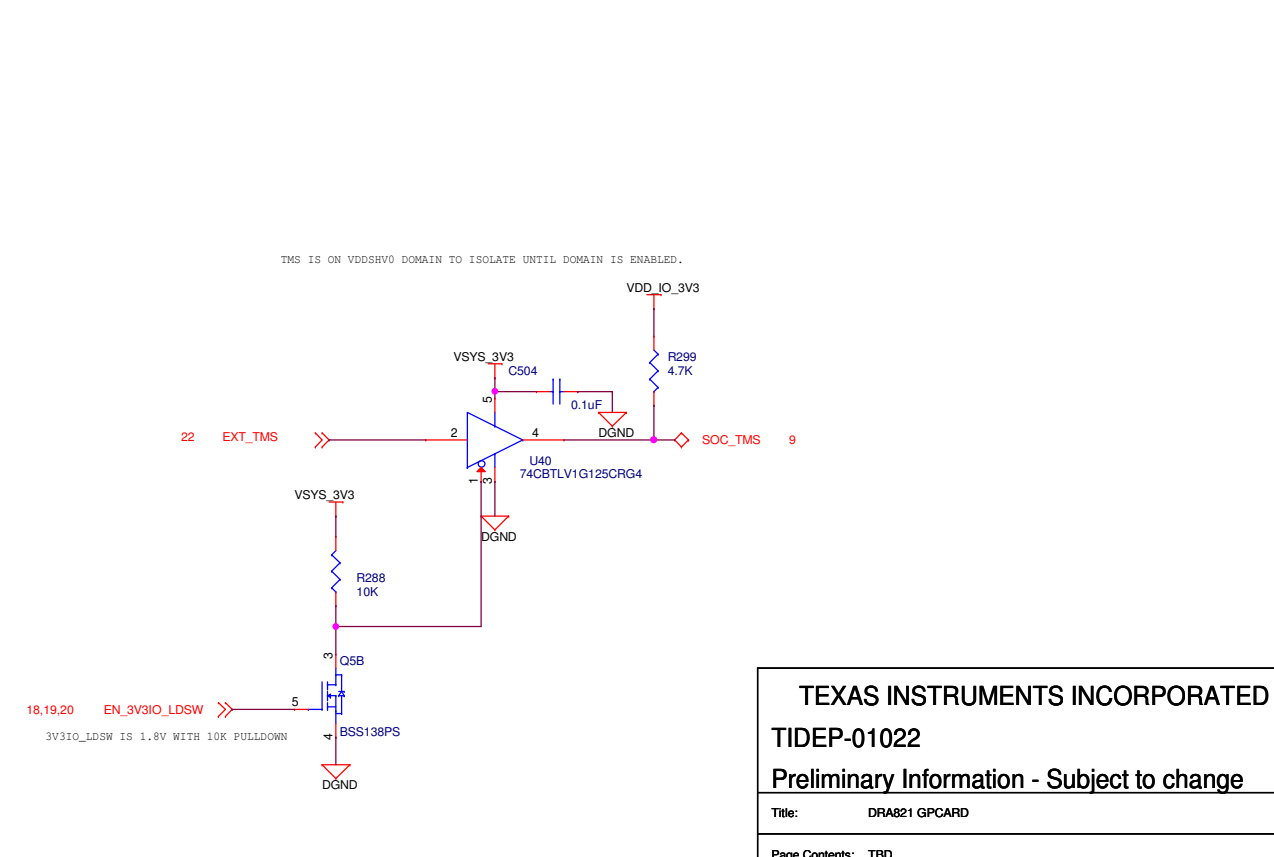
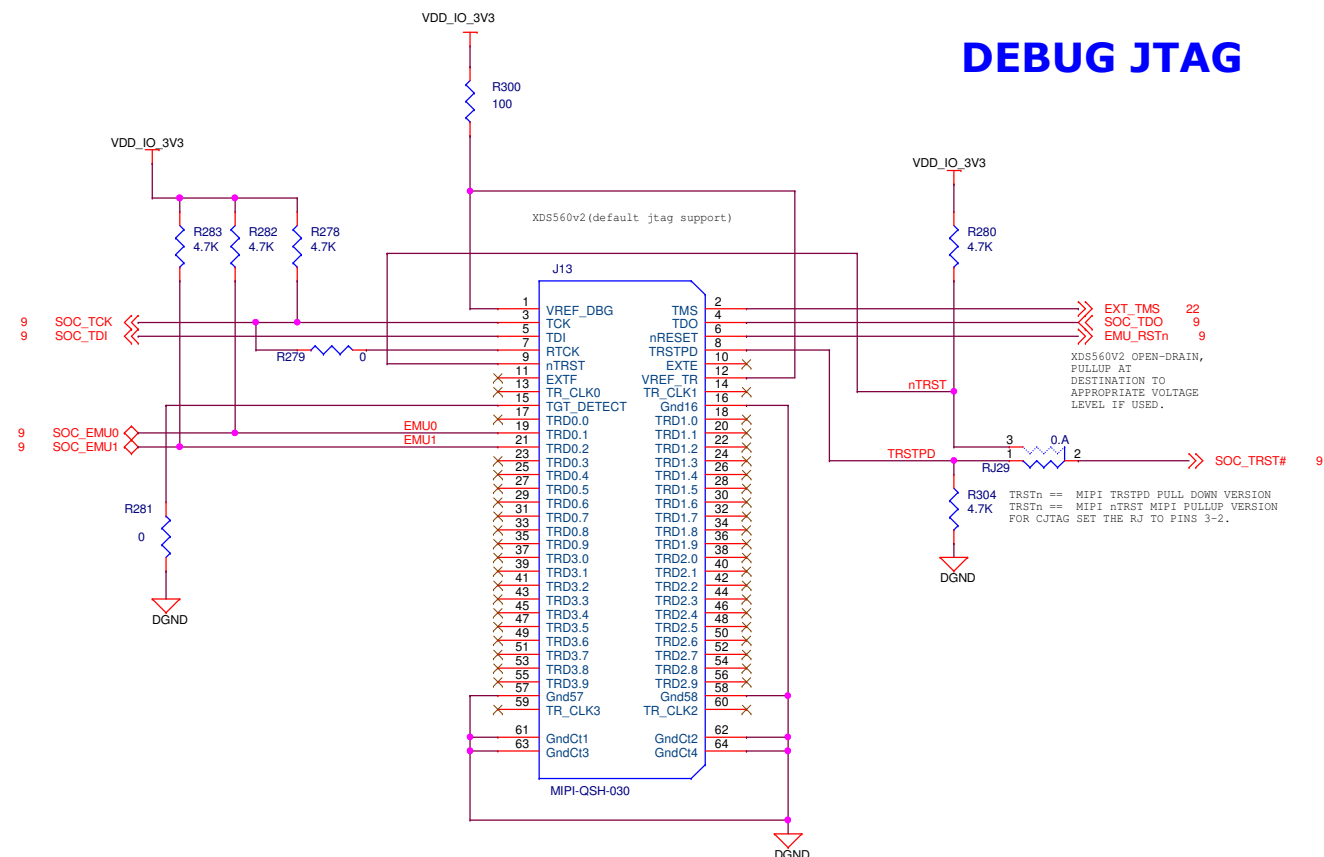
# Terminal Connector



# DEBUG CONSOLE

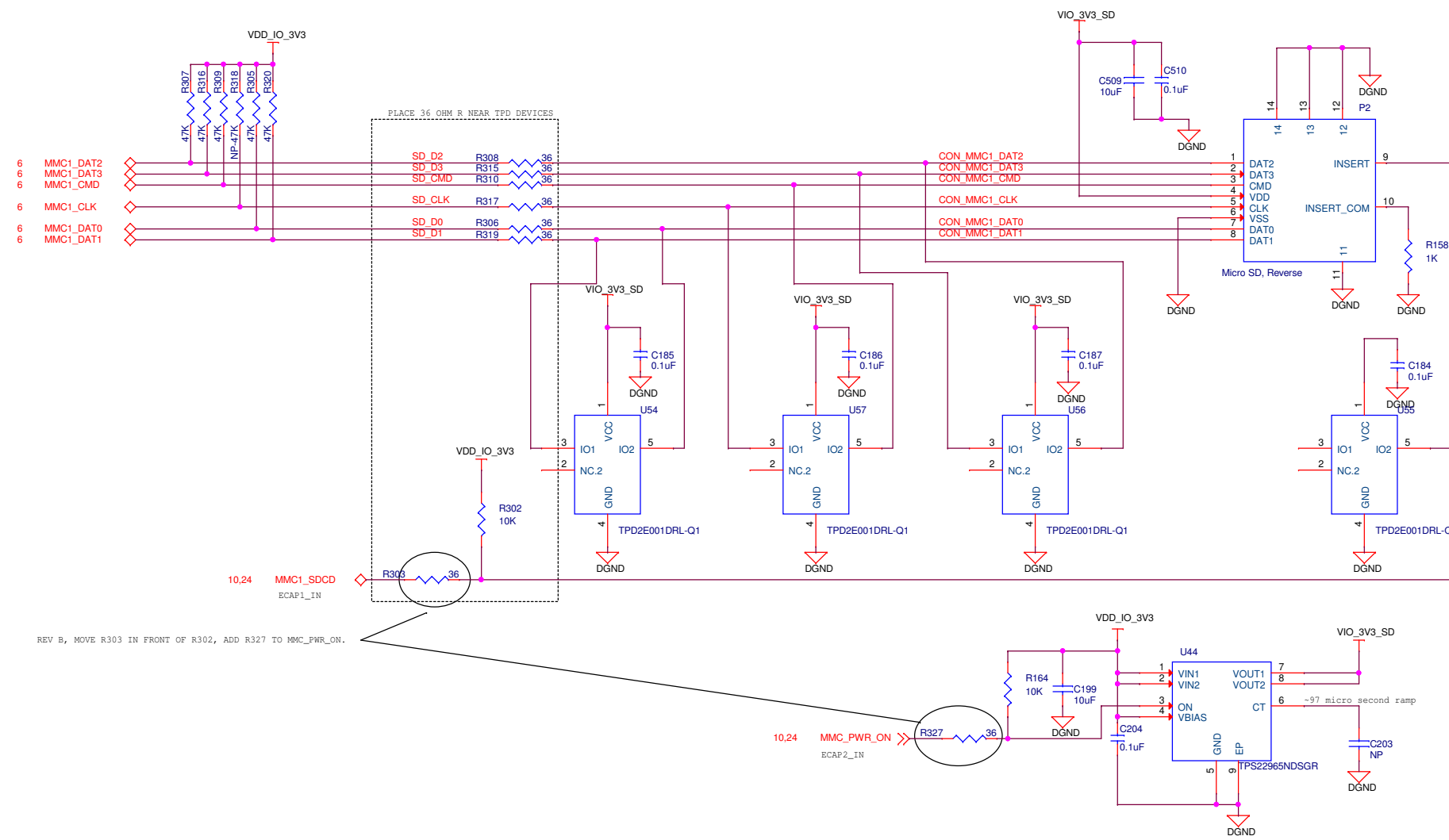


# DEBUG JTAG

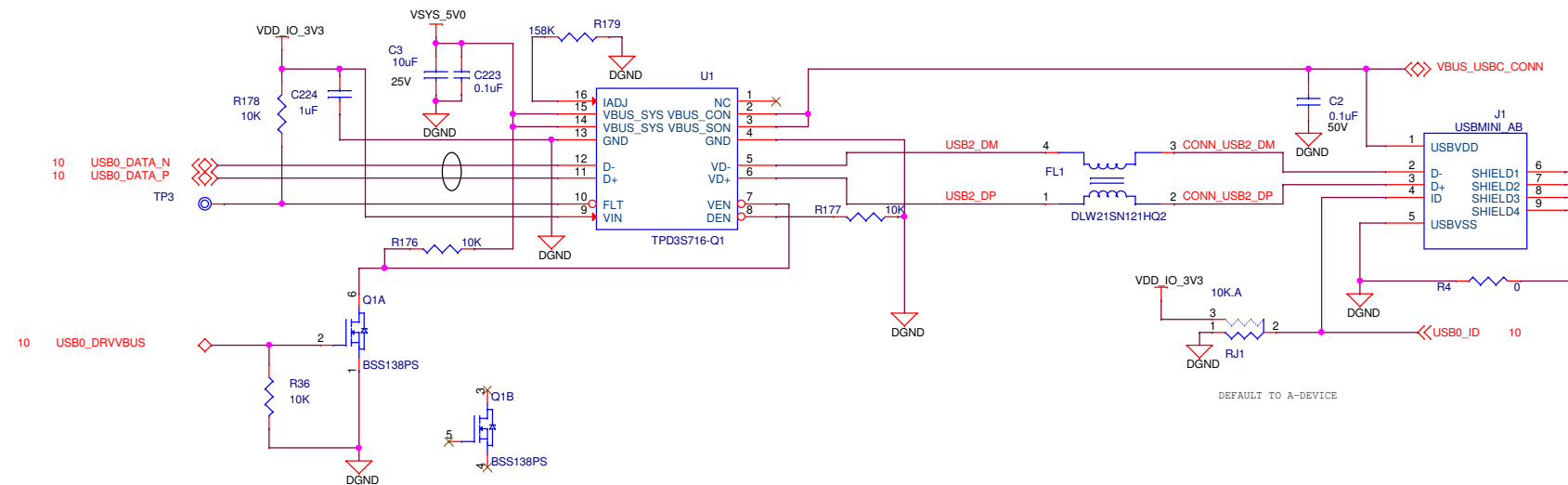


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# OPTIONAL SD CARD SUPPORT



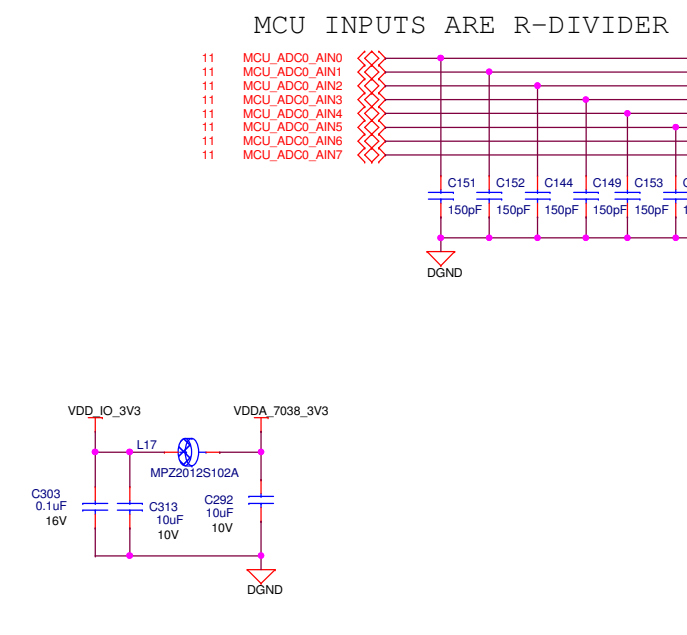
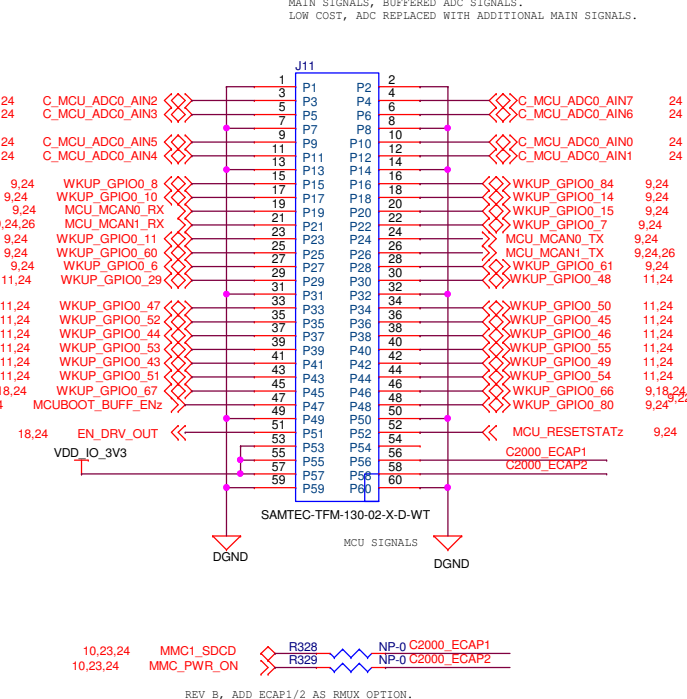
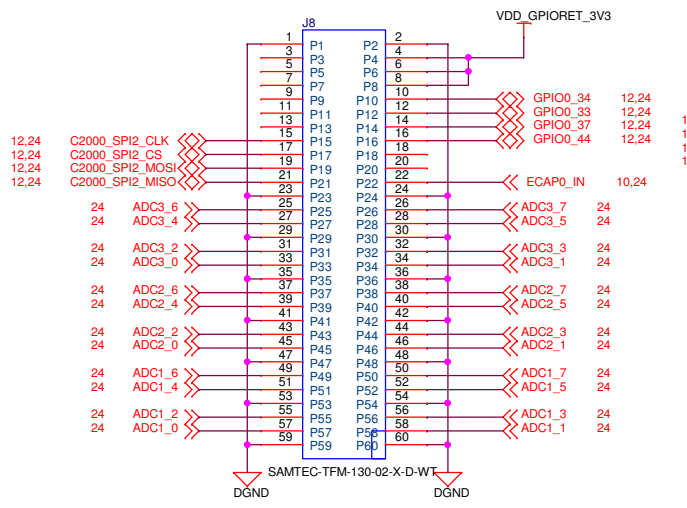
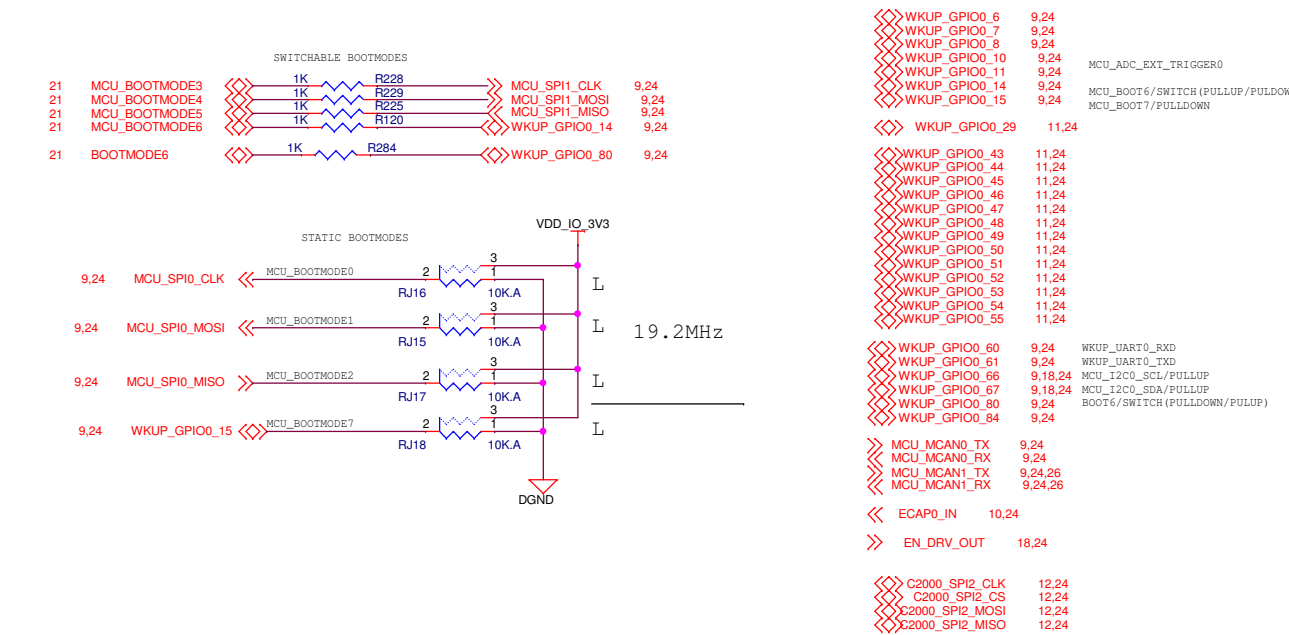
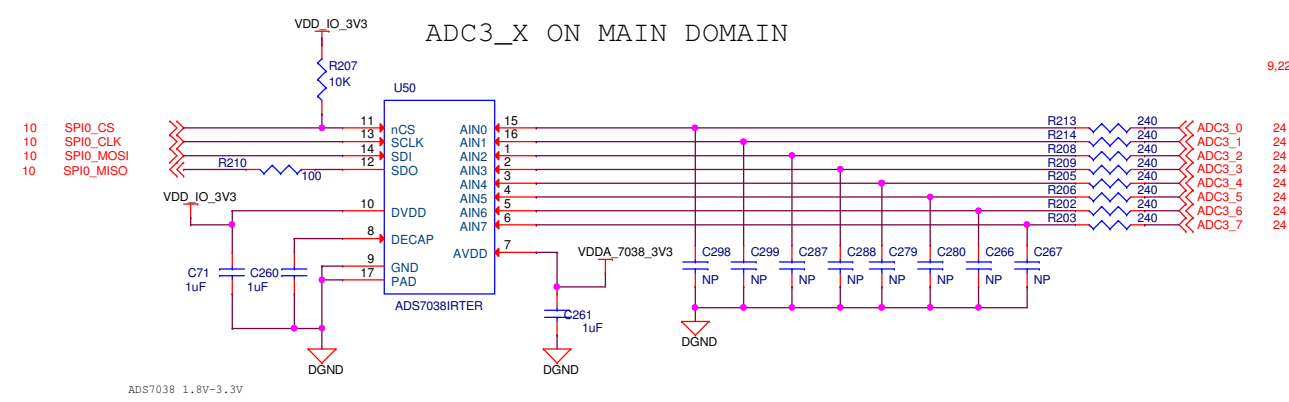
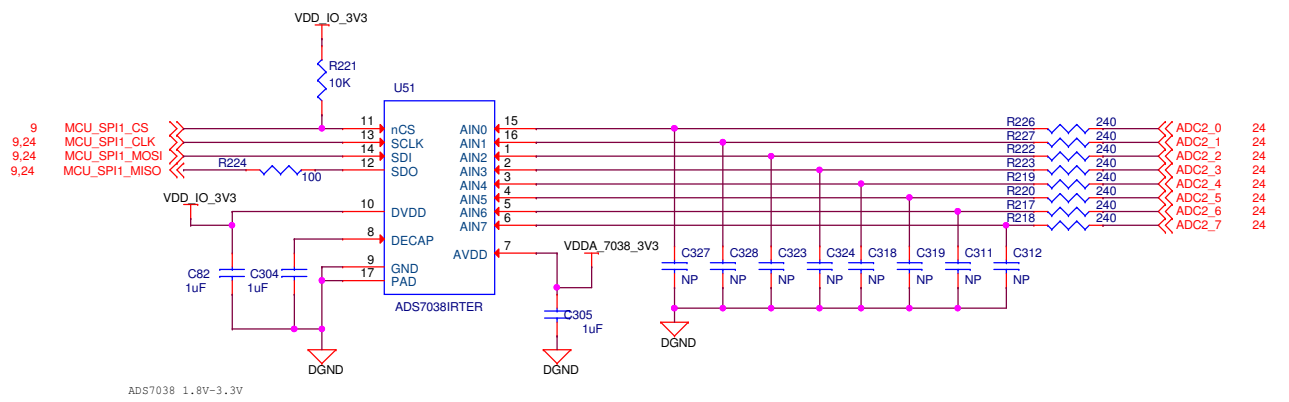
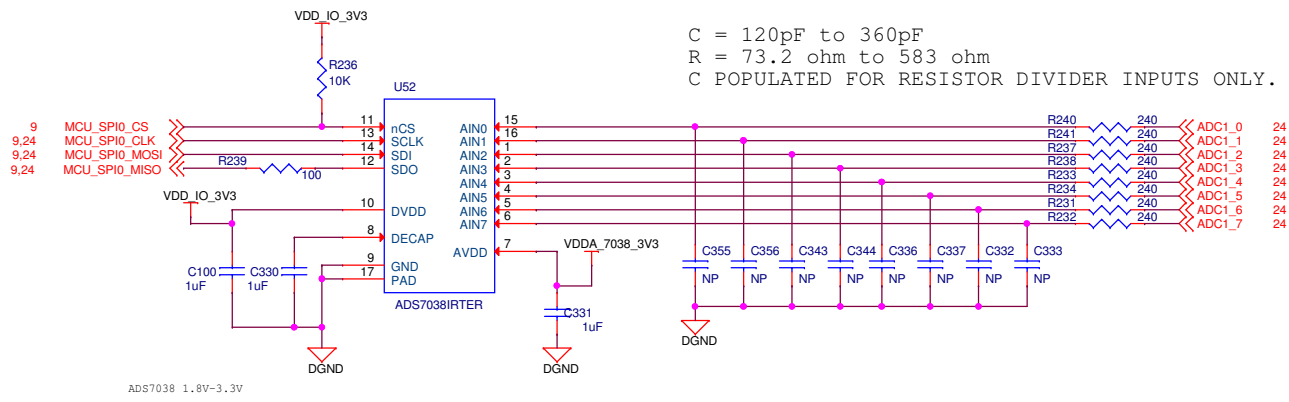
# USB PORT FOR DEBUG



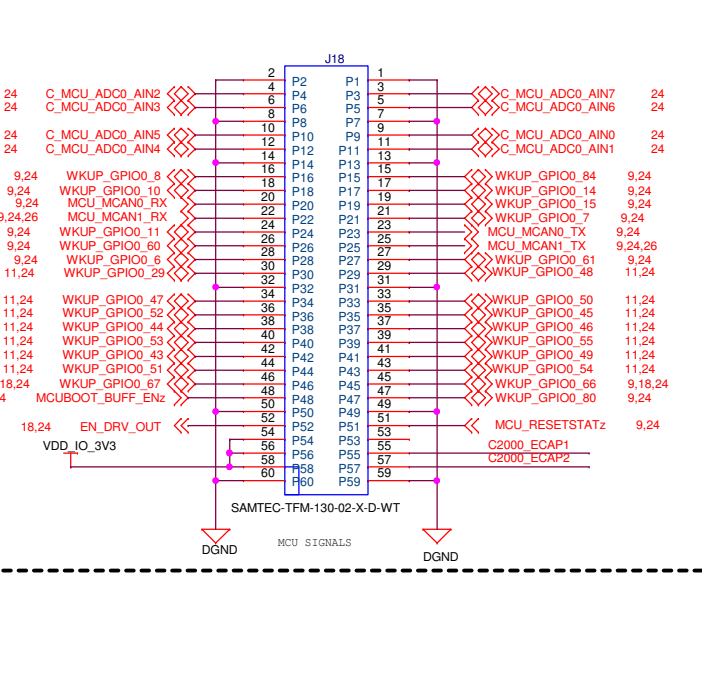
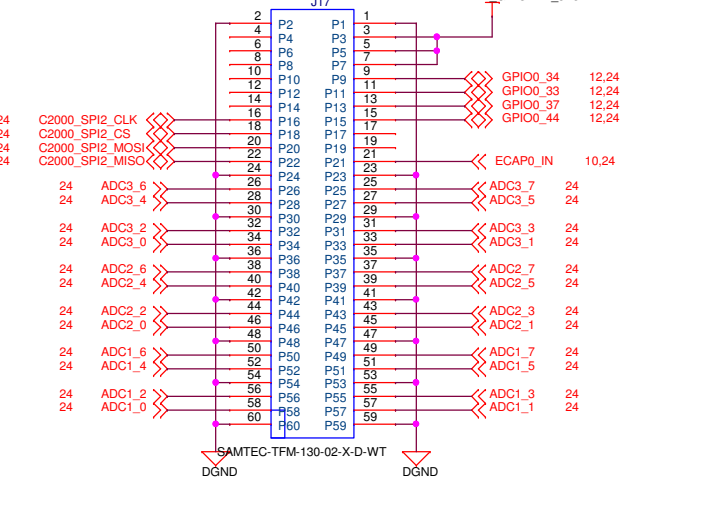
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# ADS7038 - AVDD IS FILTERED DVDD COMMON SUPPLY

C = 120pF to 360pF  
R = 73.2 ohm to 583 ohm  
C POPULATED FOR RESISTOR DIVIDER INPUTS ONLY.



OPTIONAL BOTTOM SIDE MOUNT, MIRRORED CONNECTOR (NO-POP).



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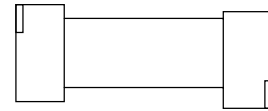
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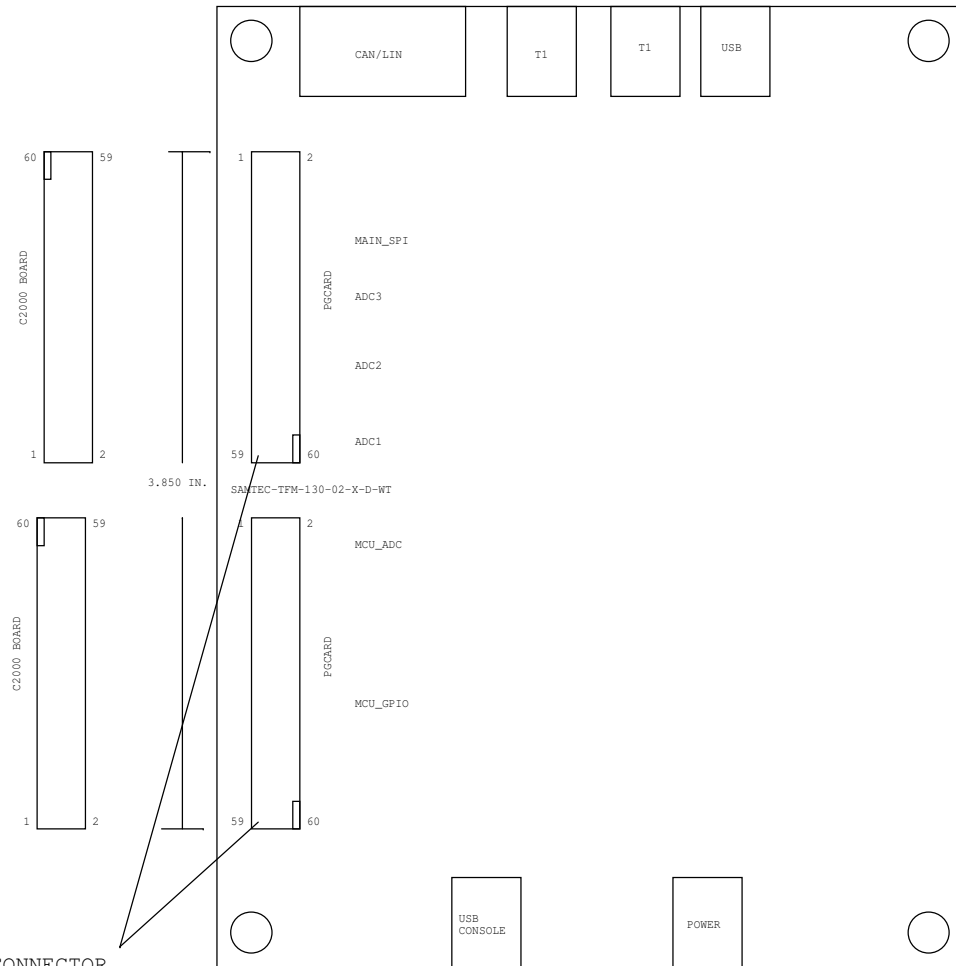
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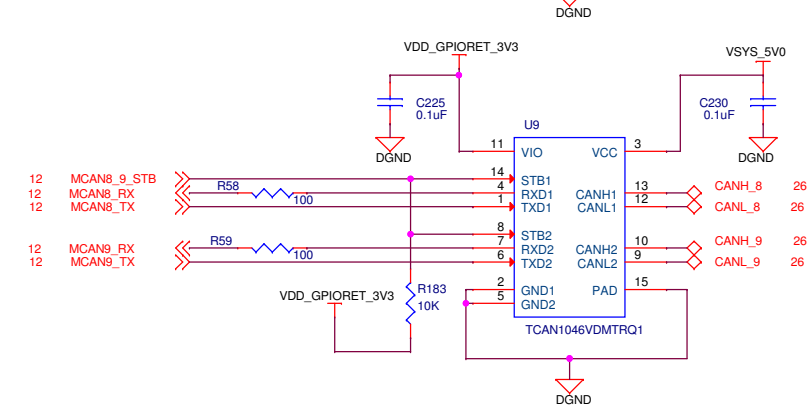
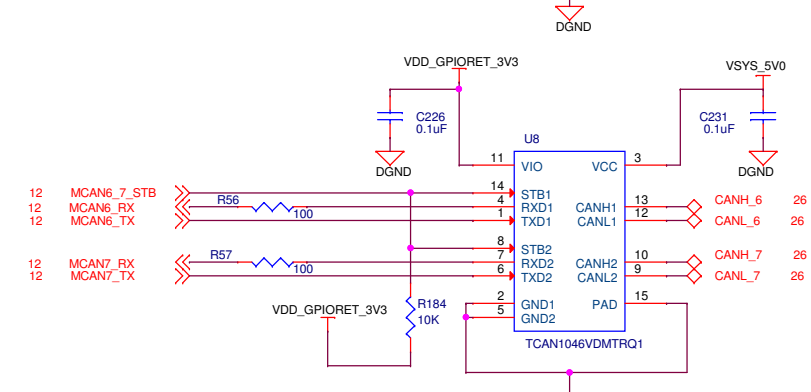
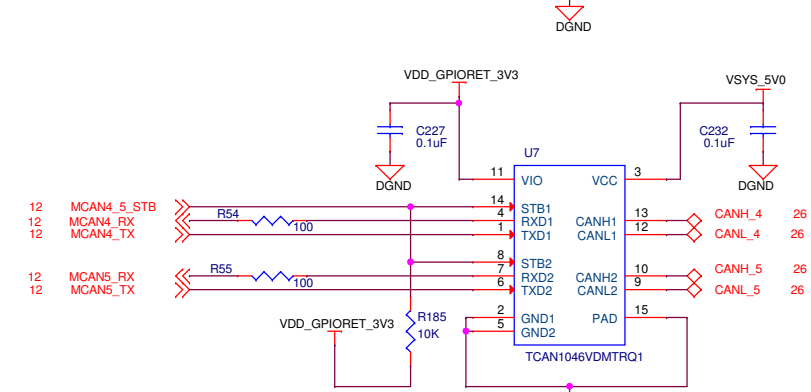
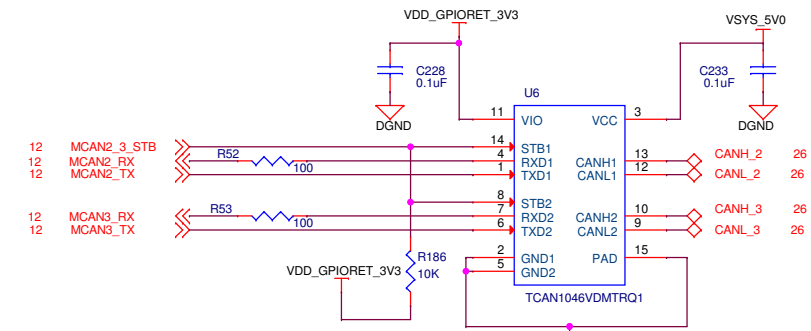
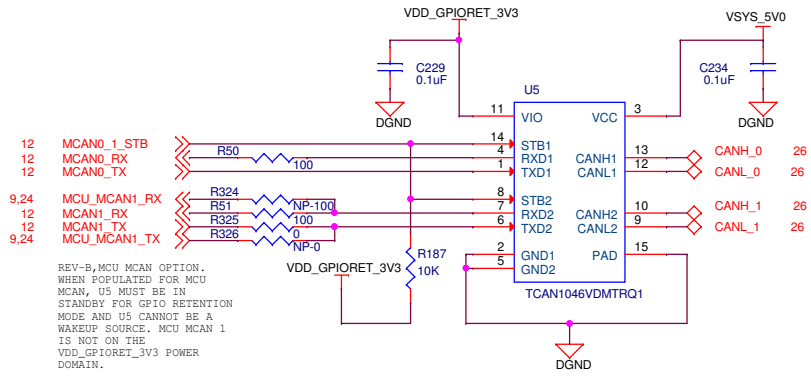
CONNECTOR PINNING FROM PGCARD TO C2000 CARD SHOULD BE MIRRORED:  
SEE sfsdx-xx-xxx-xx-xx.xx-xx-xxx-mkt.pdf FOR CABLE DETAILS.



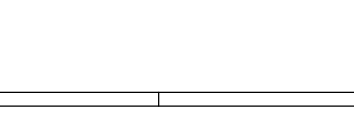
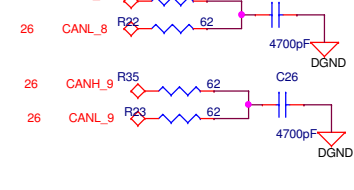
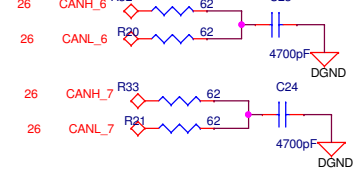
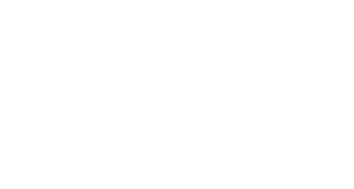
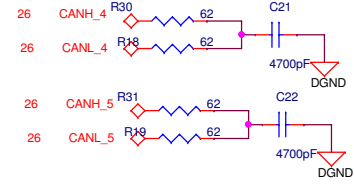
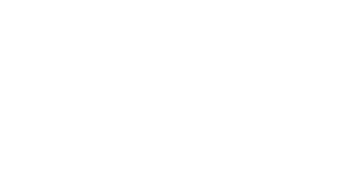
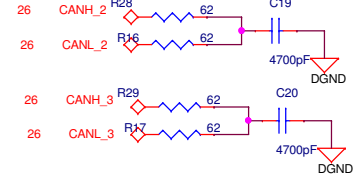
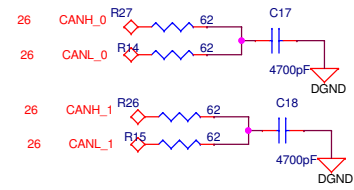
OPTIONAL CONNECTOR  
FOOTPRINT ON BOTTOM  
SIDE.

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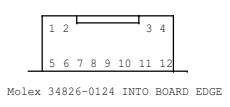
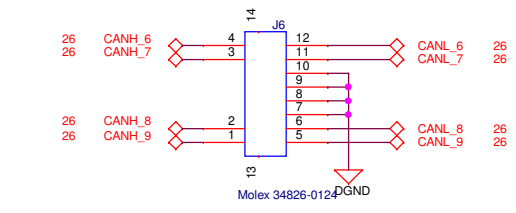
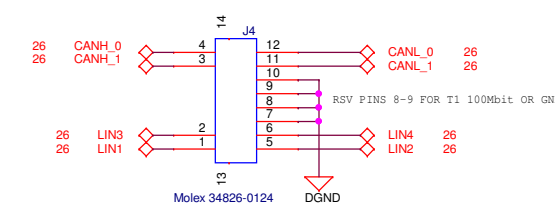
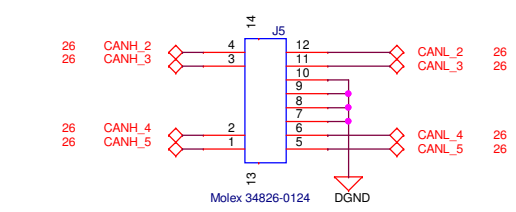
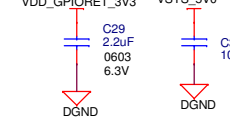
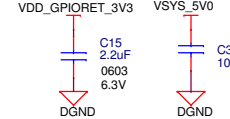
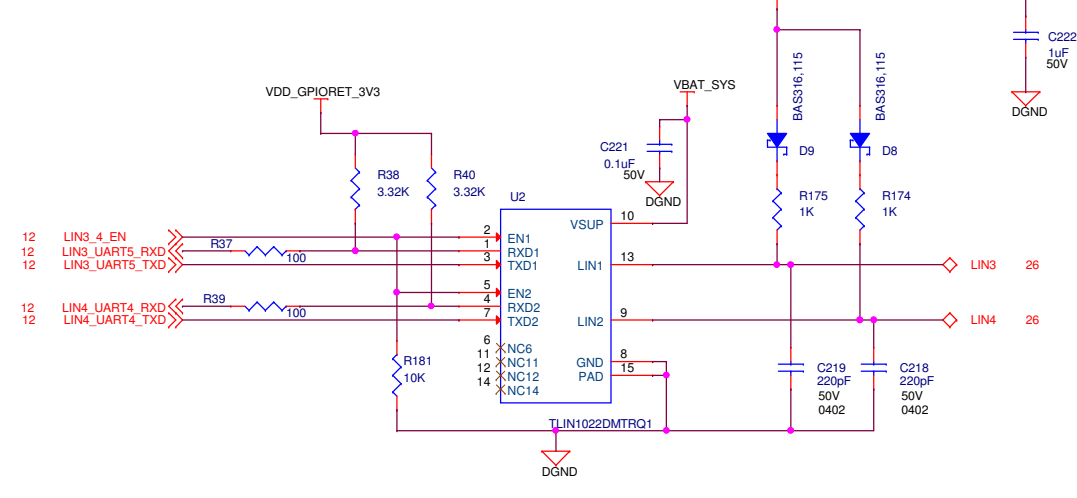
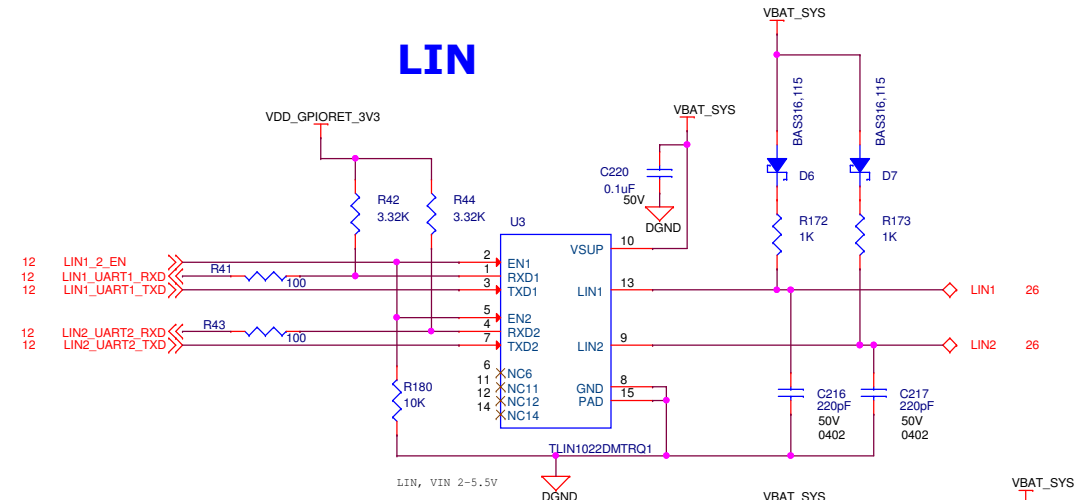
# CAN



CAN/LIN POWER UP IN STANDBY/DISABLED.  
CAN/LIN SUPPORT IO RETENTION AND ARE WAKEUP SOURCES.



# LIN



Molex 34826-0124 INTO BOARD EDGE

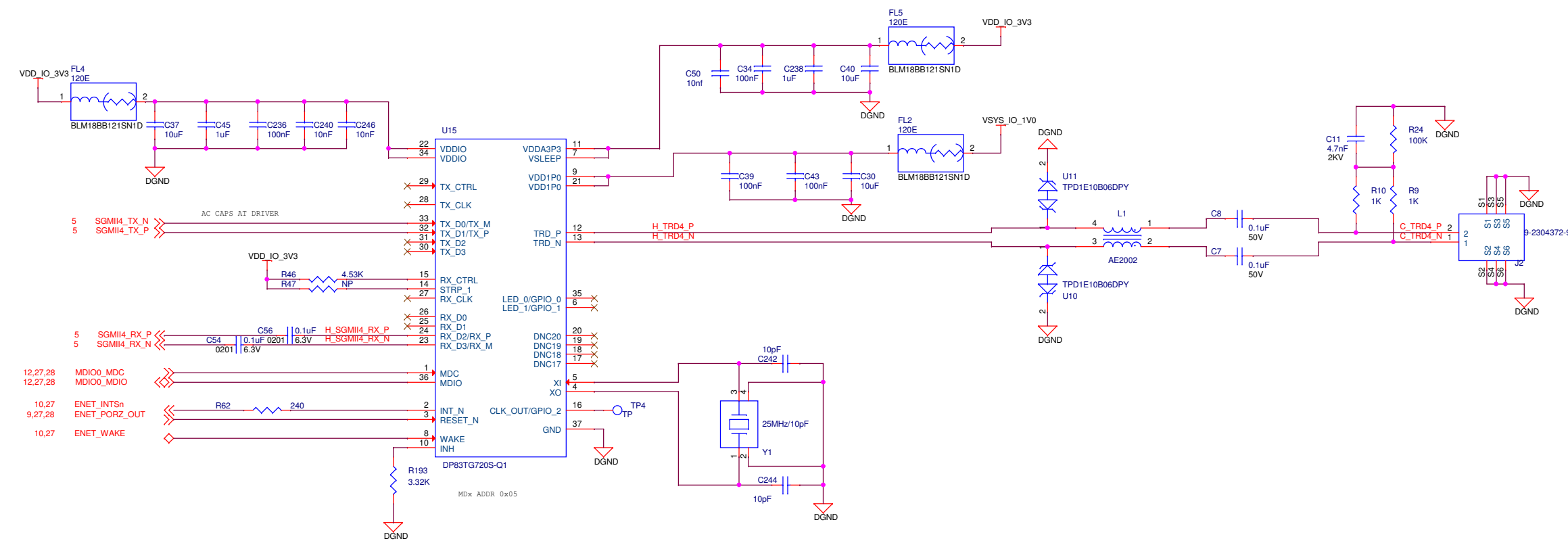
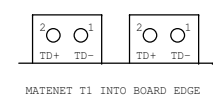
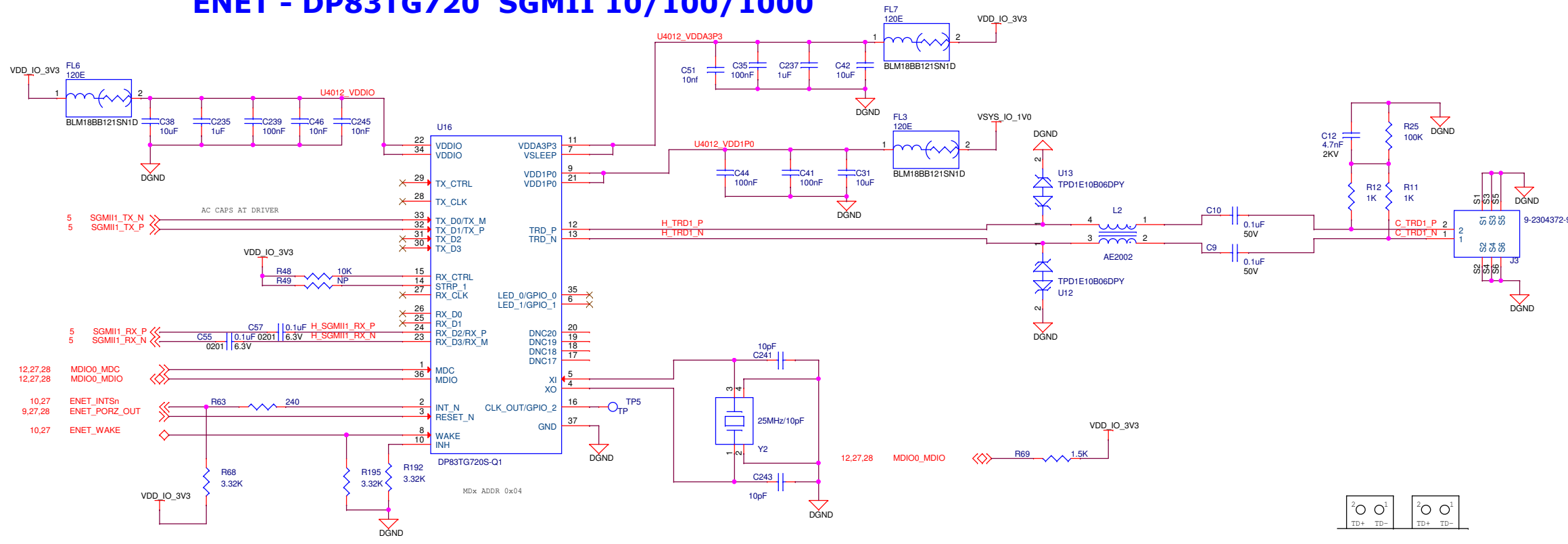
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# ENET - DP83TG720 SGMII 10/100/1000



PHY ADDRESS STRAPPING 3.3V IO

RX_CTRL	STRP_1
0	OPEN
4	10K
5	4.5K
8	OPEN
10	OPEN
12	10K
13	4.5K
14	10K
15	4.5K

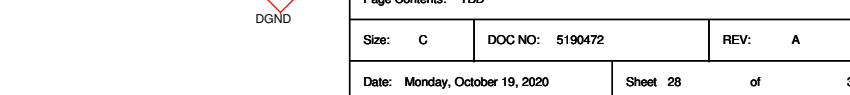
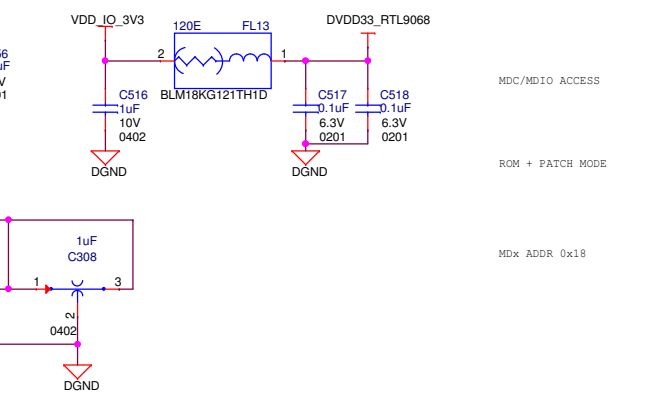
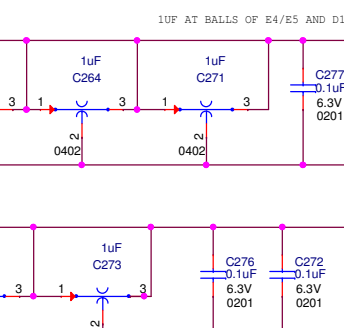
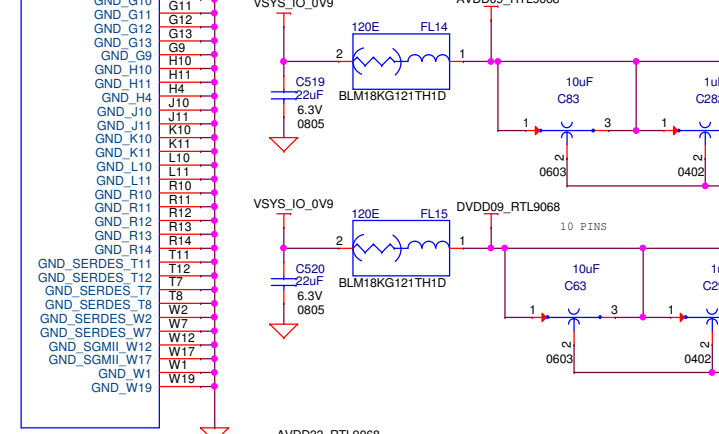
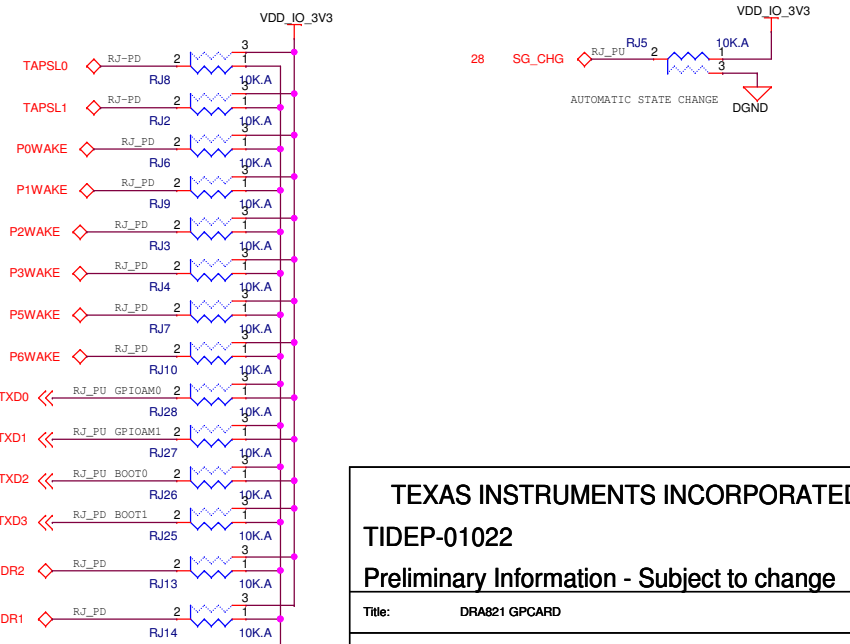
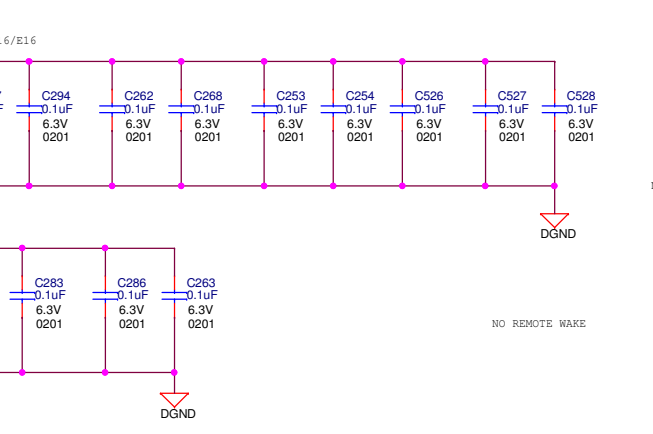
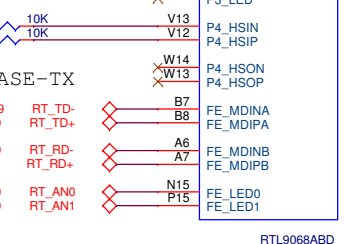
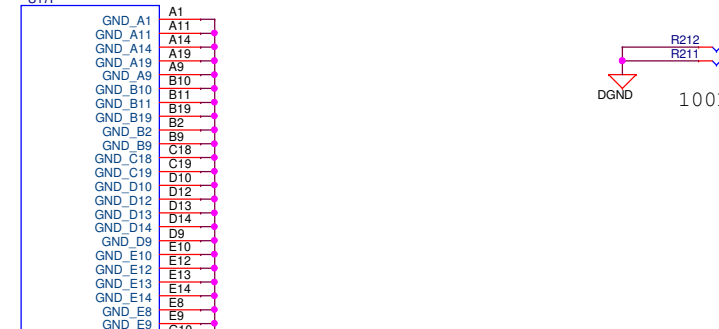
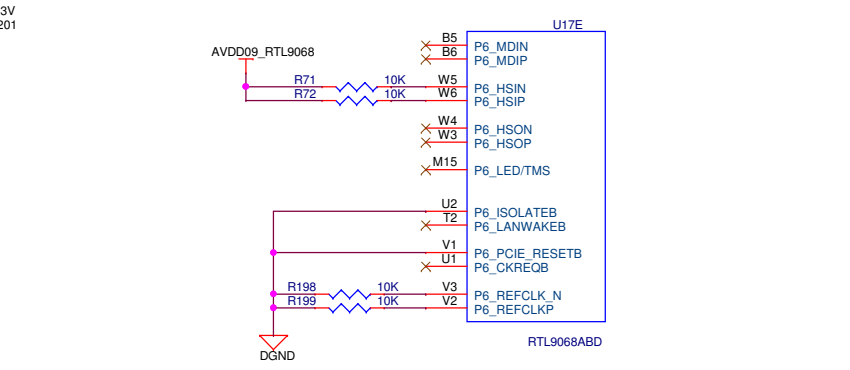
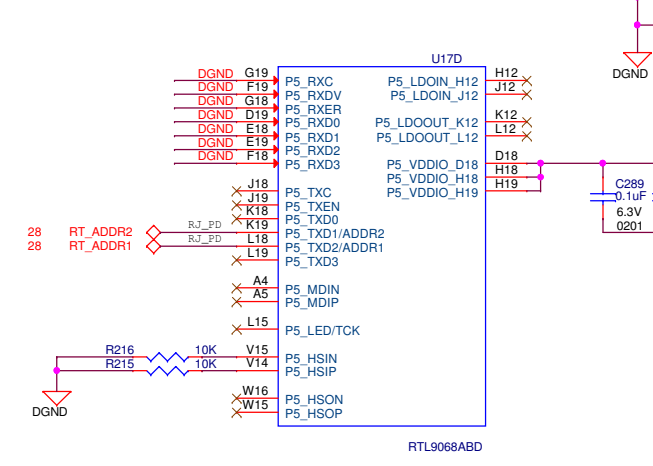
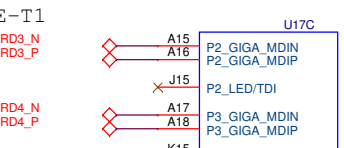
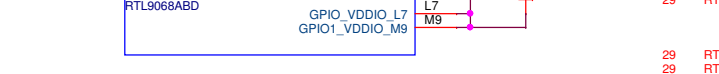
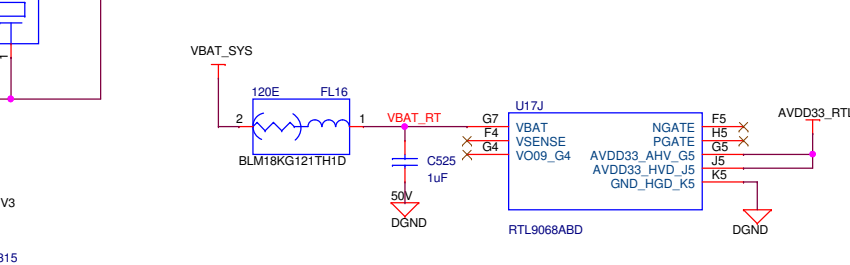
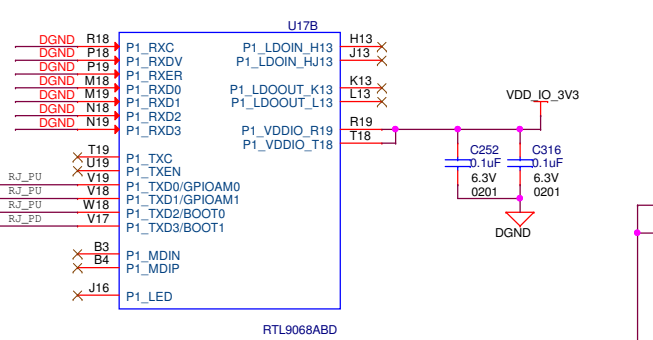
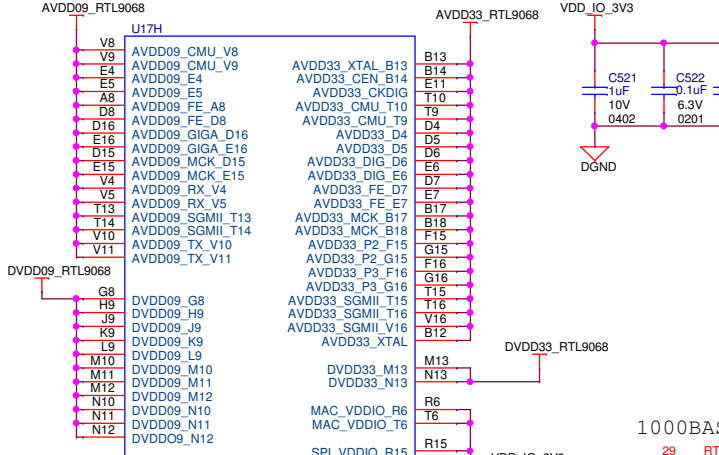
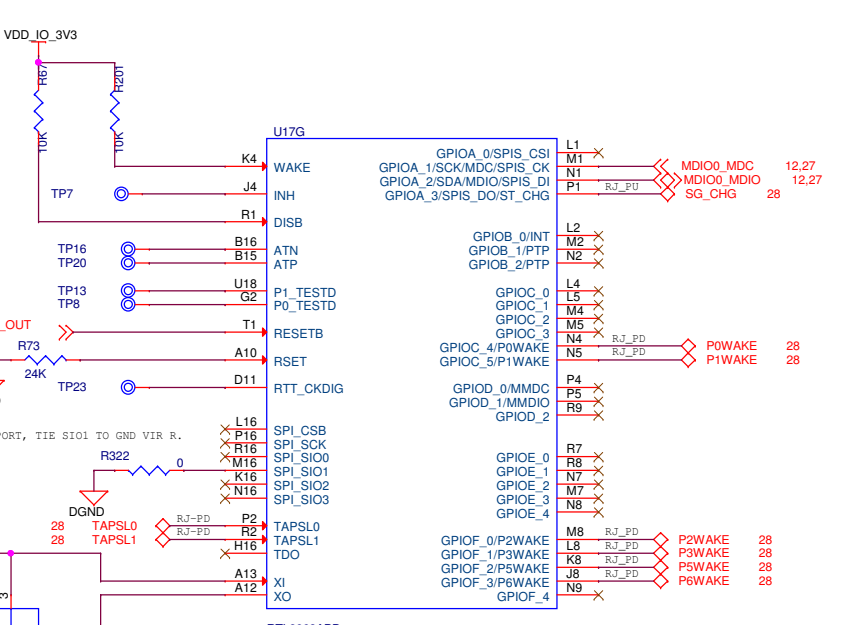
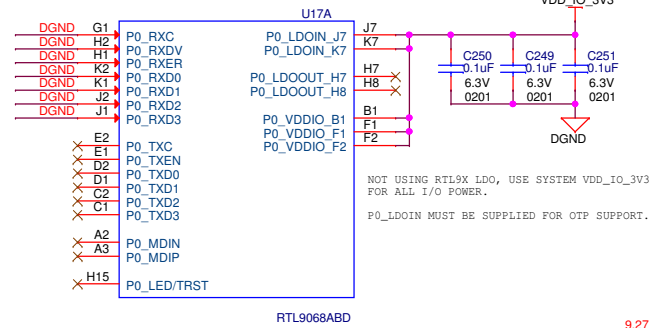
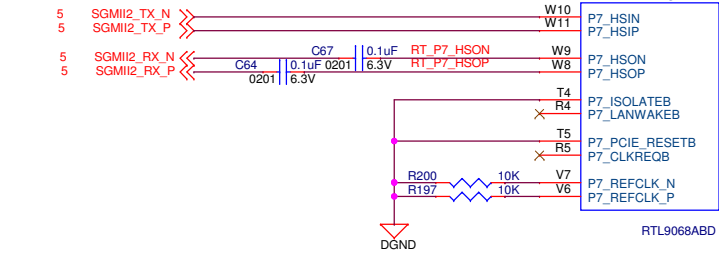
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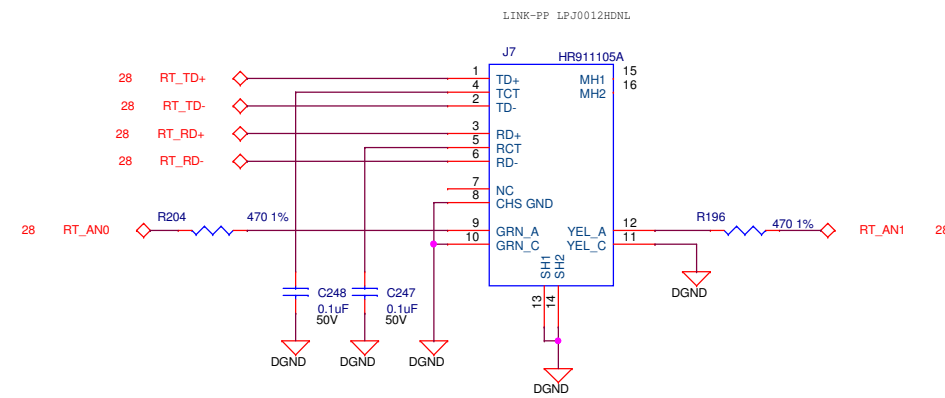
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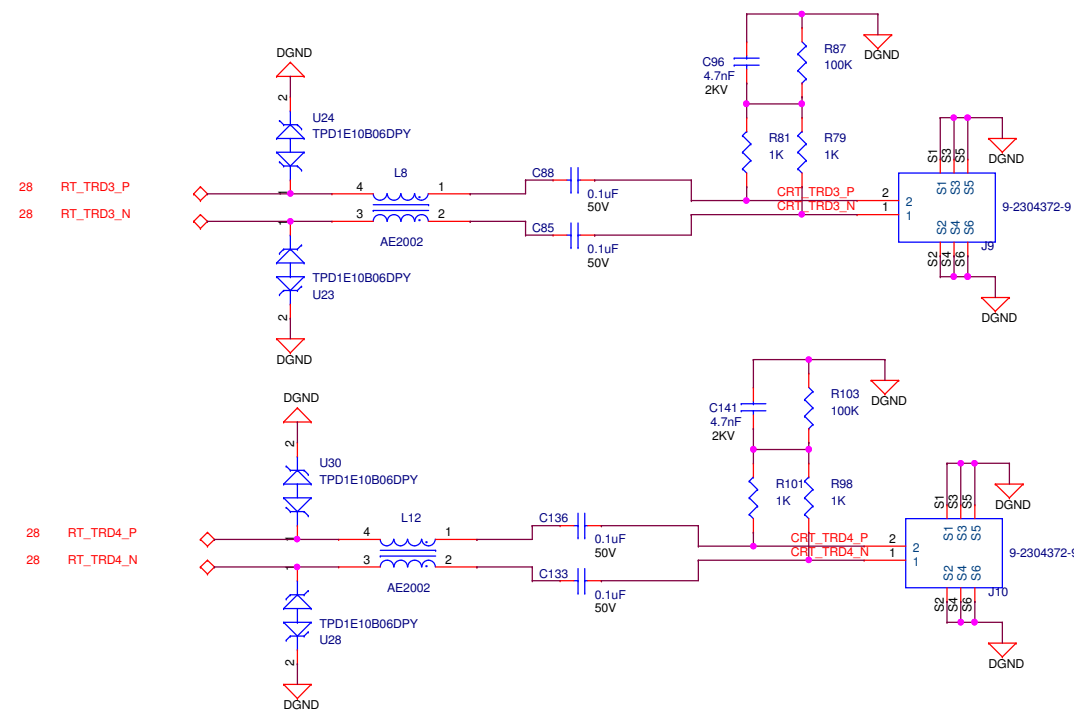
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## REALTEK 100BASE-TX 1X



## REALTEK 1000BASE-T1 x2



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SINGLE NET NODES FOR TBD FEATURES

17 SYNC\_LM5141\_DC TP38 Y17 IS PWM THAT COULD BE USED FOR CLOCK SYNC.

5 PCIE1\_PRSNT2n TP9 SINGLE LANE PCIE, SO NOT REALLY NEEDED.

VDDSHV1\_MCU GPIO

8 WKUP\_1V8\_GPIO0\_31 TP35 1.8V GPIO FROM MMC PINS  
 8 WKUP\_1V8\_GPIO0\_28 TP37

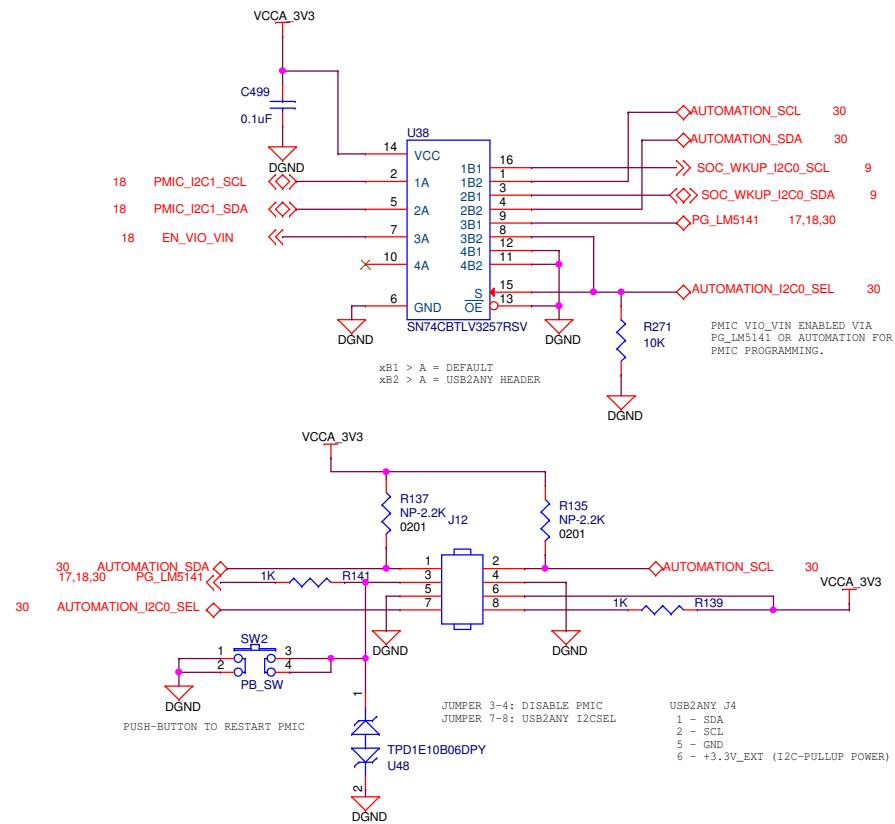
VDDSHV0 GPIO

10 GPIO0\_56 TP19 GENERAL BLOCK  
 10 GPIO0\_59 TP21

VDDSHV2 GPIO

12 GPIO0\_32 TP12 MCAN/UART BLOCK  
 12 GPIO0\_46 TP14

USB2ANY PMIC PROGRAMMING



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