*** DISCLAIMER ***

The SoC Reference Design Study provides SCH & PCB source files that can be used as a good starting point for new designs. Please be aware that the SCH & PCB are NOT 100% complete for implementing an End Product. An End Product’s feature set will define additional required signaling and SoC interfaces. As a result, a majority of signals in this SCH are "single-pin" / "unconnected" nets.

The SoC’s schematic symbol has been organized based upon each ball’s "primary signaling interface". For End Products, unused primary interface signals can then be re-defined by SoC's internal muxmode control (see Data Manual for details) to use "alternate functions" (i.e. GPIOs) to support other key system needs (i.e. interrupts, debug, etc.).

Primary objectives of this Ref Design are to demonstrate:
1. 100% signal & power breakout routing of SoC using recommended PCB design rules & strategies.
2. Key high-speed signals with controlled impedance PCB routing (i.e. DDR & SERDES).
3. Power Distribution Network (PDN) with the following:
   a) Recommended SoC power solution components (2nd stage) showing preferred SoC voltage domain to power resource mapping.
   b) Optimized decoupling capacitor scheme per key power rail using only automotive qualified caps to meet SoC recommended power integrity (PI) parameters based on this specific PCB design (stack-up, placement, routing, via types, etc).
   c) A typical 1st stage power conversion interfaced directly to input battery has been captured as an example.
REVISION HISTORY

REV A, 10/19/2020

SHEET 12, UART2 RX/TX SWAP

SHEET 19, VSYS_5V0 TO ALWAYS ON

SHEET 21, ADD R-MUX FOR McAN1/McAN2 AT US

SHEET 25, MOVE R303 IN FRONT OF R302, ADD R327 TO MMC_PWR_ON. ROUTE MMC1_SDCD(ECAP1) AND MMC_PWR_ON(ECAP2) TO J11/J18.
NOTES:
1) C2000 INTERFACE SUPPORTS BOARD TO BOARD AND BOARD TO CABLE WITH SPORTS/SPD/SPD/SFSD COMPONENTS.
2) T1 INTERFACE USES TE MATENET SINGLE PORT AUTOMOTIVE GRADE CONNECTORS.
3) CAN/LIN INTERFACE USES MOLEX MINI50 AUTOMOTIVE GRADE CONNECTORS.
4) USB INTERFACES USE MINI A/B CONNECTORS.
5) INPUT POWER IS STANDARD 2.5mm EVM STYLE.
6) 3.3V IO RETENTION ON CAN/LIN TIED TO VDDSHV2 FOR GATEWAY INTERFACE.
8) HIGH SECURITY DEVICE EFUSE PROGRAMMING NOT SUPPORTED.
9) EXTERNAL PMIC PROGRAMMING VIA USB2ANY.
10) SD CARD SUPPORT IS FIXED 3.3V.
11) SUBSET OF BOOTMODES ARE SWITCH SELECTABLE.
ON BOARD GPIO ASSIGNMENTS

<table>
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<tr>
<th>MDx</th>
<th>MAPPING</th>
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TIPS62810QWRWYRQ1 0.9@3A

DPTG720 PHY

VDD_(MCU)IO_3V3 CAN/USB HOST

VDD_GPIORET_3V3 SOC/LPDDR/OSPI/eMMC REALTEK ENET SWITCH

12V@3A NOMINAL INPUT REVERSE BATTERY FILTER WITH CUTOFF AT 4.04KHZ

LM5141-Q1 3.3V@15A

TPS62810QWRWYRQ1 1.0V@3A

TPS74501-Q1  TPS61088RHLR 5V@2A

CAN/LIN WAKEUP SUPPORTED ON GATEWAY VIA VDDSHV2@3.3V.

THE 5V CAN BOOST REGULATOR IS ENABLED WITH VDD_GPIORET_3V3 CONTROL. 5V TO THE USB POWER SWITCH IS ALSO SUPPLIED BUT DISABLED. NOT ISOLATING 5V TO USB FOR COST AND ITS OPTIONAL.
SERDES - PCIE-GEN2, SGMII, USXGMII ALL 100-OHM DIFF PAIRS.
USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS
IN GPIO RETENTION MODE NON-CAN/LIN SOC OUTPUTS SHOULD BE DRIVEN LOW. THIS PREVENTS DRIVING LOGIC HIGH INTO UNPOWERED PINS.

PRIMARY SIGNALS TO PROTECT:
- C2000*
- A72_CONSOLE_TXD
- MDIO_MDC
- MDIO0_MDC
- MDIO0_MDIO
- H_PMIC_WAKE0
- A72_CONSOLE_TXD
- A72_CONSOLE_RXD
- LIN1_UART1_TXD
- LIN1_UART1_RXD
- LIN4_UART4_RXD
- LIN4_UART4_TXD
- MCAN0_RX
- MCAN0_TX
- MCAN1_TX
- MCAN1_RX
- MCAN3_TX
- MCAN3_RX
- MCAN4_TX
- MCAN4_RX
- MCAN5_TX
- MCAN5_RX
- MCAN6_TX
- MCAN6_RX
- MCAN7_TX
- MCAN7_RX
- MCAN8_TX
- MCAN8_RX
- MCAN9_TX
- MCAN9_RX
- MCAN10_TX
- MCAN10_RX
- MCAN11_TX
- MCAN11_RX
- MCAN12_TX
- MCAN12_RX
- MCAN13_TX
- MCAN13_RX
- MCAN15_TX
- MCAN15_RX
- UART2_TXD
- UART2_RXD
- UART8_TXD
- UART8_RXD
- UART0_TXD
- UART0_RXD
- UART1_TXD
- UART1_RXD
- GPIO0_41
- GPMC0_CLK
- RMII1_TX_EN
- RMII1_RXD1
- RMII1_TXD0
- RMII1_RX_ER
- RMII1_RXD0
- RMII1_TXD1
- RMII1_CRS_DV
- PMIC_WAKE0
DIGITAL POWER 2

HIGH-SECURITY DEVICE
EFUSE PROGRAMMING NOT SUPPORTED

Note: A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Diac scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

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INPUT PROTECTION AND FILTER

Vgs 40V
Vgs = -20V
Vs ≤ 1V
Driving f = 1kHz @ 35V
Dissipation ≤ 50W
Ciss = 3730pF
Vcap(min) = 37nF

VBBAT 3.3V Nominal @ 15A max

STAGE-1 3.3V POWER

For 3.3V/5V
L = SRP1265A-2R2 - DCR=3.8-4.2mohm, Irms=22A, Isat=40A

For 5V/5V
L = SRP1265A-2R2 - DCR=3.8-4.2mohm, Irms=22A, Isat=40A

MHP125-250
M3
M6
M4
M5
M2
M1
TP40 SMT-TP
TP41 SMT-TP
TP42 SMT-TP
TP43 SMT-TP
TP2 SMT-TP
TP44 SMT-TP
TP45 SMT-TP
TP17 SMT-TP

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OPTIONAL SD CARD SUPPORT

USB PORT FOR DEBUG
CONNECTOR PINNING FROM PGCARD TO C2000 CARD SHOULD BE MIRRORED:
SEE sfsdx-xx-xxx-xx.xx-xx-xxx-mkt.pdf FOR CABLE DETAILS.

OPTIONAL CONNECTOR FOOTPRINT ON BOTTOM SIDE.
CAN/LIN POWER UP IN STANDBY/DISABLED. CAN/LIN SUPPORT IO RETENTION AND ARE WAKEUP SOURCES.
REALTEK 100BASE-TX 1X

REALTEK 1000BASE-T1 x2

C85 0.1uF 50V
C133 0.1uF 50V
R81 1K
R101 1K
U23 TPD1E10B06DPY

C88 0.1uF 50V
C136 0.1uF 50V
R79 1K
R98 1K
U28 TPD1E10B06DPY

R204 470 1%
C248 0.1uF 50V

R87 100K
R103 100K
C96 4.7nF 2KV
C141 4.7nF 2KV

L8 AE2002
L12 AE2002

J7 HR911105A

J10 9-2304372-9

S1
S2
S3
S4
S5
S6

RT_TRD3_P 28
RT_TRD3_N 28
RT_TRD4_P 28
RT_TRD4_N 28
RT_TD+ 28
RT_TD- 28
RT_RD+ 28
RT_RD- 28
RT_AN0 28
RT_AN1 28
SINGLE NET NODES FOR TBD FEATURES

V17 IS PWR THAT COULD BE USED FOR CLOCK PWR.

SINGLE LANE PCIE, SO NOT REALLY NEEDED.

1.9V GPIO FROM MMC PINS

SINGLE NET NODES FOR TBD FEATURES

USB2ANY PMIC PROGRAMMING

SW2 PB_SW

R137 NP-2.2K

R139 1K

C499 0.1uF

R141 1K

R271 10K

TP14

TP9

TP35

TP37

TP21

TP12
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