All capacitor values are shown as farads.
All inductance values are shown as henries.
All resistor values are shown as ohms.
Place these capacitors as close to their device pins as possible.

Place each capacitor on the ADIN pins as close as possible to the device.

Place each capacitor pair as close to the device pins as possible.

Place 0.1u capacitors closest to the device pins.
FOLLOWING SCHEMATIC AND LAYER PLACEMENT REVIEW WE MODIFIED THE POWER
INPUT STRUCTURES, CHANGED Y-AXIS AND Z-AXIS FILTERS SO THAT THEY EQUAL THE
X-AXIS FILTERS. THE ITEMS IN REV-H, REV-J, AND REV-K WERE APPROVED.

BOARD WAS RELEASED TO LAYOUT. LAYOUT REVIEW WILL BE HELD WHEN
PLACEMENT IS FINALIZED.

MODIFIED SCHEMATIC TO REFLECT THE ERRORS NOTED DURING LAYOUT
1) SB27 HAS AN OPEN PIN
2) SB7 AND SB8 ARE CONNECTED TO THE SAME NET. SB8 WAS MOVED TO CORRECT NET
3) BOARD GREW 0.4 INCH LONGER AND NEEDED TWO MORE MOUNTING HOLES
4) ADDED C535 AND C536 TO ARM7 SO THAT EACH SIDE OF THE DEVICE HAS A
DECOUPLING CAP ON BOTH POWER NETS

ADDED FOOTPRINT TO JP2

THE REFHI NET WAS BROKEN, IT WAS CONNECTED AT R84.

SOME COMPONENT VALUES WERE UPDATED PER THE NEW DESIGN RULES FROM TI.
SOME PART NUMBERS AND/OR FOOTPRINTS WERE UPDATED TO BRING BOM IN STEP
WITH THE OLD BOM>

REVIEW WITH HECTOR TORRES. SCHEMATIC EDITED BASED ON HECTORS FEEDBACK.
A/D CONNECTIONS TO 0G NET, VCOM AND VREF NETS WERE MODIFIED
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