

ECR	ECR NUMBER	DATE
	-----	xx/xx/xx

NOTES:

1. PLACE NET NAMES ON ALL JUMPERS AND HEADERS.
2. PLACE ALL PARTS OTHER THAN SMP CONNECTORS ON A 0 OR 90 DEGREE ORIENTATION.
3. SERIAL DATA SHOULD BE ROUTED AS SINGLE-ENDED 50 OHM TRANSMISSION LINES ON OUTSIDE LAYERS. ROUTING DISTANCE SHOULD BE 3 INCHES OR LESS.
4. USE ROGERS MATERIAL FOR OUTSIDE LAYERS AND FR4-370 MATERIAL FOR INSIDE LAYERS.
5. SERIAL AND REFCLK NETS MUST MATCH WITHIN +/- 0.5 MILS
6. MATCH DIFFERENTIAL TRACE WIDTHS OF SERIAL AND REFCLK LINES WITH SMP/SMA PADS.

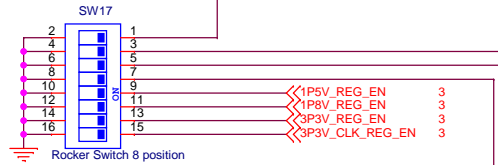
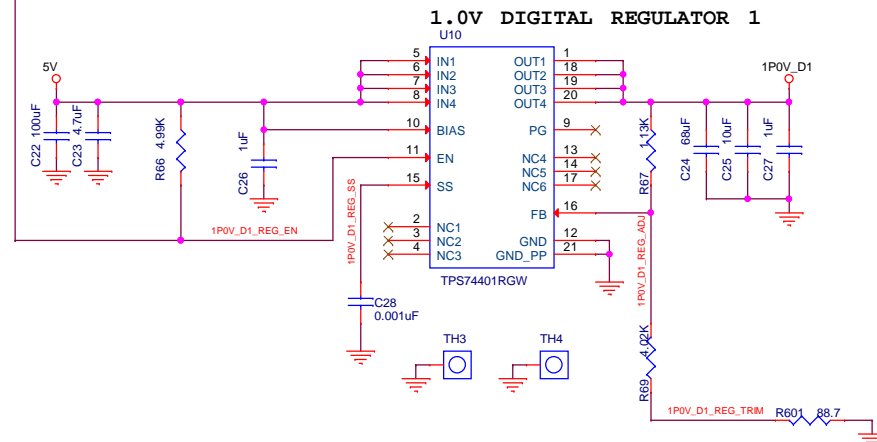
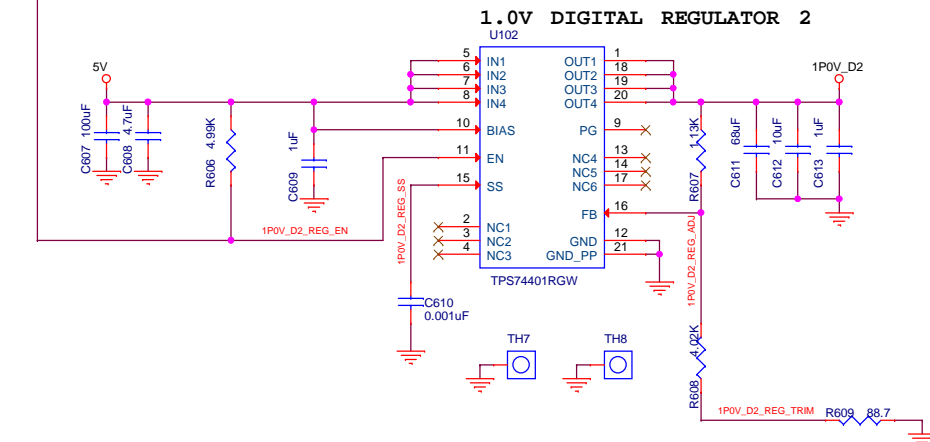
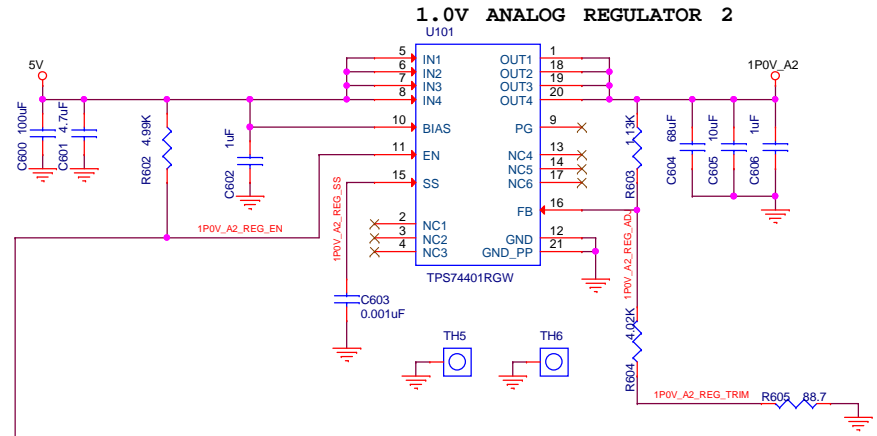
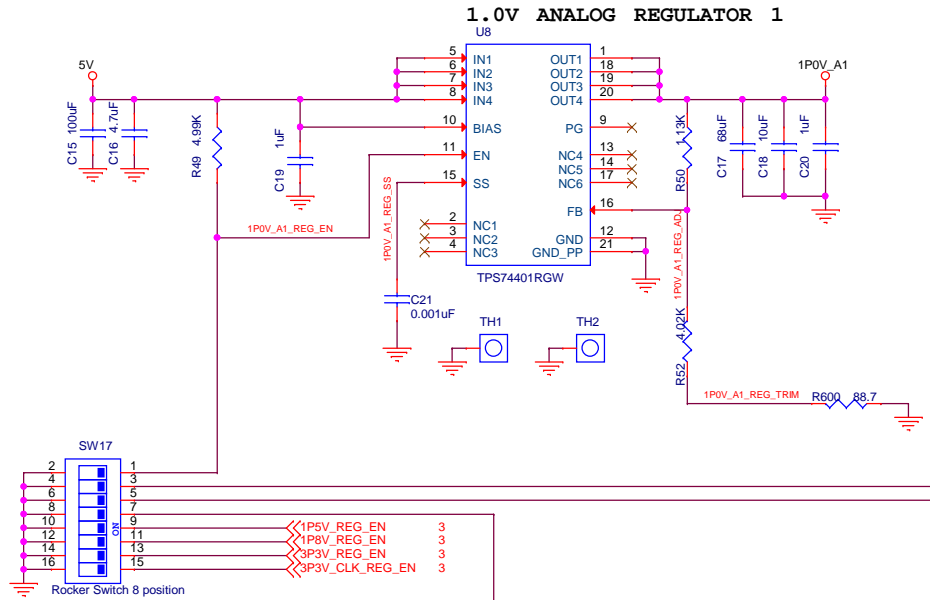
SCHEMATIC SHEET INDEX:	
SHEET 01:	TLK10081 COVER SHEET AND NOTES
SHEET 02:	1P0V REGULATORS
SHEET 03:	1P5V, 1P8V, 2P5V, 3P3V REGULATORS
SHEET 04:	POWER DISTRIBUTION
SHEET 05:	VOLTAGE MONITORING
SHEET 06:	DEVICE POWER AND GROUND
SHEET 07:	GLOBAL SIGNALS
SHEET 08:	MDIO, JTAG, AND I2C INTERFACE
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SHEET 10:	CLOCK CONTROL
SHEET 11:	CRYSTAL OSCILLATORS
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SHEET 14:	DATA BOARD TO BOARD CONNECTOR
SHEET 15:	CLOCK BOARD TO BOARD CONNECTOR



TEXAS INSTRUMENTS	
SCHEMATIC TITLE TIDA-00269 TLK10081 REFERENCE DESIGN	
PAGE TITLE COVER PAGE AND NOTES	

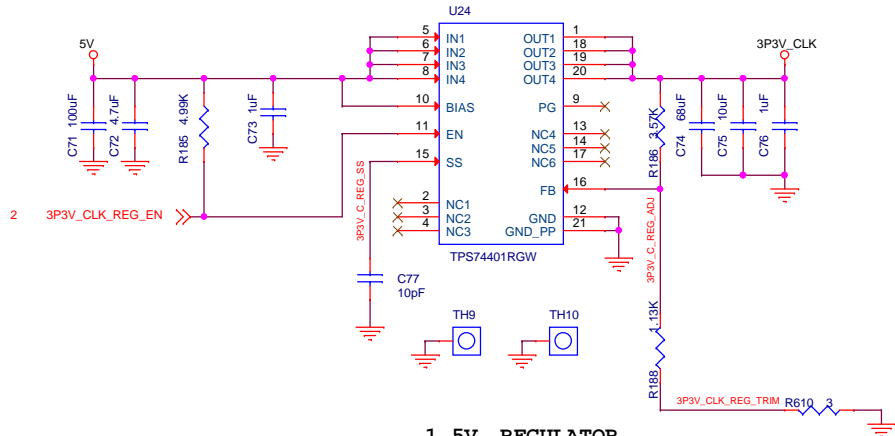
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J. NERGER	05/23/13
LAYOUT	DATE
DFW TEST	05/23/13
RELEASED	DATE
J. NERGER	05/23/13

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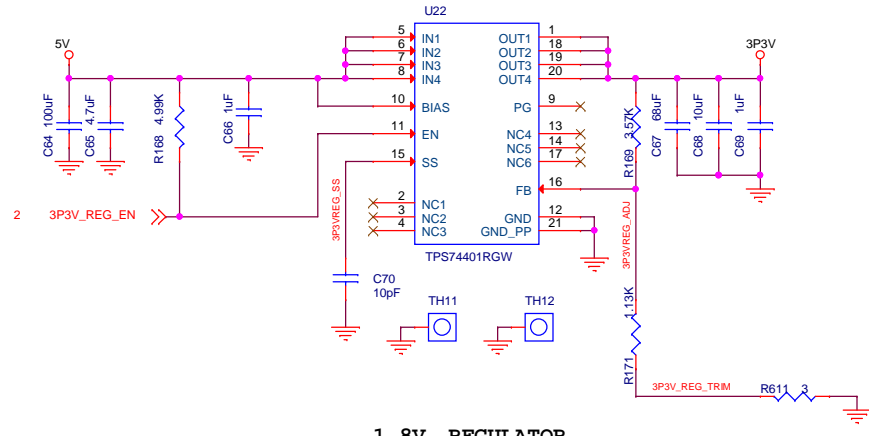


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1P0V REGULATORS TIDA-00269			
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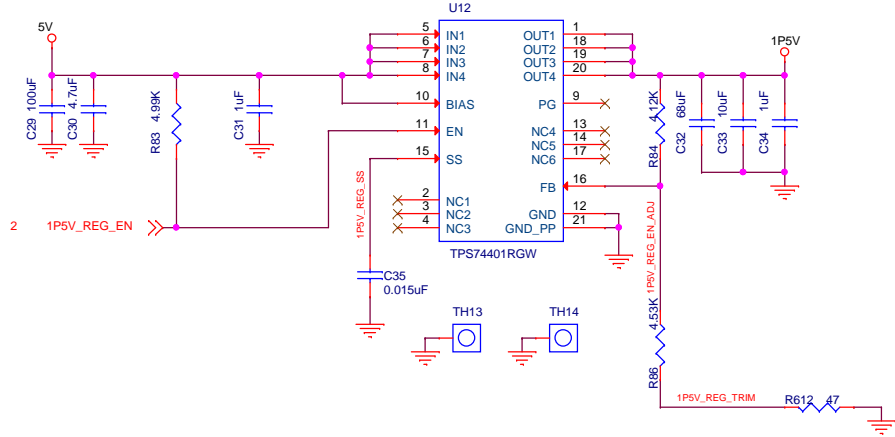
3.3V CLK REGULATOR



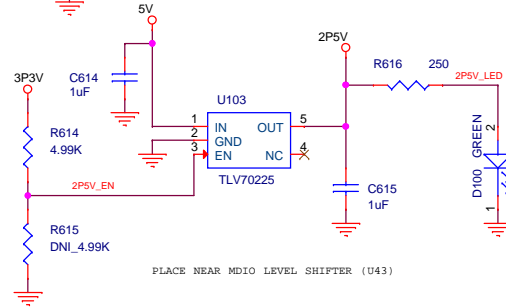
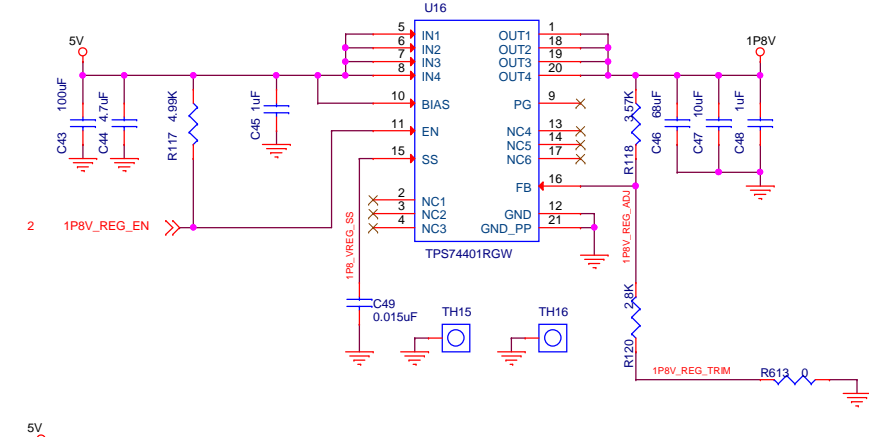
3.3V REGULATOR



1.5V REGULATOR



1.8V REGULATOR

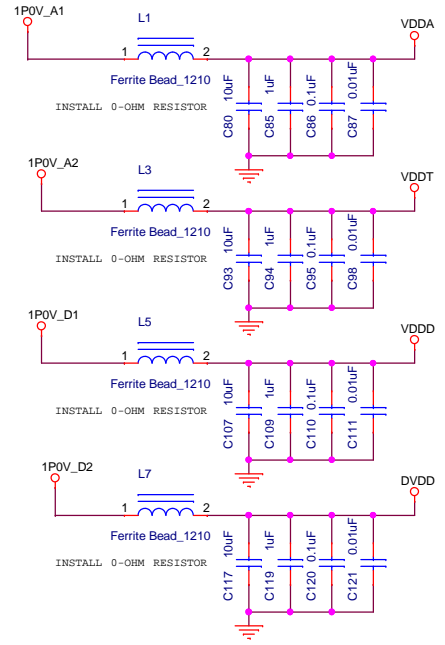
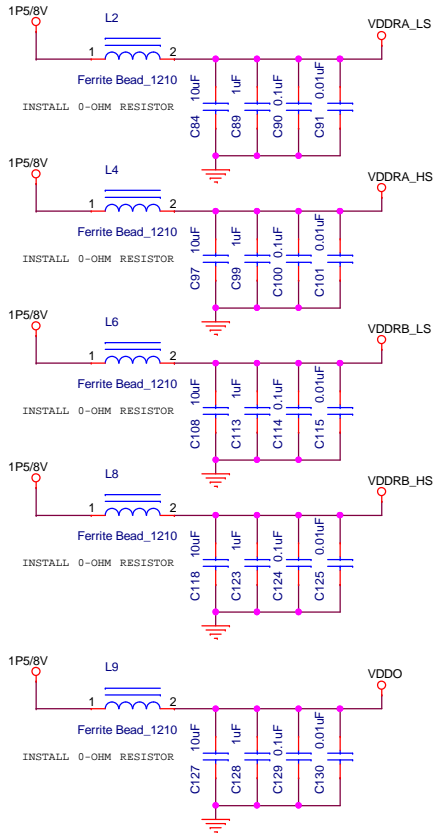
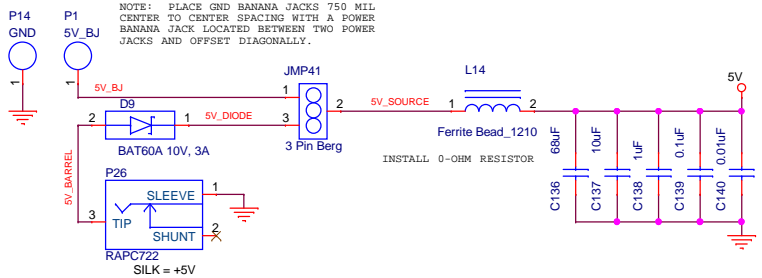
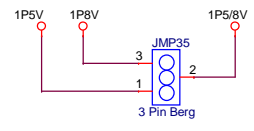
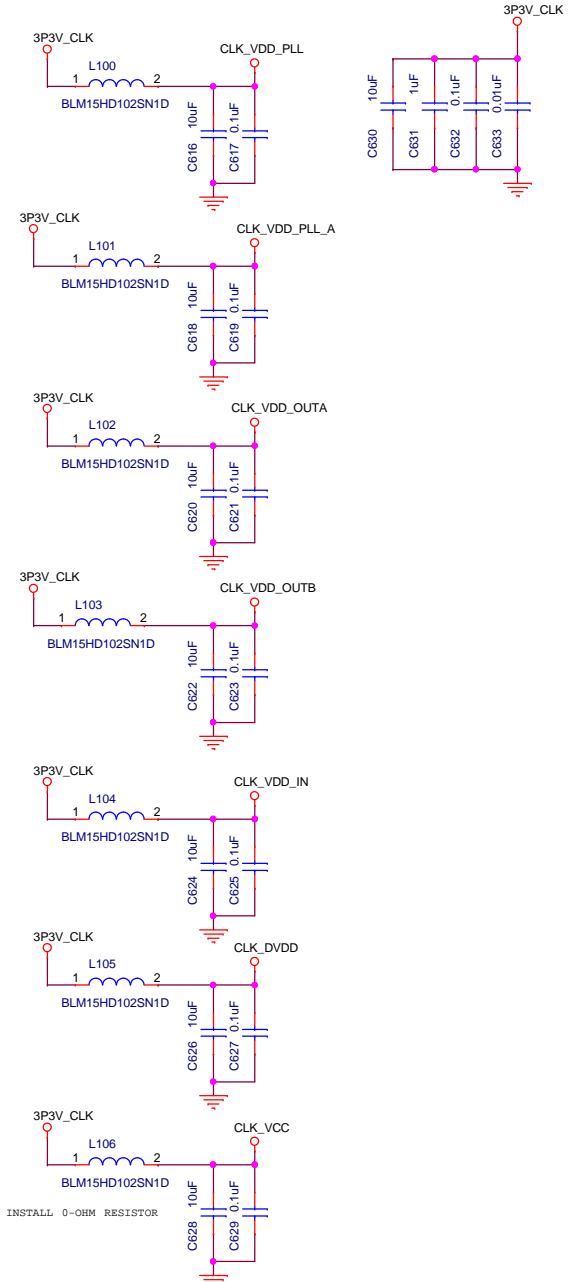


PLACE NEAR MDIO LEVEL SHIFTER (U43)

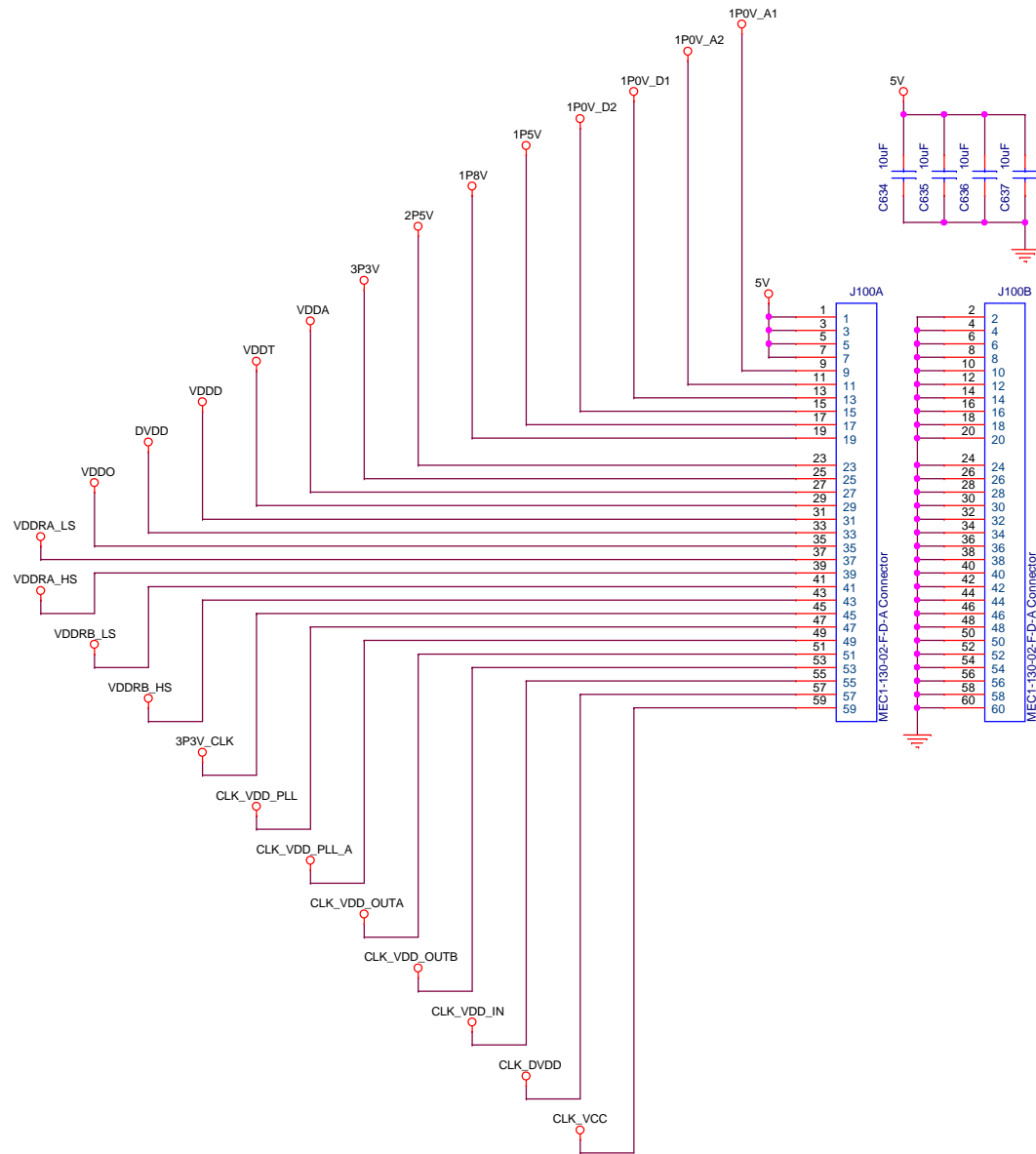


PAGE TITLE			
1P5V, 1P8V, 2P5V, 3P3V REGULATORS TODA-00269			
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PLANE FILTERING / BULK DECOUPLING




NOTE:



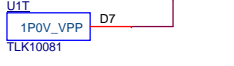
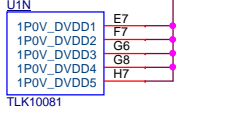
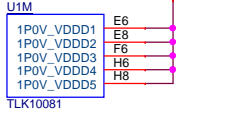
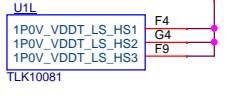
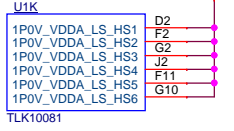
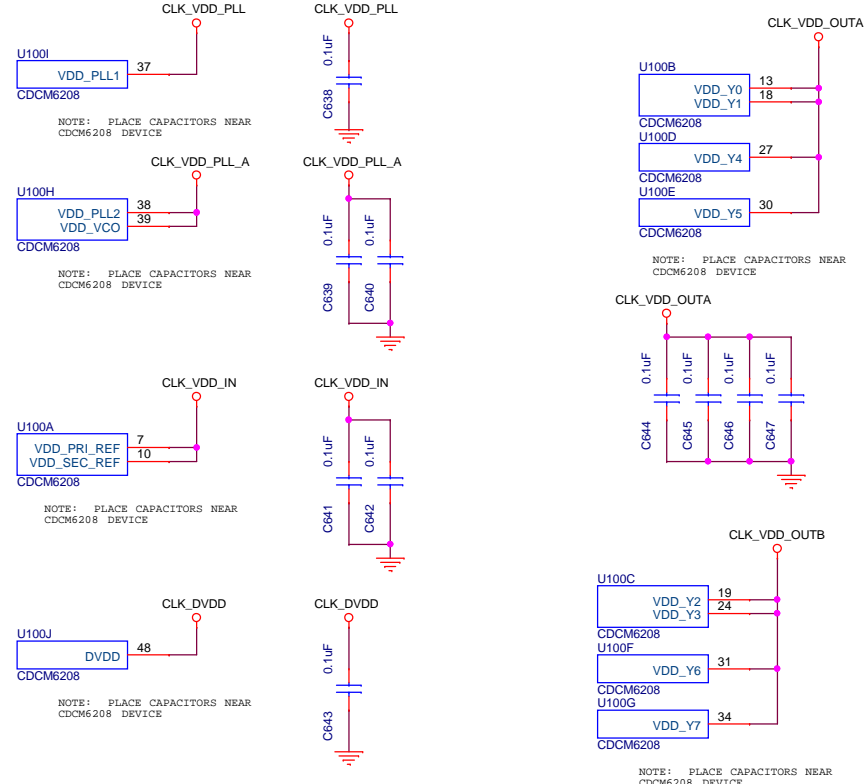
NOTE:
PLACE DECOUPLING CAPS NEAR J100 CONNECTOR



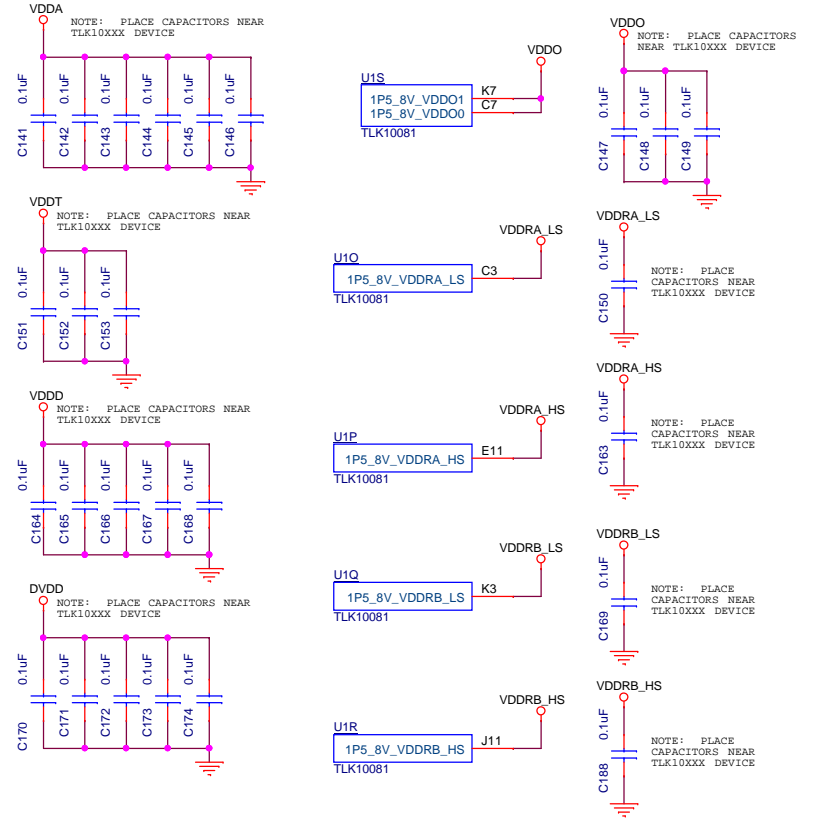
 TEXAS INSTRUMENTS				
PAGE TITLE VOLTAGE MONITORING TIDA-00629				
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NOTES:
 DECOUPLING GENERAL GUIDELINES:
 1. PLACE CAPACITORS SUCH THAT SMALLER VALUE CAPACITORS ARE NEARER THE DUT AND THEN SUCCESSIVELY PLACE LARGER VALUE CAPACITORS AS YOU MOVE AWAY FROM THE DUT.
 2. PLACE CAPACITORS NEAR VIAS AND CONNECTORS. THESE CAPACITORS SHOULD DECOUPLE THE DRIVER SUPPLY TO THE GROUND PLANE. IF A SIGNAL IS REFERENCED TO A POWER PLANE AND THIS POWER PLANE IS NOT ASSOCIATED WITH THE DRIVER SUPPLY, THEN THIS PLANE SHOULD ALSO BE DECOUPLED TO GROUND NEAR ALL ASSOCIATED VIAS AND CONNECTORS.

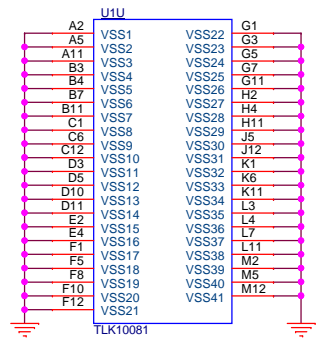
CDCM6208 DEVICE POWER / LOCAL DECOUPLING

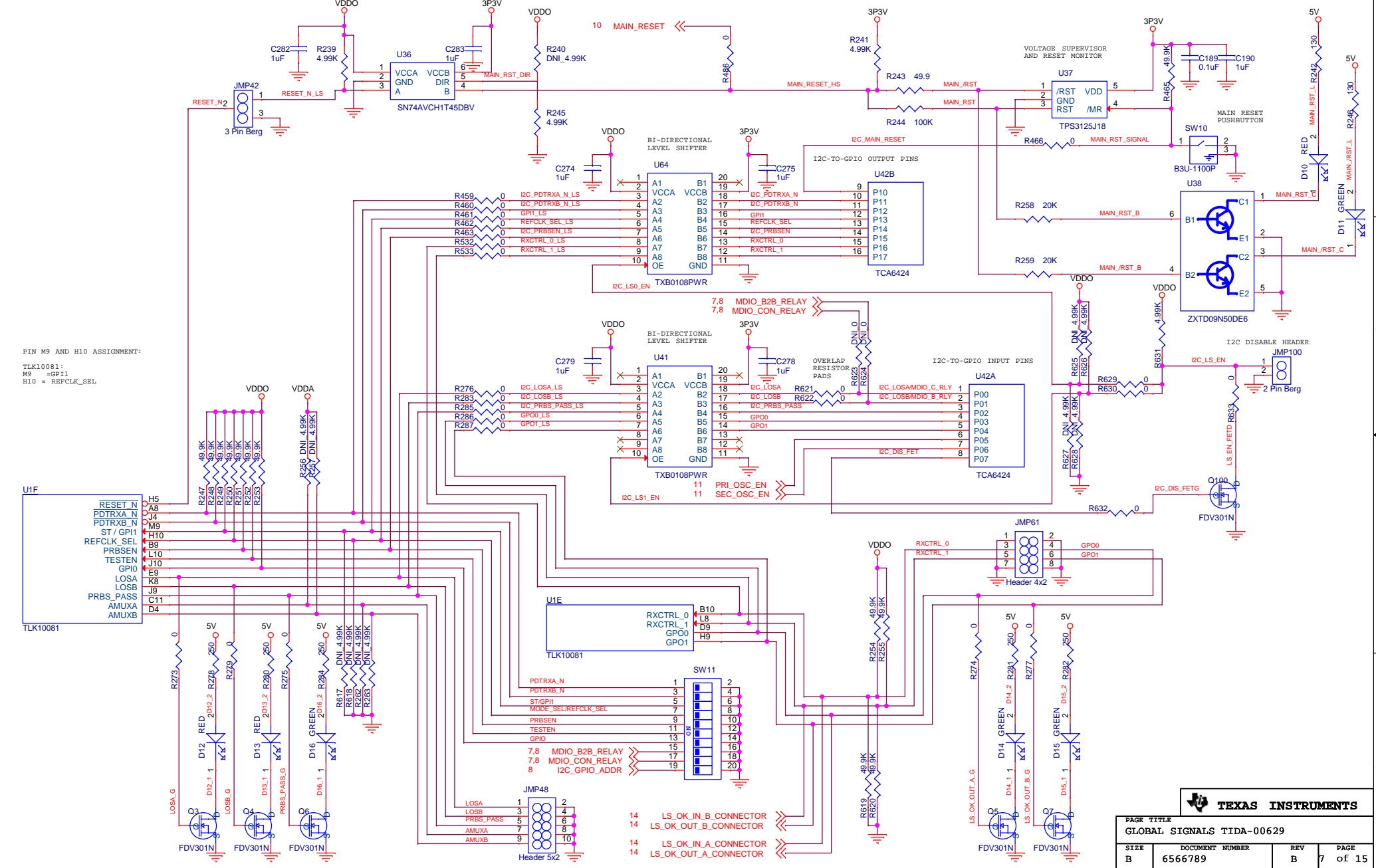


TLK10081 DEVICE POWER / LOCAL DECOUPLING



TLK10081 DEVICE GROUND





PIN M9 AND H10 ASSIGNMENT:
 TLK10081:
 M9 = GP11
 H10 = REFCLK_SEL

U1F
 RESET_N
 PDTRXA_N
 PDTRXB_N
 ST/GPH
 REFCLK_SEL
 PRBSEN
 TESTEN
 GPIO
 LOSA
 LOSB
 PRBS_PASS
 AMUXA
 AMUXB

TLK10081

U1D
 LOSA
 LOSB
 PRBS_PASS
 AMUXA
 AMUXB

FDV301N

FDV301N

FDV301N

FDV301N

FDV301N

FDV301N

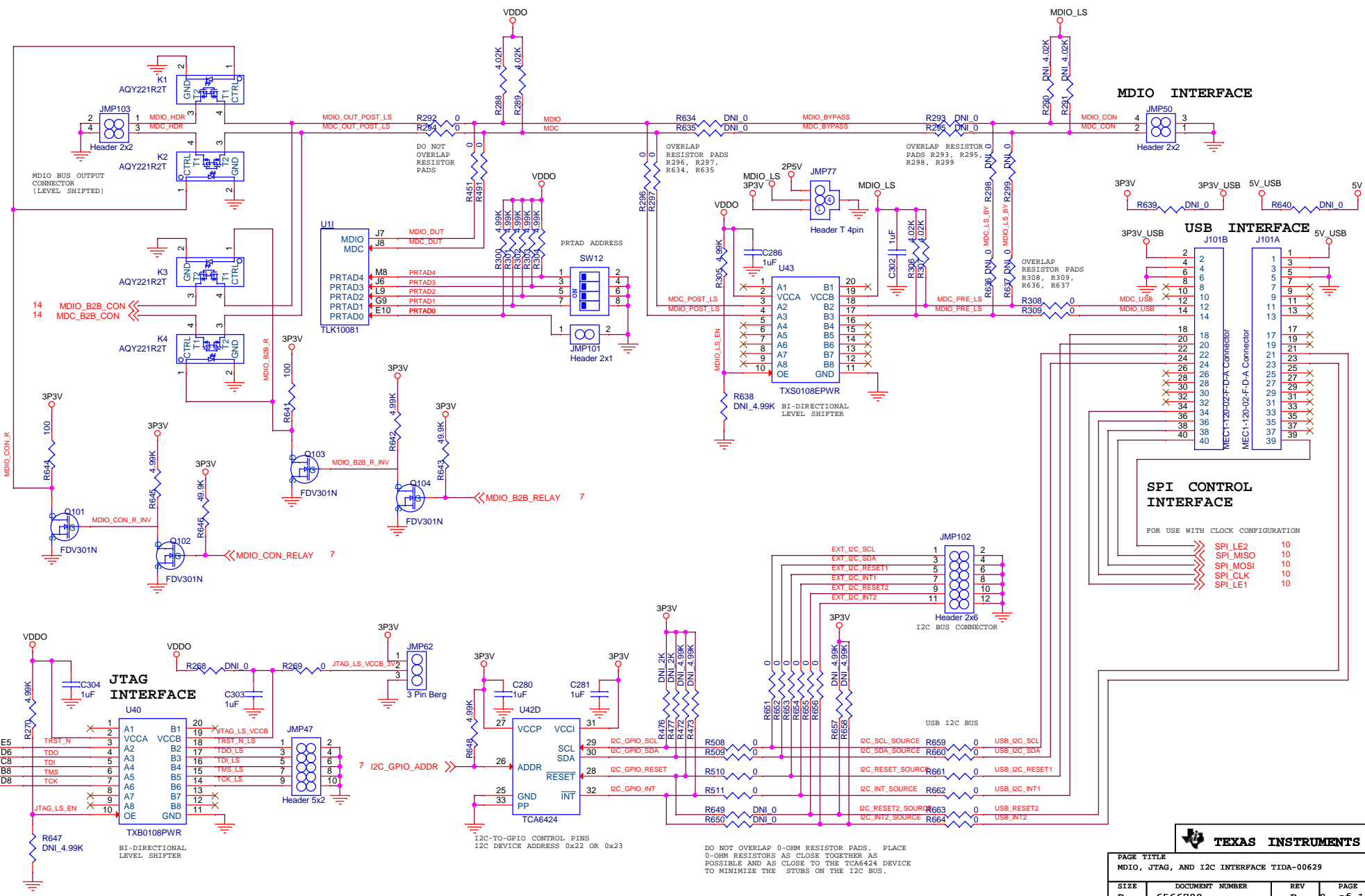
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GLOBAL SIGNALS TIDA-00629

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MDIO INTERFACE

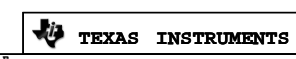
USB INTERFACE

SPI CONTROL INTERFACE

- FOR USE WITH CLOCK CONFIGURATION
- SPI_LE2 10
 - SPI_MISO 10
 - SPI_MOSI 10
 - SPI_CLK 10
 - SPI_LE1 10

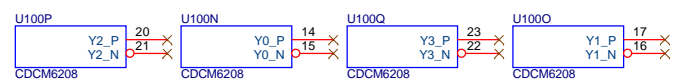
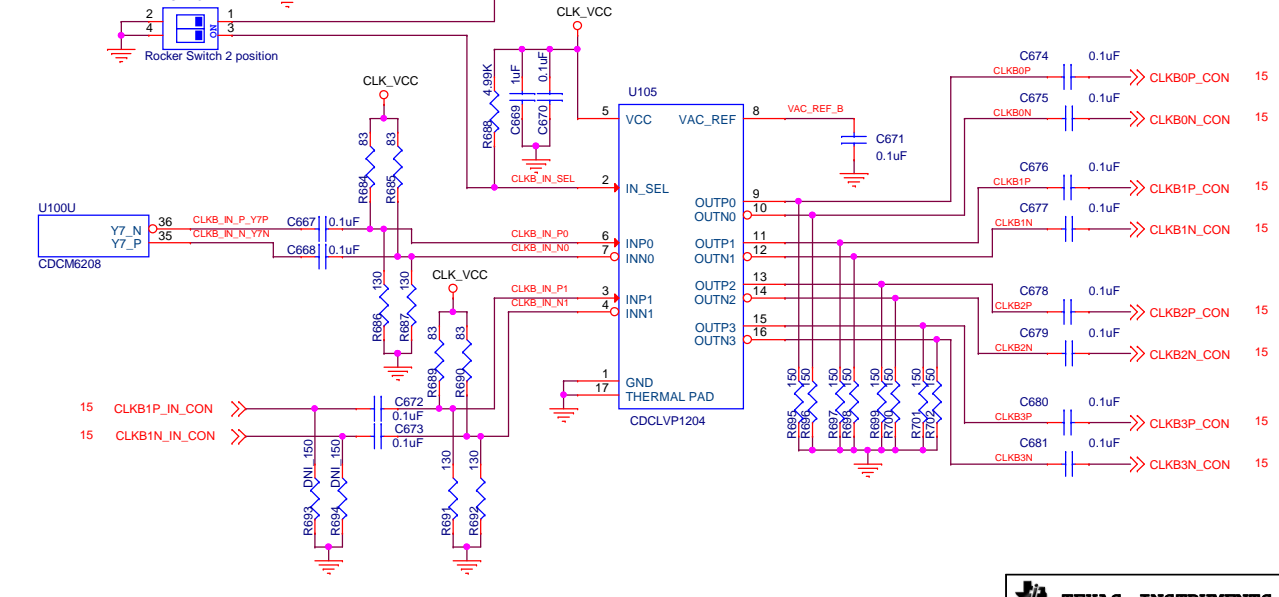
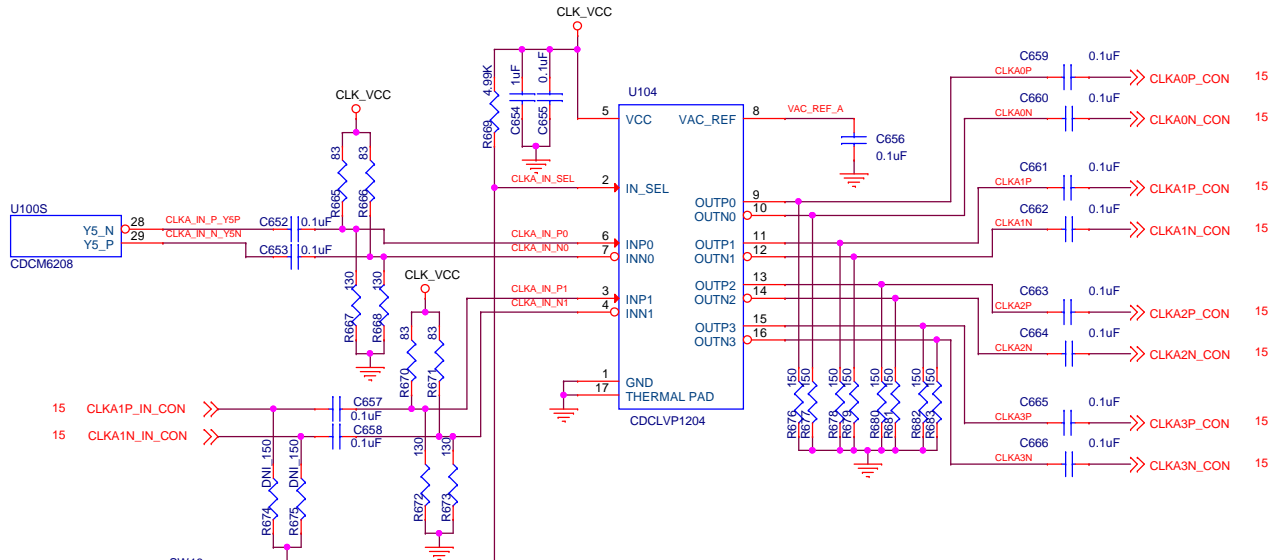
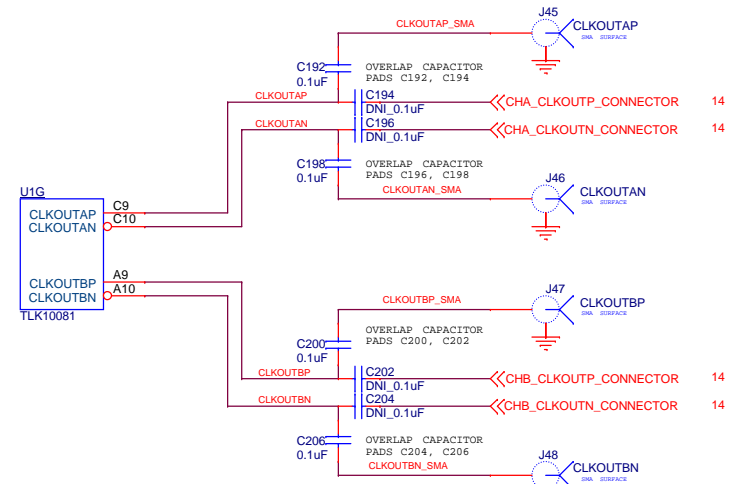
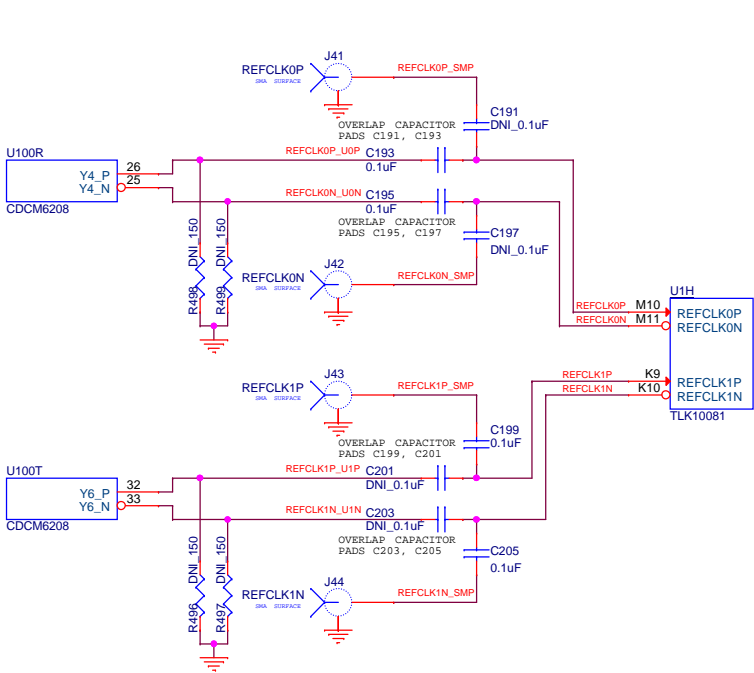
JTAG INTERFACE

DO NOT OVERLAP 0-OHM RESISTOR PADS. PLACE 0-OHM RESISTORS AS CLOSE TOGETHER AS POSSIBLE AND AS CLOSE TO THE TCA6424 DEVICE TO MINIMIZE THE STUBS ON THE I2C BUS.

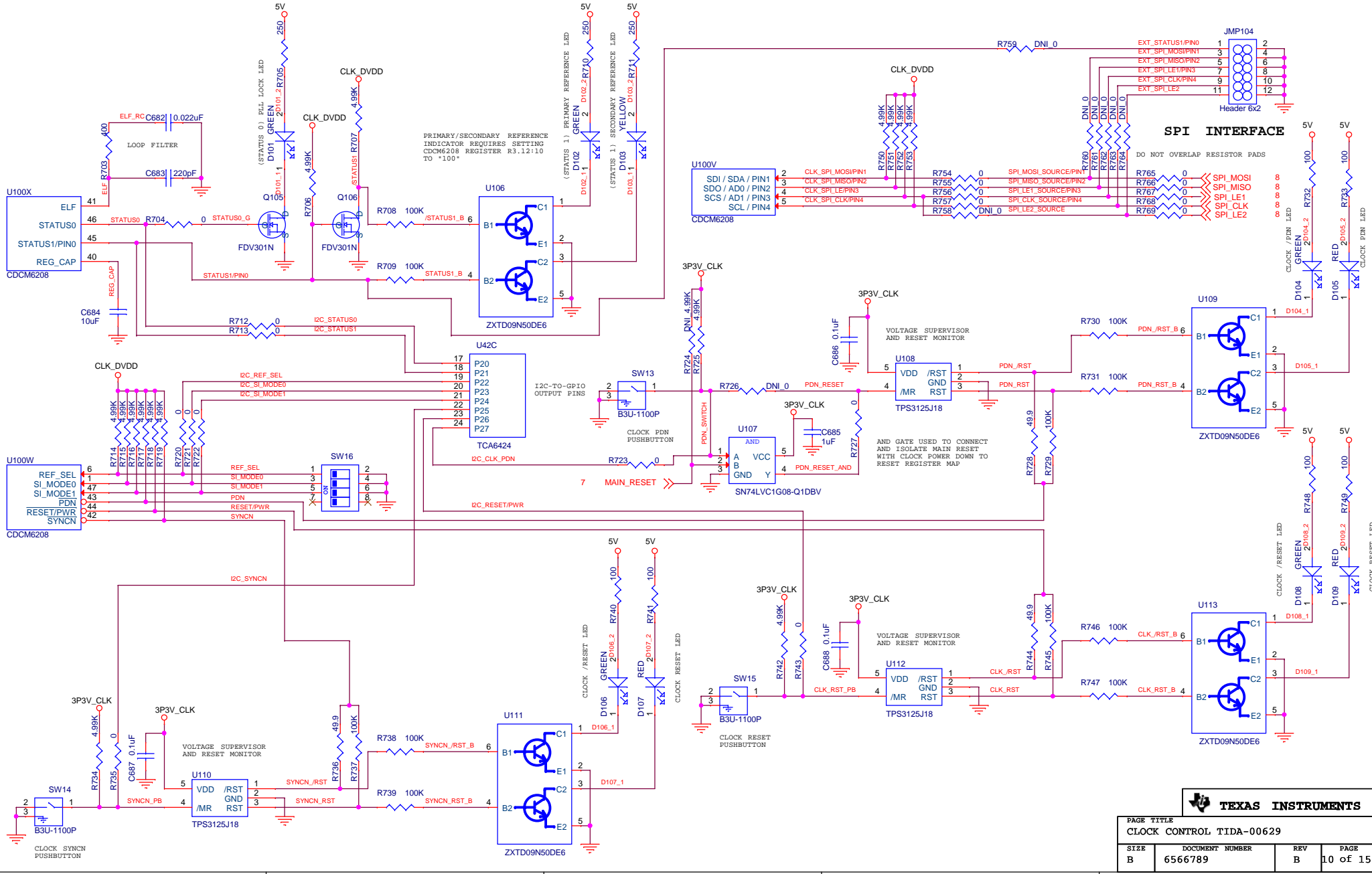


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MDIO, JTAG, AND I2C INTERFACE TIDA-00629			
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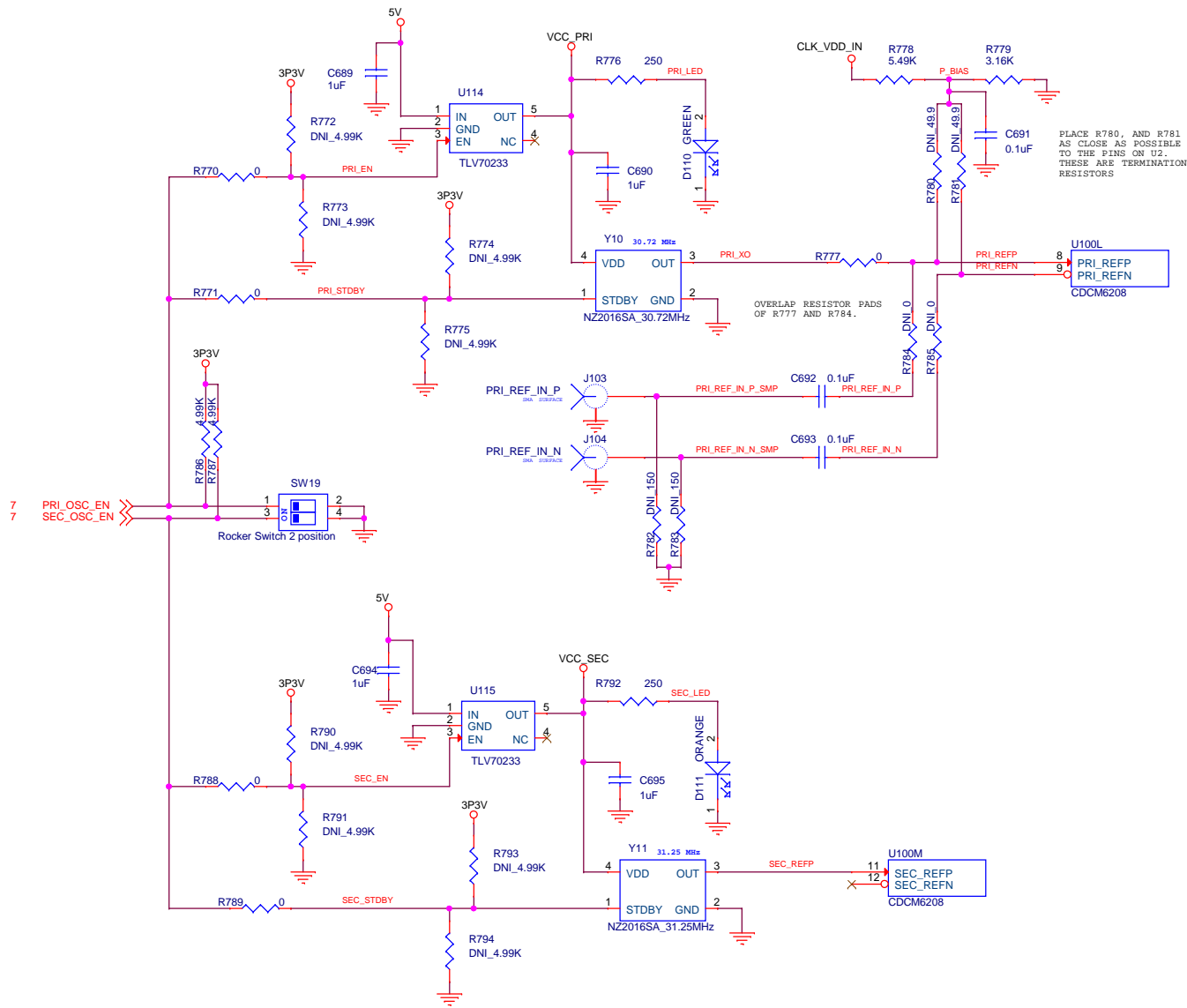
NOTE: 1. MATCH REFCLK0/1_P/N AND CLKOUT0/1_P/N TRACE LENGTHS TO EACHOTHER



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CLOCKS TIDA-00629			
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NOTE:



PLACE R780, AND R781
AS CLOSE AS POSSIBLE
TO THE PINS ON U2.
THESE ARE TERMINATION
RESISTORS

OVERLAP RESISTOR PADS
OF R777 AND R784.



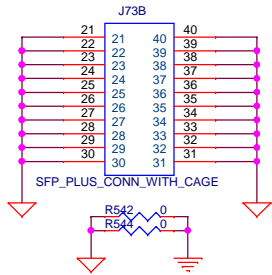
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CRYSTAL OSCILLATORS TIDA-00629			
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5 4 3 2 1

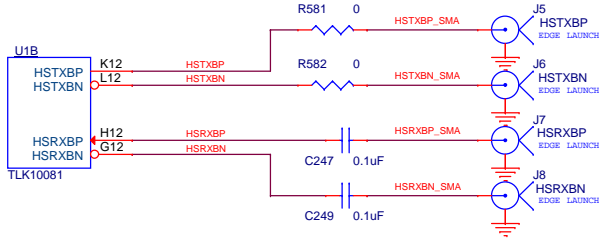
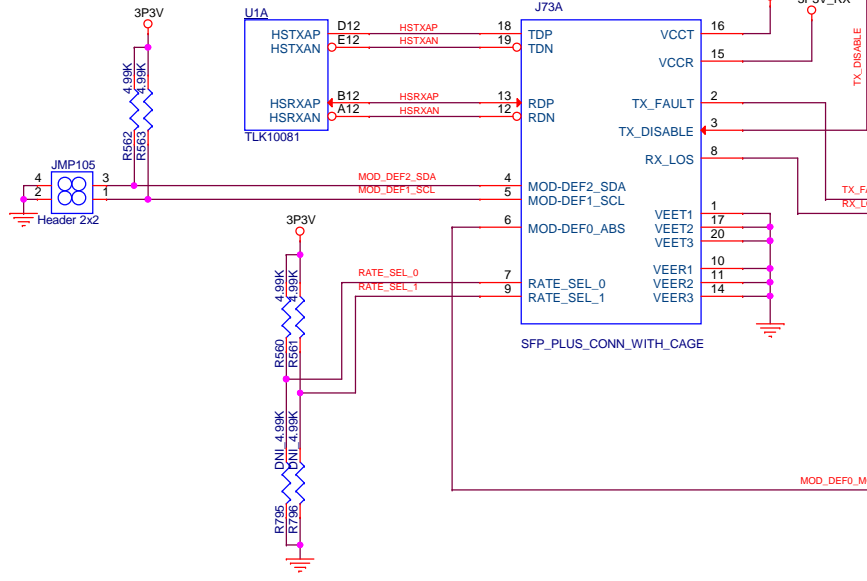
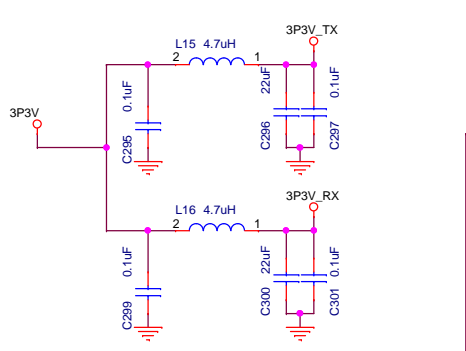
NOTE:
 1. MATCH LOW SPEED INPUT AND OUTPUT TRACE LENGTHS TO EACHOTHER
 2. MATCH HIGH SPEED TRANSMIT AND RECEIVE TRACE LENGTHS TO EACHOTHER



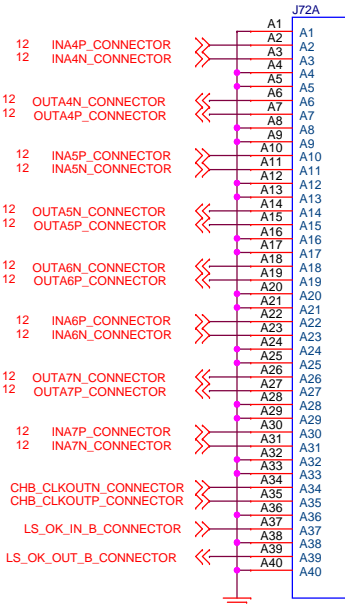
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LOW SPEED DATA SIGNALS TIDA-00629			
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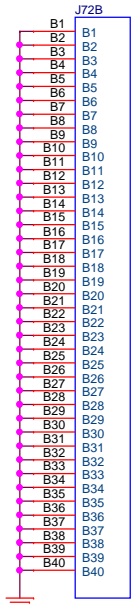
RESISTORS ARE USED TO PROVIDE COMMON PATH TO GROUND. PLACE ONE ON EACH SIDE OF OPTICAL MODULE CAGE NEAR THE MIDDLE OF THE MODULE.



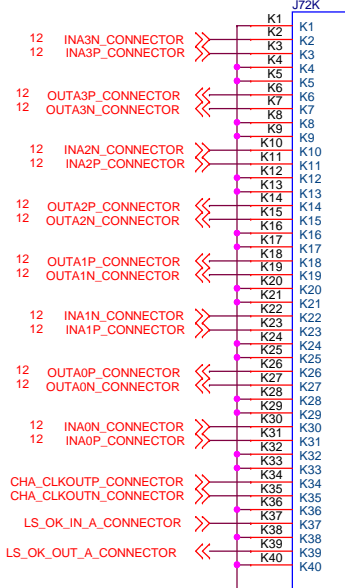
THE HIGH SPEED TX LINES SHOULD BE AC COUPLED IN THE SYSTEM WITH 0.1uF CAPACITORS FOR PROPER OPERATION. ZERO OHM RESISTORS ARE INSTALLED ON THIS BOARD TO ALLOW FOR EXTERNAL LOOPBACK BETWEEN THE HSTXB AND HSRXB UTILIZING THE AC CAPACITORS ON THE HSRXB PINS. THE ZERO OHM RESISTORS CAN BE REPLACED WITH 0.1uF CAPACITORS IF AC COUPLING CAPACITORS ARE NEEDED ON THESE SIGNALS.



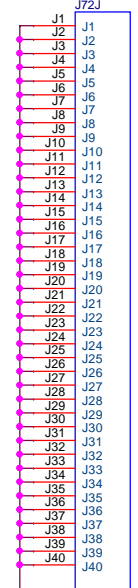
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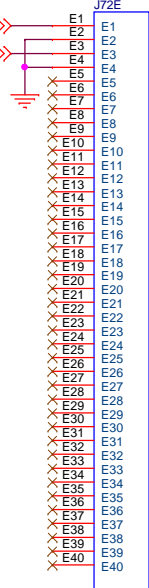


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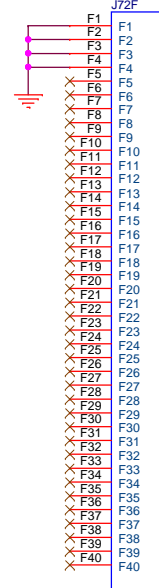


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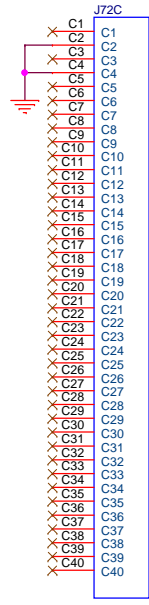
8 MDIO_B2B_CON
8 MDC_B2B_CON



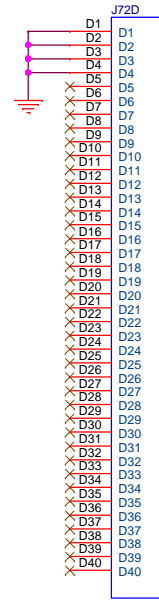
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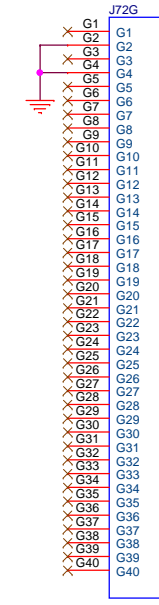
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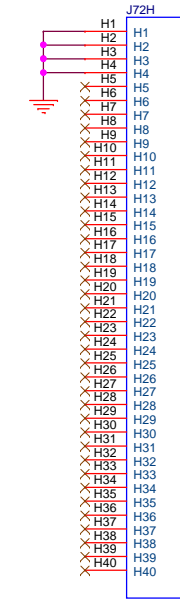
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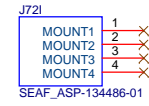
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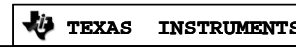
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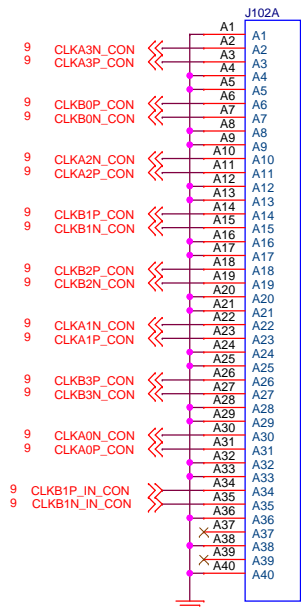
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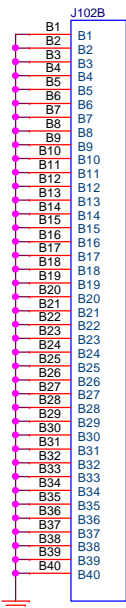
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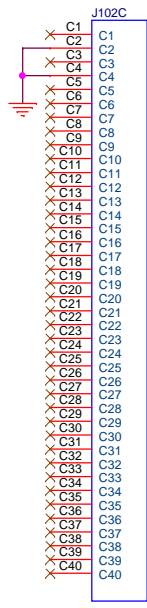
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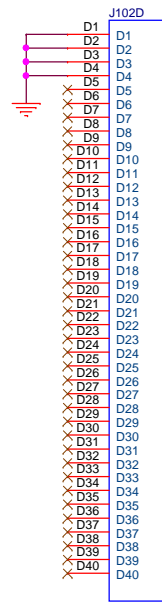
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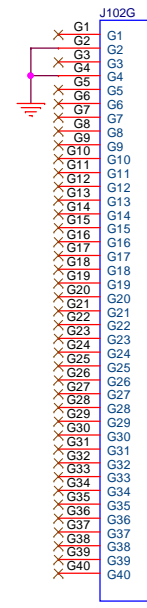
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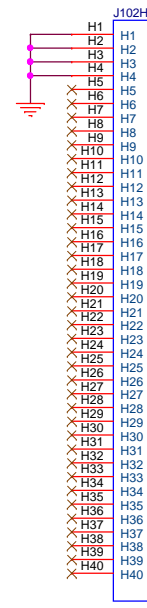
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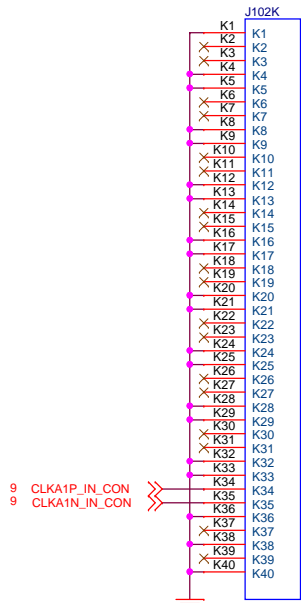
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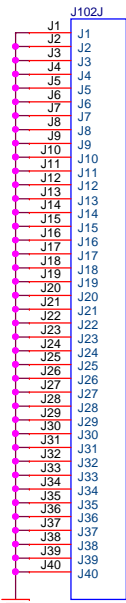
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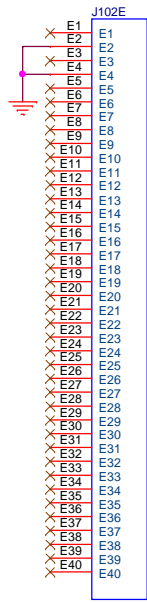
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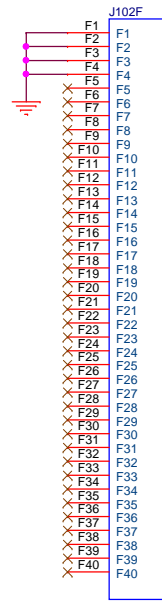
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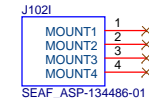
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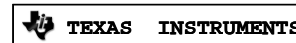
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SEAF_ASP-134486-01



PAGE TITLE
CLOCK BOARD TO BOARD CONNECTOR TIDA-00629

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