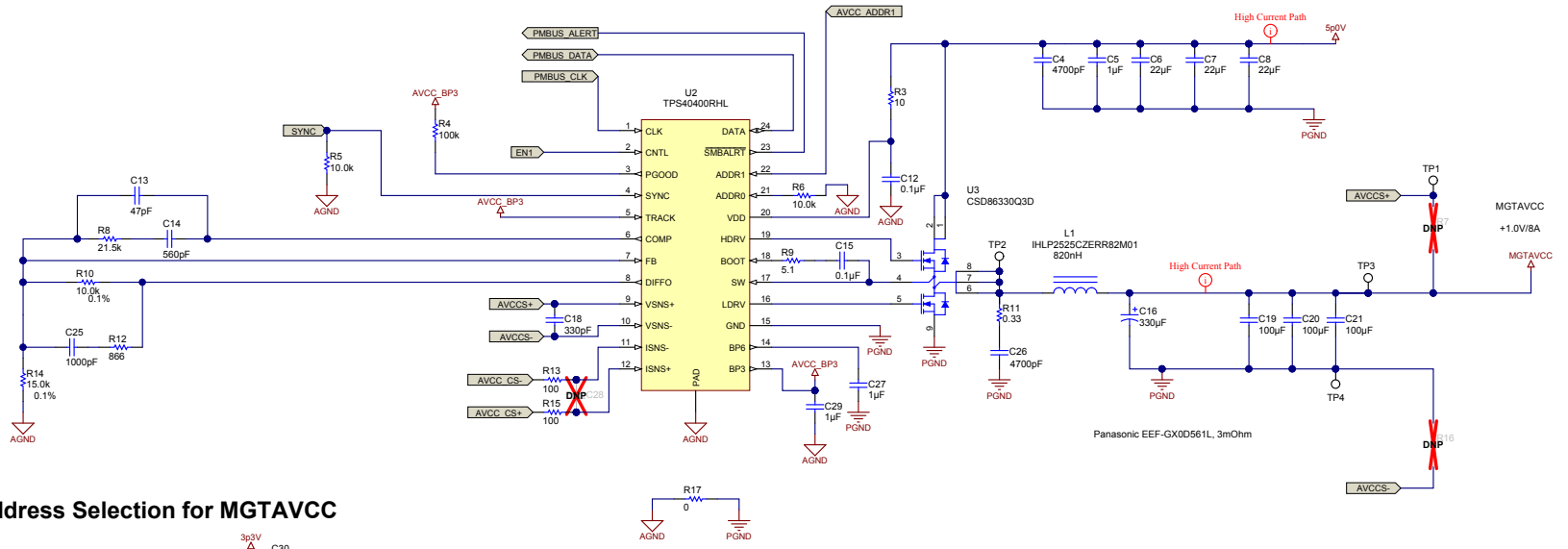
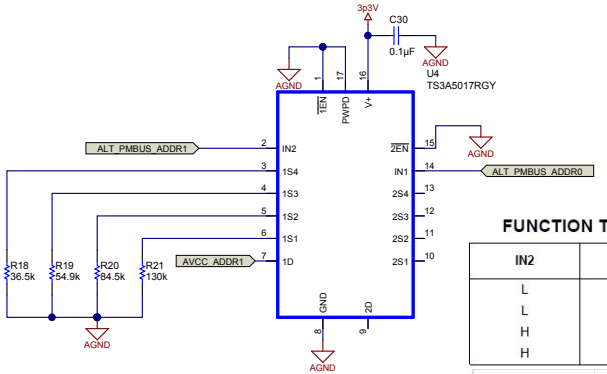
MGTAVCC - 1.0V@8A



Single connection between AGND and PGND

PMBUS Address Selection for MGTAVCC

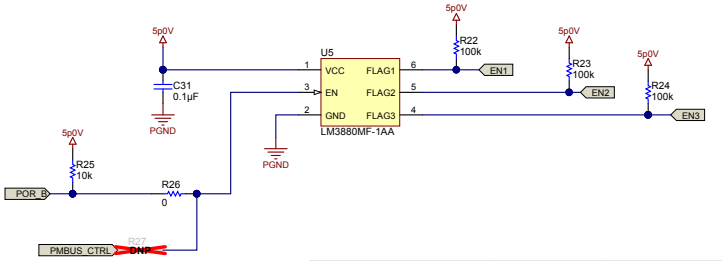


FUNCTION TABLE

IN2	IN1	D TO S, S TO D
L	L	D = S_1
L	H	D = S_2
H	L	D = S_3
H	H	D = S_4

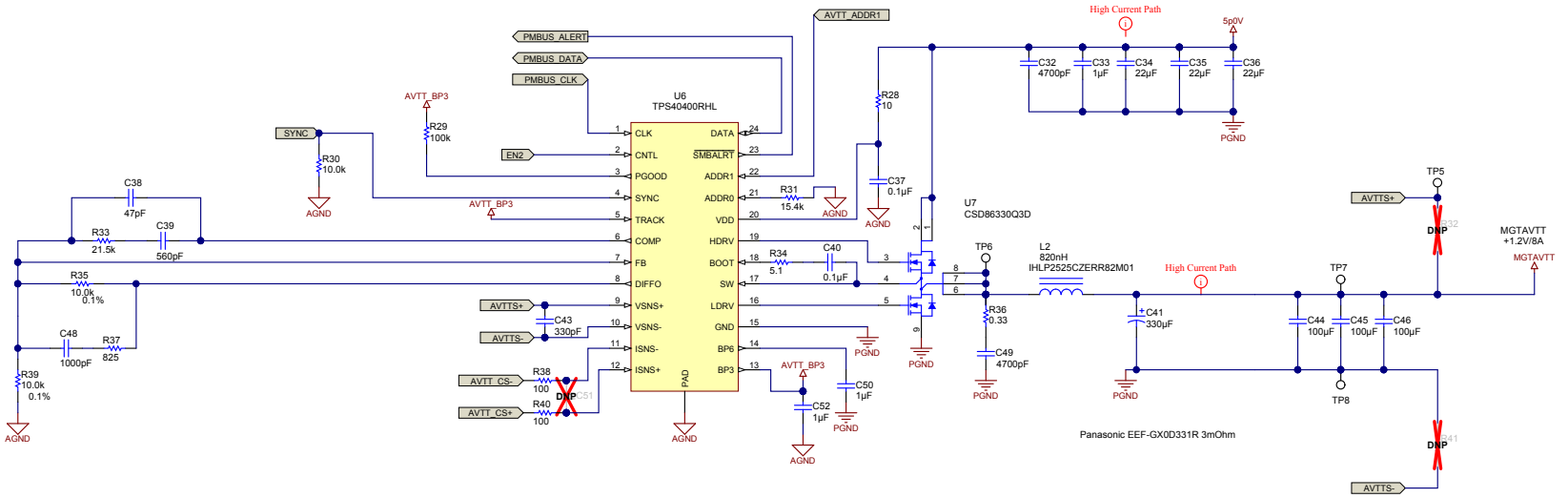
AVCC Rail 1					
ALT_PMBUS_1	ALT_PMBUS_0	HEX	OCTAL	Raddr1 (kohm)	Raddr0 (kohm)
GND	GND	0x30	60	130	10
GND	OPEN	0x28	50	84.5	10
OPEN	GND	0x20	40	54.9	10
OPEN	OPEN	0x18	30	36.5	10

Sequencer

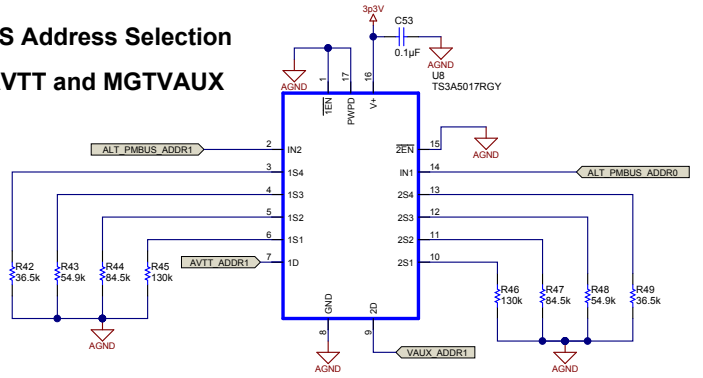


Designed for: Public Release		Mod. Date: 6/27/2014	
Project Title: PMP9463 Xilinx Ultrascale Kintex MGT			
Number: PMP9463	Rev: E1	Sheet Title: MGTAVCC	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 6
Drawn By: Sami Sirhan		File: Page1.SchDoc	Size: B
Engineer: Sami Sirhan		Contact: http://www.ti.com/support	http://www.ti.com

MGTAVTT - 1.2V@8A



PMBUS Address Selection for MGTAVTT and MGTVAUX



Provides address selection for MGTAVTT rail

Provides address selection for MGTVCCAUX rail

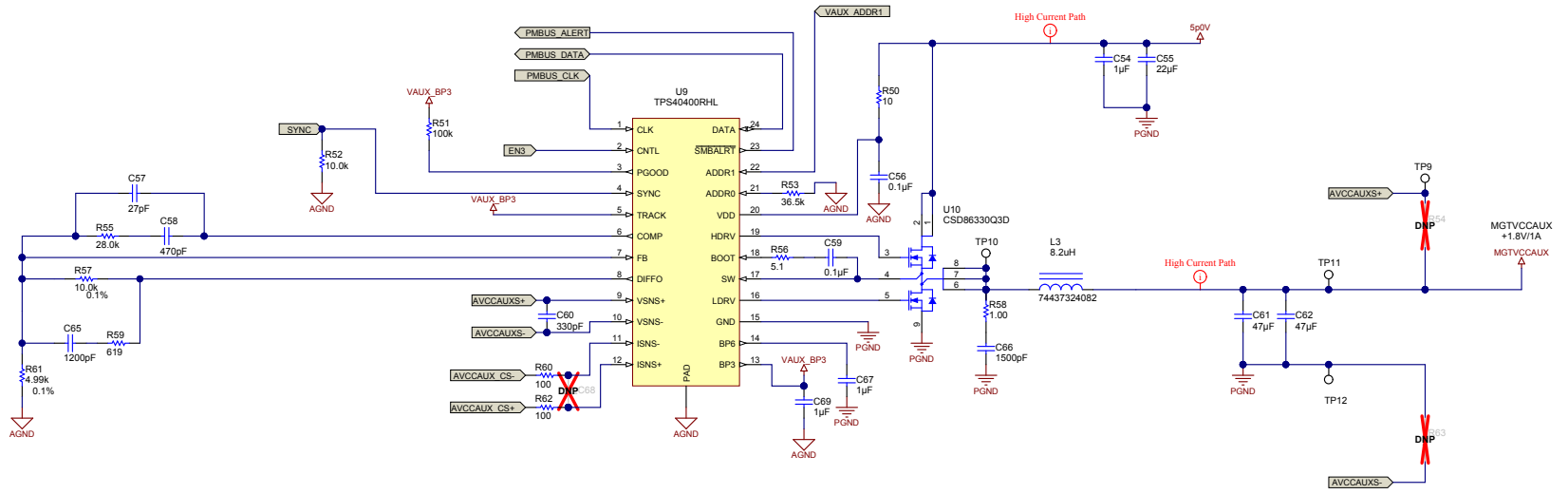
FUNCTION TABLE

IN2	IN1	D TO S, S TO D
L	L	D = S_1
L	H	D = S_2
H	L	D = S_3
H	H	D = S_4

AVTT Rail 2					
ALT_PMBUS_1	ALT_PMBUS_0	HEX	OCTAL	Raddr1 (kohm)	Raddr0 (kohm)
GND	GND	0x31	61	130	15.4
GND	OPEN	0x29	51	84.5	15.4
OPEN	GND	0x21	41	54.9	15.4
OPEN	OPEN	0x19	31	36.5	15.4

Designed for: Public Release		Mod. Date: 6/27/2014	
Project Title: PMP9463 Xilinx Ultrascale Kintex MGT			
Number: PMP9463	Rev: E1	Sheet Title: MGTAVTT	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 3 of 6
Drawn By: Sami Sirhan		File: Page2.SchDoc	Size: B
Engineer: Sami Sirhan		Contact: http://www.ti.com/support	http://www.ti.com

MGTVCCAUX - 1.8V@1A

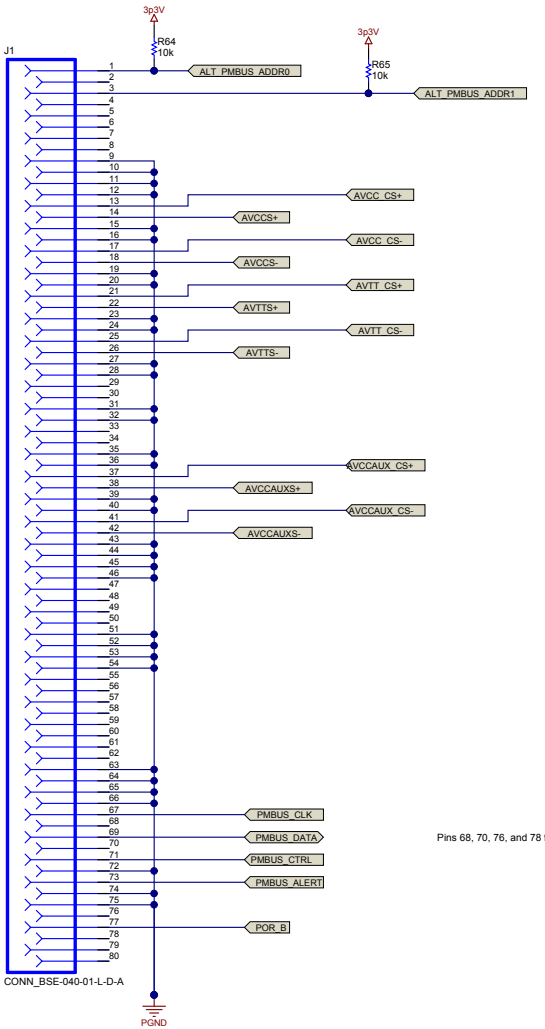


FUNCTION TABLE

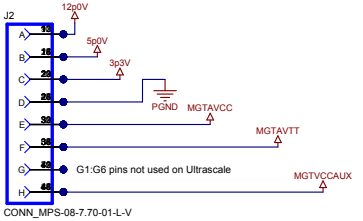
IN2	IN1	D TO S, S TO D
L	L	$D = S_1$
L	H	$D = S_2$
H	L	$D = S_3$
H	H	$D = S_4$

AVCCAUX Rail 3					
ALT_PMBUS_1	ALT_PMBUS_0	HEX	OCTAL	Raddr1 (kohm)	Raddr0 (kohm)
GND	GND	0x33	63	130	36.5
GND	OPEN	0x2B	53	84.5	36.5
OPEN	GND	0x23	43	54.9	36.5
OPEN	OPEN	0x1B	33	36.5	36.5

Designed for: Public Release		Mod. Date: 6/27/2014	
Project Title: PMP9463 Xilinx Ultrascale Kintex MGT			
Number: PMP9463	Rev: E1	Sheet Title: MGTVCCAUX	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 6
Drawn By: Sami Sirhan		File: Page3.SchDoc	Size: B
Engineer: Sami Sirhan		Contact: http://www.ti.com/support	http://www.ti.com



Pins 68, 70, 76, and 78 for I2C not used



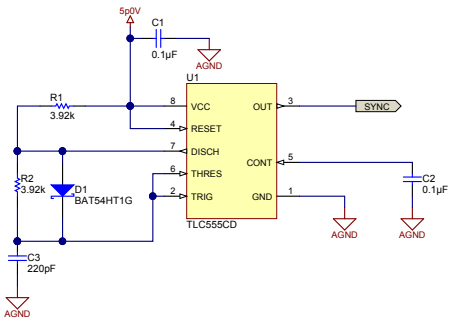
MGTAVCC on Ultrascale. Previously called MGTHAVCC on Gen 6 and 7-series

MGTAVTT on Ultrascale. Previously called MGTAVCCRX on Gen 6 and MGTHAVTT on 7-series

Pins 29, 30, 33, and 34 not used for Ultrascale. Previously called MGTHAVTT on Gen 6.

MGTVCCAUX on Ultrascale. Previously called MGTAVCCPLL on Gen 6 and MGTHVCCAUX on 7-series

SYNC CIRCUIT



500kHz fsw

Designed for: Public Release		Mod. Date: 6/27/2014	
Project Title: PMP9463 Xilinx Ultrascale Kintex MGT			
Number: PMP9463	Rev: E1	Sheet Title: Connector	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 6
Drawn By: Sami Sirhan		File: Connector.SchDoc	Size: B
Engineer: Sami Sirhan		Contact: http://www.ti.com/support	http://www.ti.com

DNP FID1 DNP FID2 DNP FID3 DNP FID4 DNP FID5 DNP FID6

PCB Number: PMP9463
PCB Rev: E1

PCB
LOGO
Texas Instruments

Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Designed for: Public Release		Mod. Date: 3/28/2014	
Project Title: PMP9463 Xilinx Ultrascale Kintex MGT			
Number: PMP9463	Rev: E1	Sheet Title: Hardware	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 6 of 6
Drawn By: Sami Sirhan		File: Hardware.SchDoc	Size: B
Engineer: Sami Sirhan		Contact: http://www.ti.com/support	http://www.ti.com

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