Buttons, Switches, LEDs
SHEET 2

DDR III
SHEET 3

FMC CONN
SHEET 4

ARRIA High Speed Bank
SHEETS 5

ARRIA V I/O
SHEETS 6-12

FPGA Configuration
SHEETS 13

ARRIA V POWER
SHEETS 14

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SHEETS 15

FPGA Decoupling
SHEET 16

USB
SHEET 17

Supply Voltage Supervisors
SHEET 18

POWER SUPPLIES
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NOTE: DNI = DO NOT INSTALL COMPONENT.

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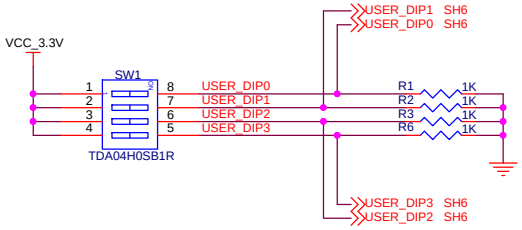
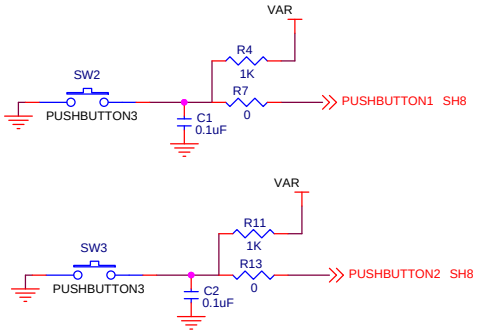
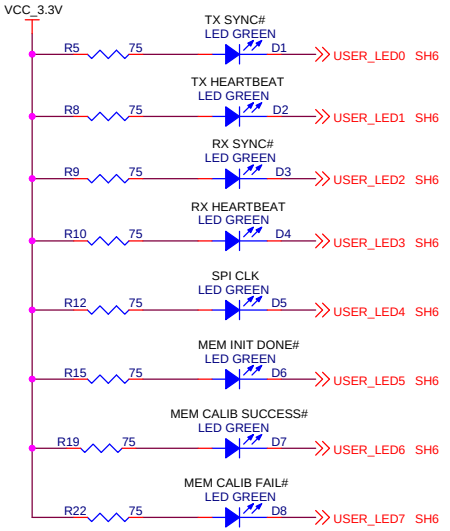
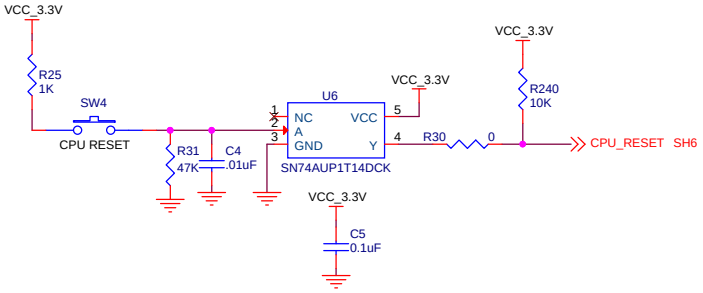
Drawn: L. NGUYEN	Size B	Document Number	Rev B
Engineer J. SETON / E. DWOBENG	Date: Monday, May 05, 2014	Sheet 1 of 21	

Buttons, Switches, LEDs

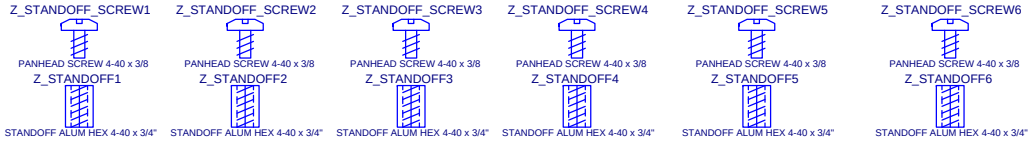








MECHANICAL PARTS



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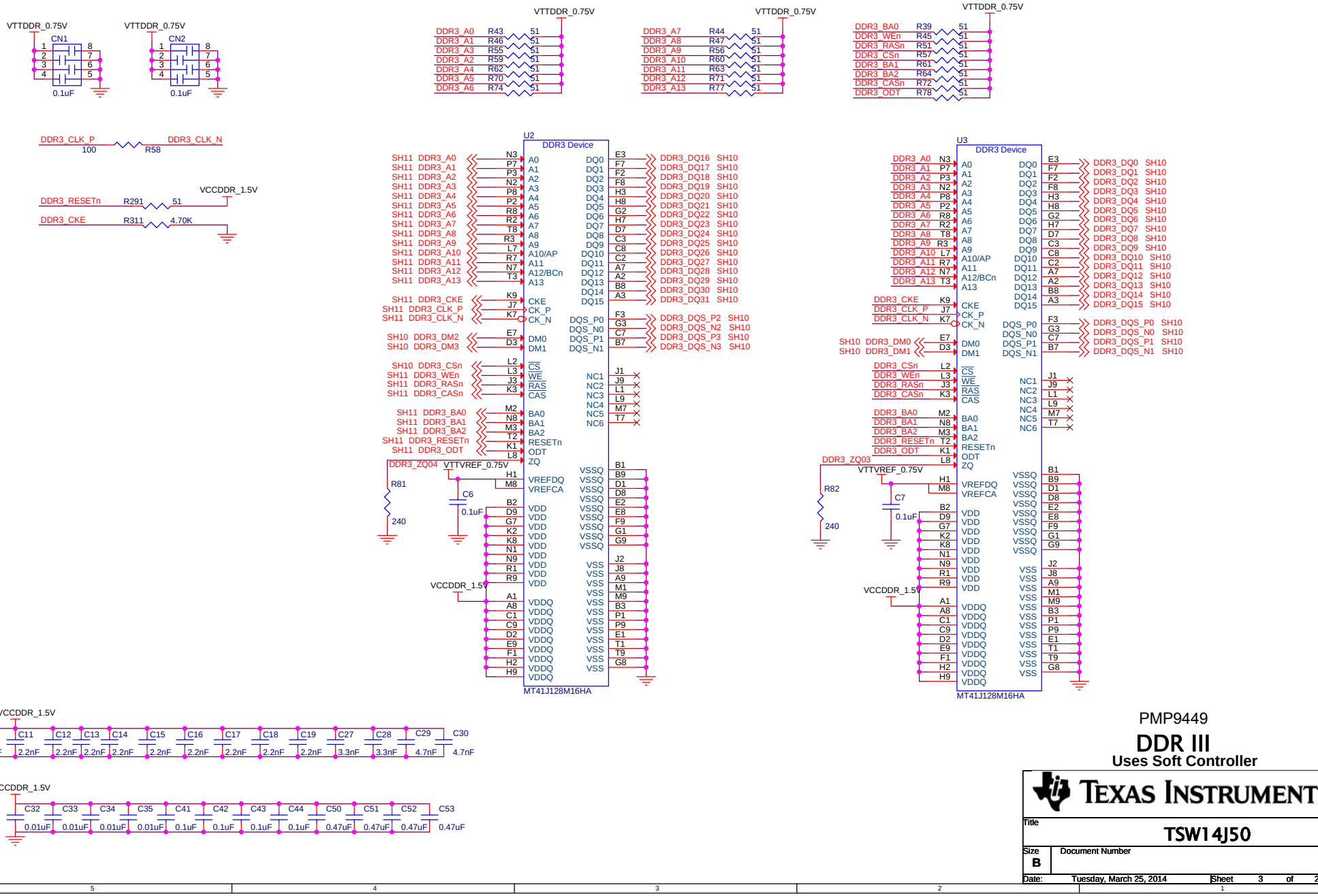

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DDR III

Uses Soft Controller

TEXAS INSTRUMENTS

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Size B	Document Number		Rev B
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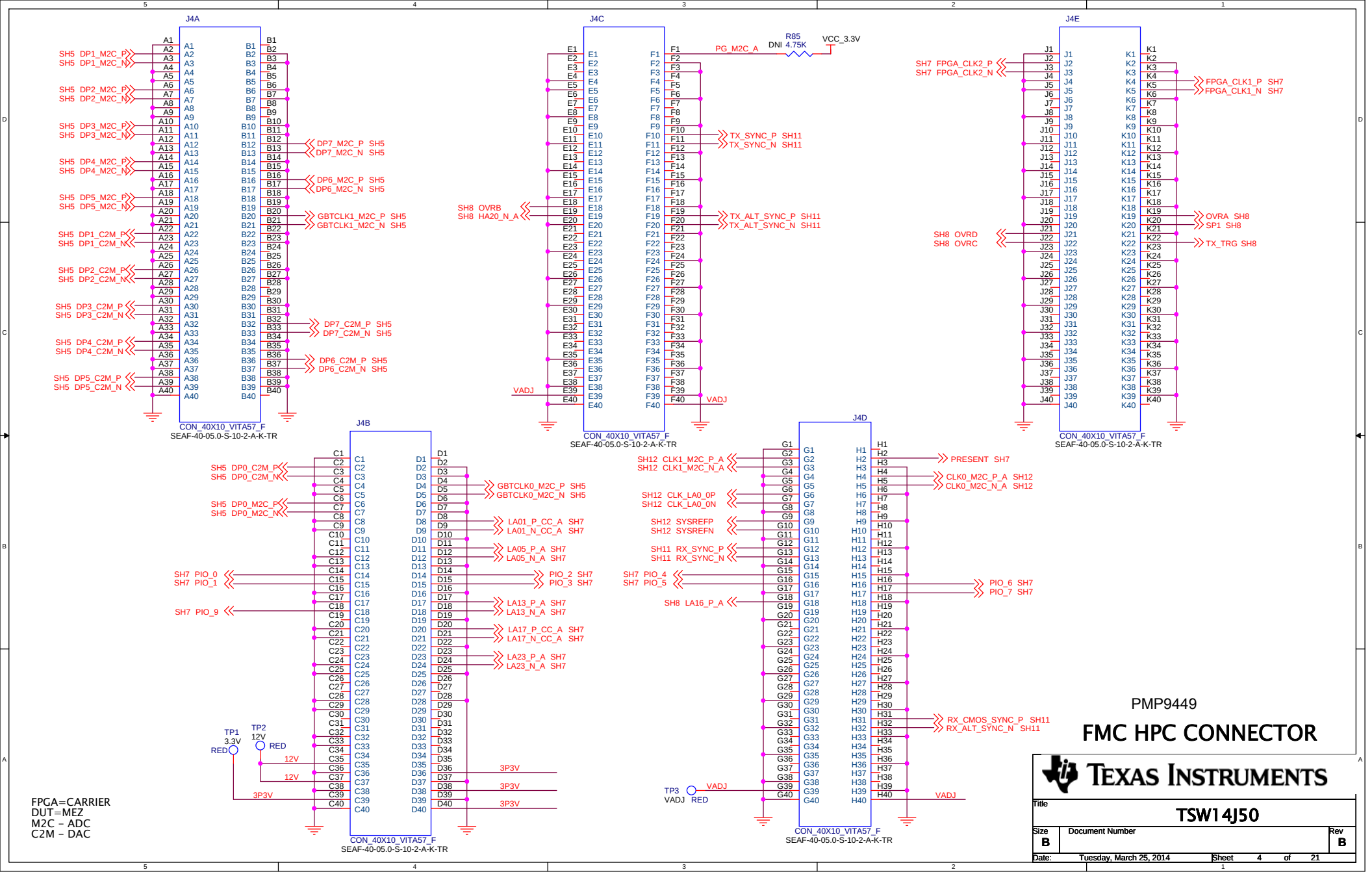
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SH5 DP1_M2C_N
SH5 DP2_M2C_P
SH5 DP2_M2C_N
SH5 DP3_M2C_P
SH5 DP3_M2C_N
SH5 DP4_M2C_P
SH5 DP4_M2C_N
SH5 DP5_M2C_P
SH5 DP5_M2C_N
SH5 DP1_C2M_P
SH5 DP1_C2M_N
SH5 DP2_C2M_P
SH5 DP2_C2M_N
SH5 DP3_C2M_P
SH5 DP3_C2M_N
SH5 DP4_C2M_P
SH5 DP4_C2M_N
SH5 DP5_C2M_P
SH5 DP5_C2M_N
DP7_M2C_P SH5
DP7_M2C_N SH5
DP6_M2C_P SH5
DP6_M2C_N SH5
GBTCLK1_M2C_P SH5
GBTCLK1_M2C_N SH5
DP7_C2M_P SH5
DP7_C2M_N SH5
DP6_C2M_P SH5
DP6_C2M_N SH5
CON_40X10_VITA57_F
SEAF-40-05.0-S-10-2-A-K-TR
J4C
PG_M2C_A
R85
DNI 4.75K
VCC_3.3V
TX_SYNC_P SH11
TX_SYNC_N SH11
SH8 OVRB
SH8 HA20_N_A
TX_ALT_SYNC_P SH11
TX_ALT_SYNC_N SH11
VADJ
CON_40X10_VITA57_F
SEAF-40-05.0-S-10-2-A-K-TR
J4E
SH7 FPGA_CLK2_P
SH7 FPGA_CLK2_N
FPGA_CLK1_P SH7
FPGA_CLK1_N SH7
OVRA SH8
SP1 SH8
SH8 OVRD
SH8 OVRC
TX_TRG SH8
CON_40X10_VITA57_F
SEAF-40-05.0-S-10-2-A-K-TR
J4B
SH5 DP0_C2M_P
SH5 DP0_C2M_N
SH5 DP0_M2C_P
SH5 DP0_M2C_N
GBTCLK0_M2C_P SH5
GBTCLK0_M2C_N SH5
LA01_P_CC_A SH7
LA01_N_CC_A SH7
LA05_P_A SH7
LA05_N_A SH7
SH7 PIO_0
SH7 PIO_1
PIO_2 SH7
PIO_3 SH7
SH7 PIO_9
LA13_P_A SH7
LA13_N_A SH7
LA17_P_CC_A SH7
LA17_N_CC_A SH7
LA23_P_A SH7
LA23_N_A SH7
TP1
3.3V
RED
TP2
12V
RED
12V
12V
3P3V
3P3V
3P3V
3P3V
CON_40X10_VITA57_F
SEAF-40-05.0-S-10-2-A-K-TR
J4D
SH12 CLK1_M2C_P_A
SH12 CLK1_M2C_N_A
SH12 CLK_LA0_0P
SH12 CLK_LA0_0N
SH12 SYSREFP
SH12 SYSREFN
SH11 RX_SYNC_P
SH11 RX_SYNC_N
SH7 PIO_4
SH7 PIO_5
SH8 LA16_P_A
PRESENT SH7
CLK0_M2C_P_A SH12
CLK0_M2C_N_A SH12
PIO_6 SH7
PIO_7 SH7
RX_CMOS_SYNC_P SH11
RX_ALT_SYNC_N SH11
TP3
VADJ
RED
VADJ
VADJ
CON_40X10_VITA57_F
SEAF-40-05.0-S-10-2-A-K-TR
FPGA=CARRIER
DUT=MEZ
M2C - ADC
C2M - DAC
PMP9449
FMC HPC CONNECTOR
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Title
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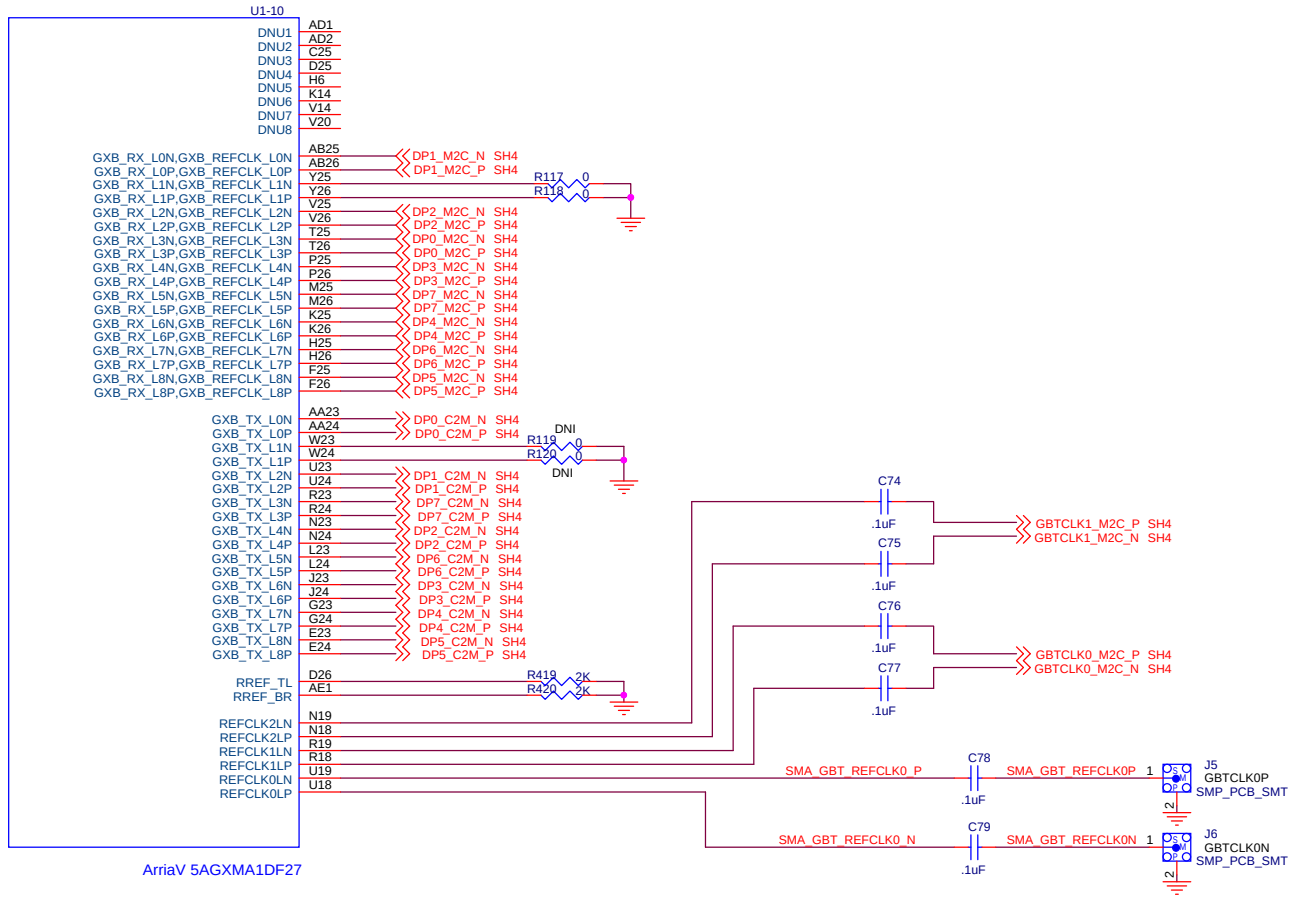

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HIGH SPEED BANK

TEXAS INSTRUMENTS

Title: TSW14J50

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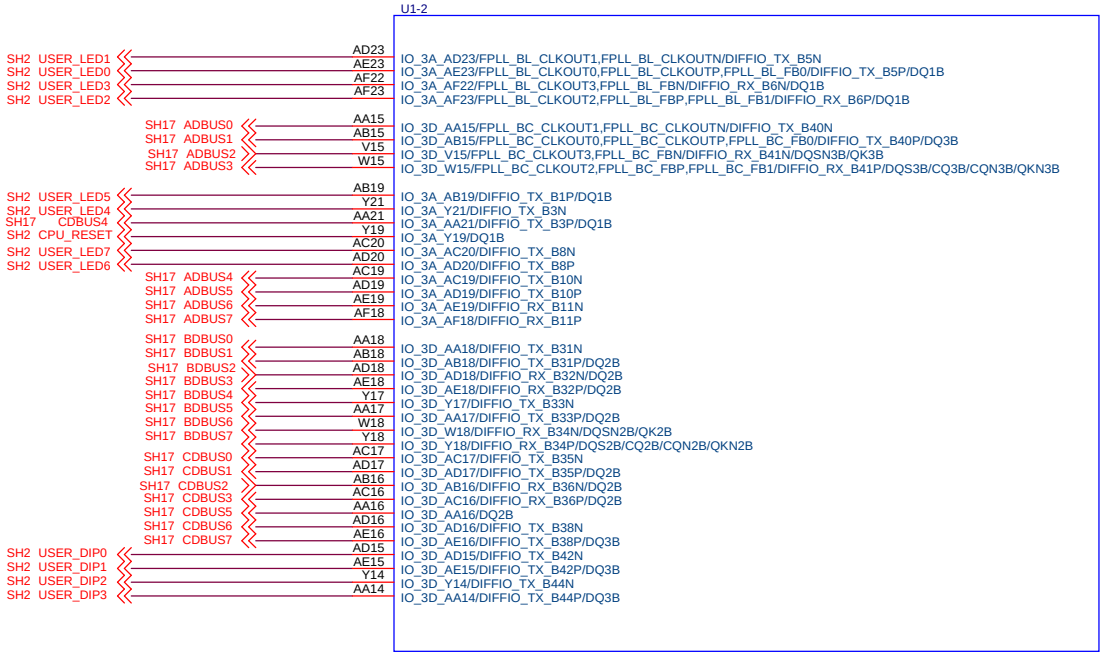

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BANK 3

TEXAS INSTRUMENTS

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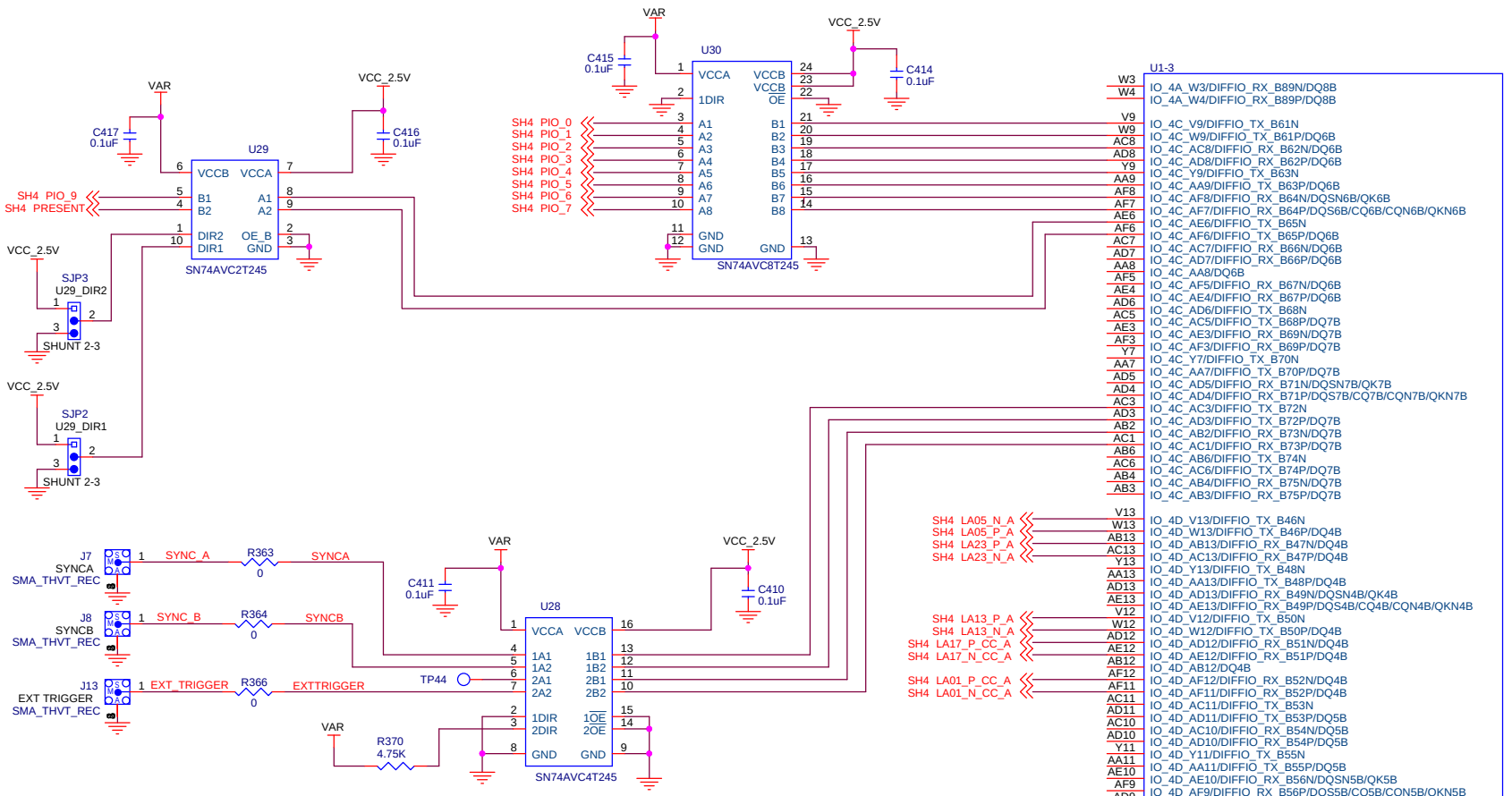

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BANK 4C (3.3V)
BANK 4D (2.5V)

TEXAS INSTRUMENTS

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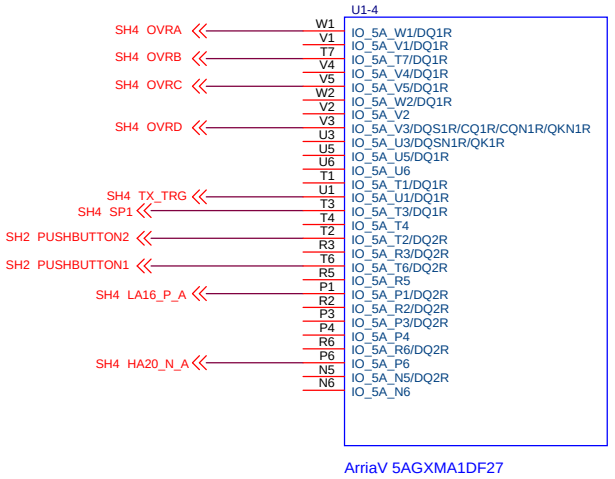

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FPGA Bank 5A (VAR)

TEXAS INSTRUMENTS

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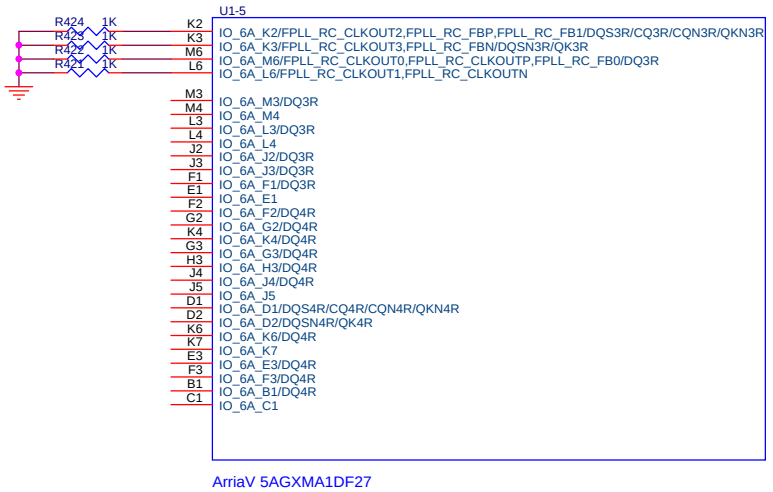

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FPGA Bank 6 (2.5V)

TEXAS INSTRUMENTS

Title: TSW14J50		
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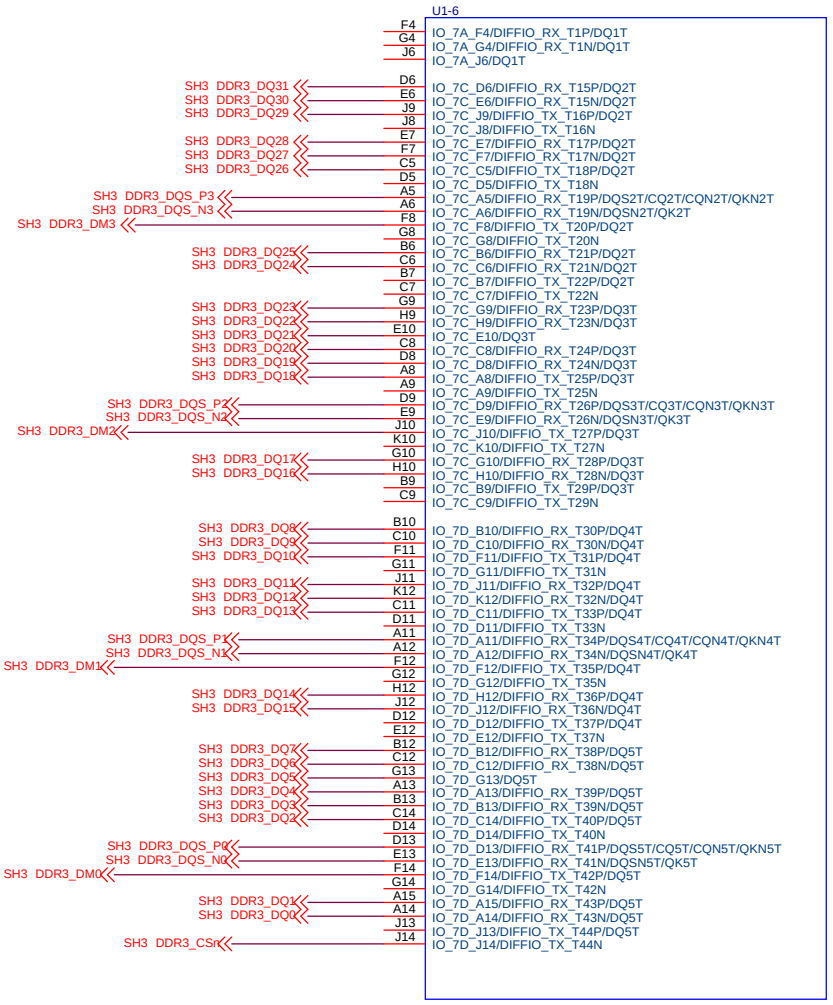

PMP9449

DDRIII - FPGA Bank 7C & 7D (1.5V)

TEXAS INSTRUMENTS

Title: TSW14J50		
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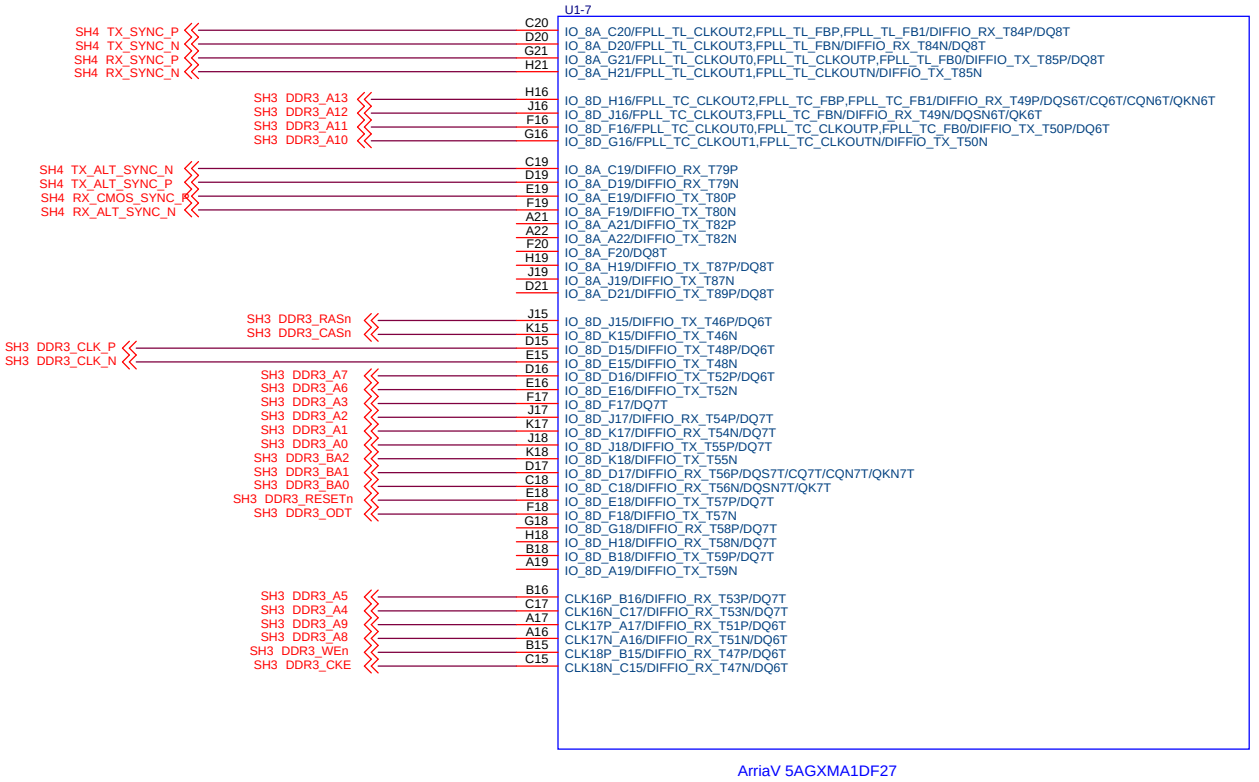

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DDRIII - FPGA Bank 8D (1.5V)
FPGA Bank 8A (2.5V)

TEXAS INSTRUMENTS

Title: TSW14J50		
Size: B	Document Number	Rev: B
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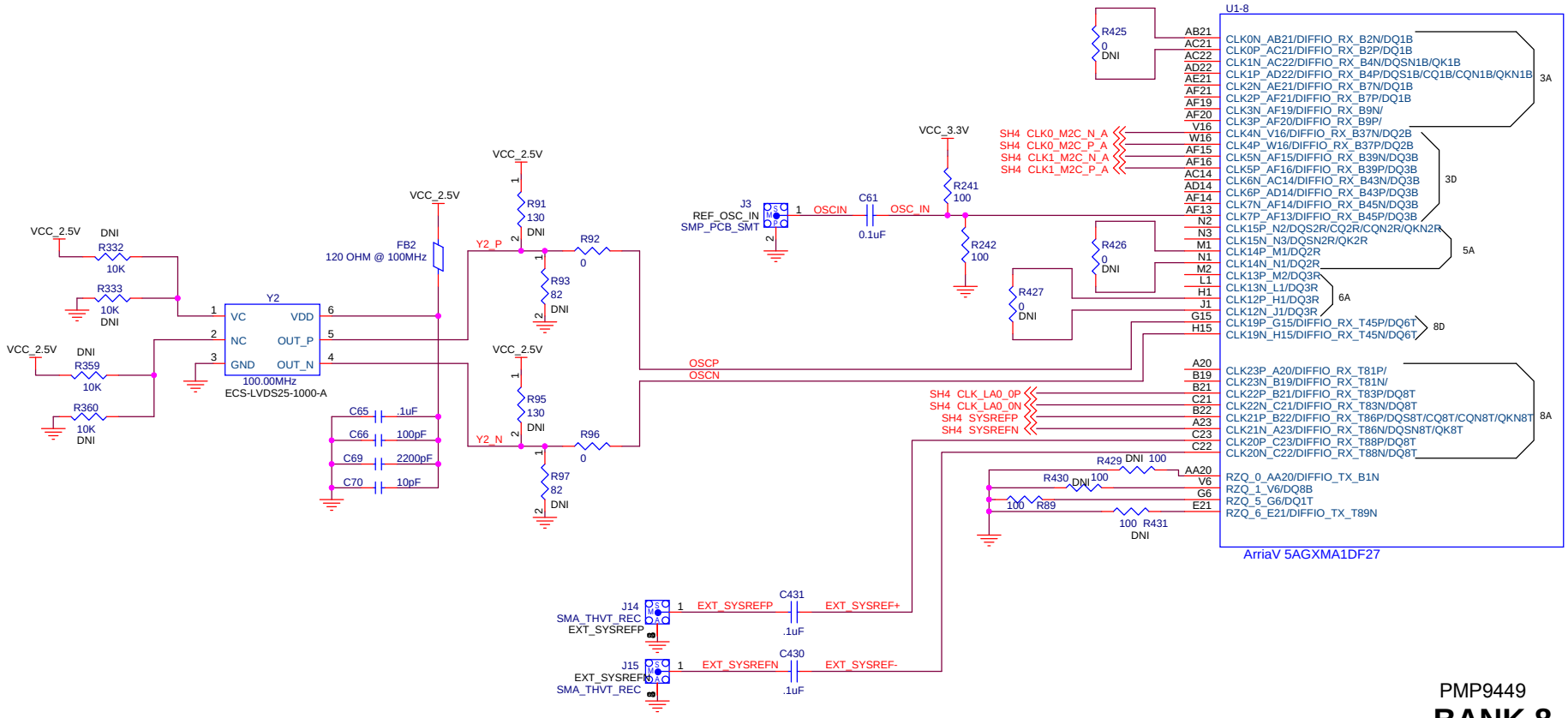

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BANK 8

TEXAS INSTRUMENTS

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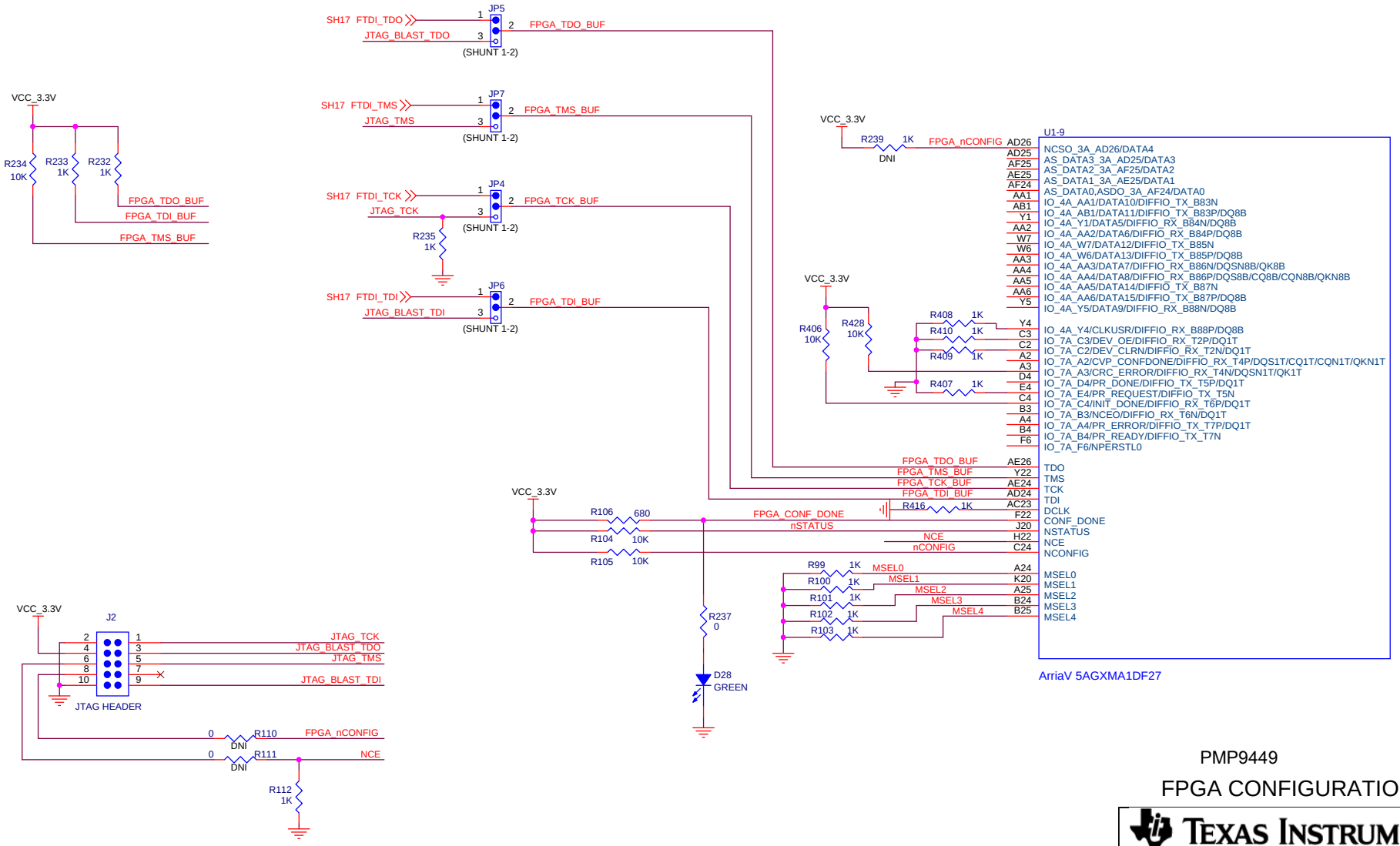

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FPGA CONFIGURATION

TEXAS INSTRUMENTS

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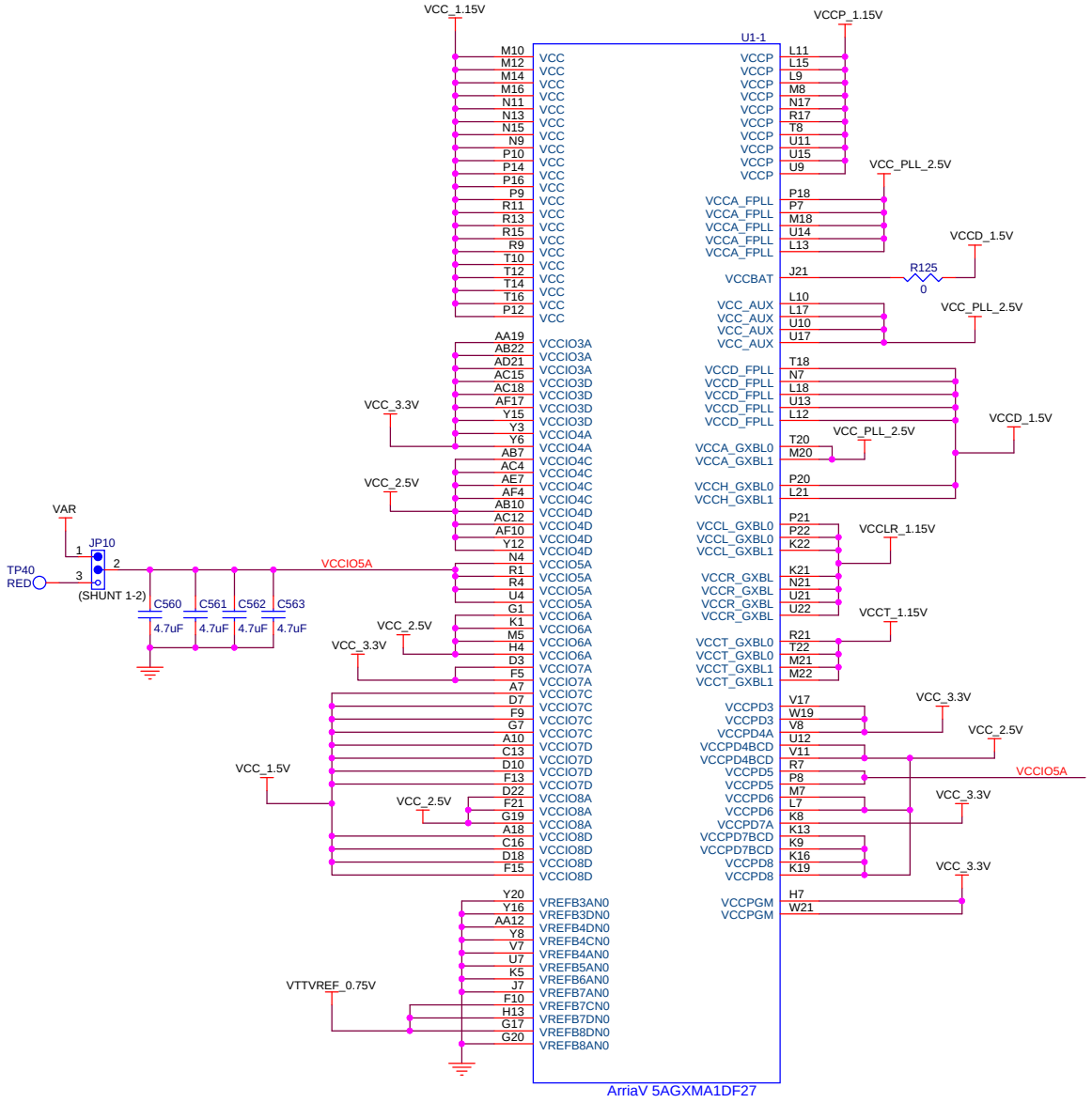

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FPGA POWER

TEXAS INSTRUMENTS

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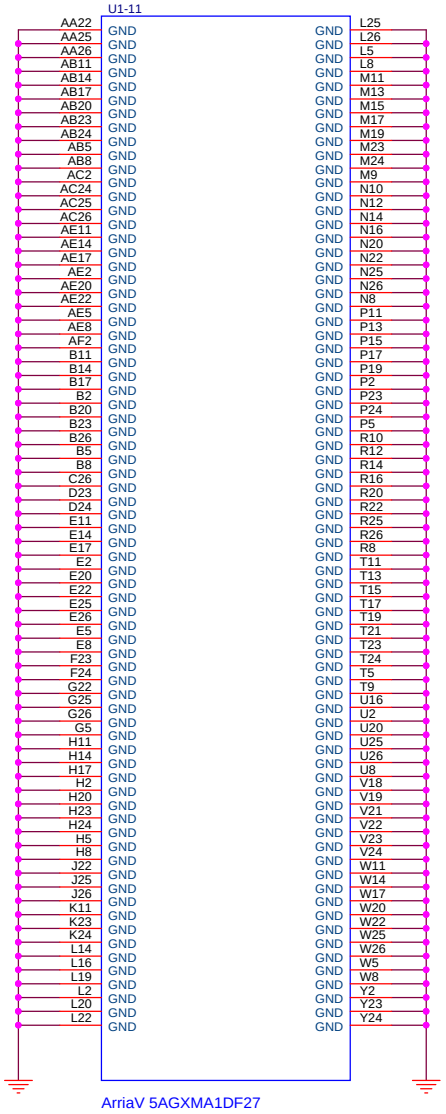

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FPGA GROUND

TEXAS INSTRUMENTS

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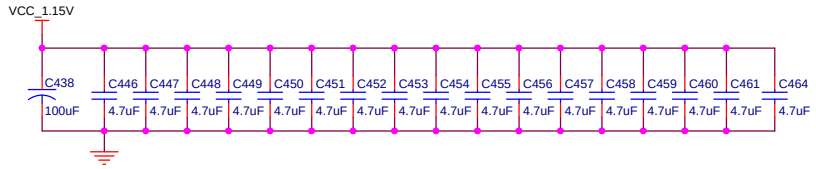

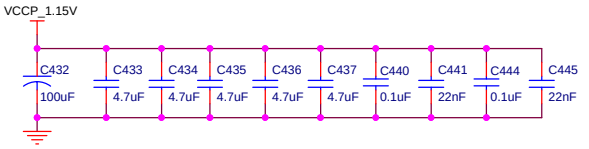

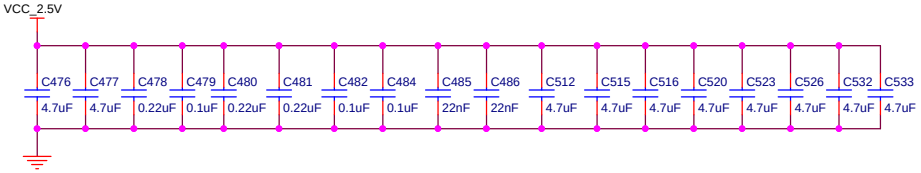

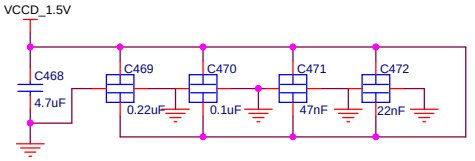

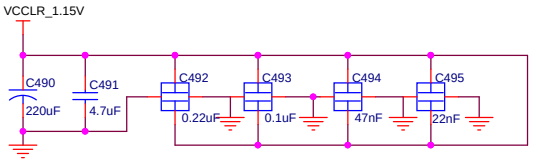

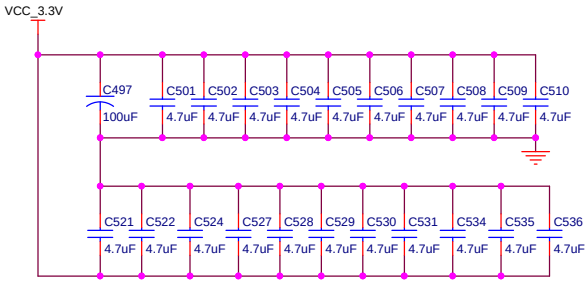

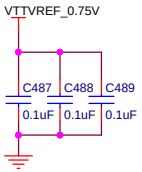

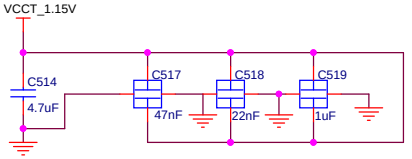

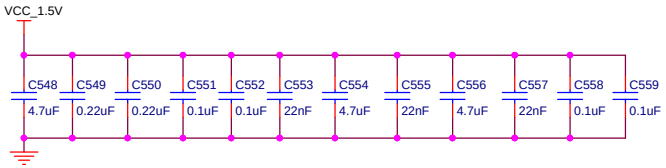

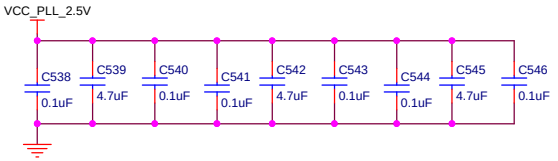

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FPGA Decoupling

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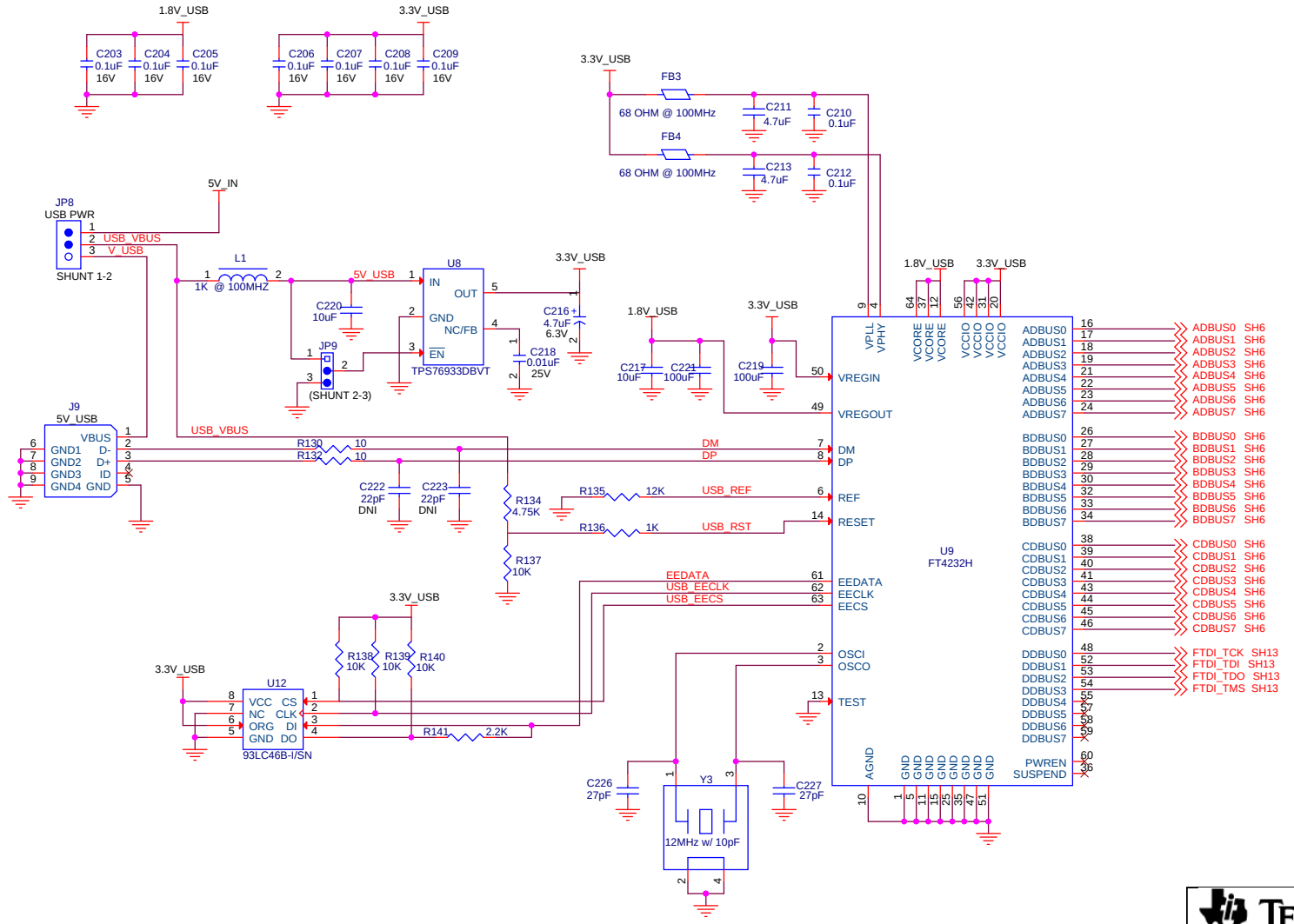

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USB

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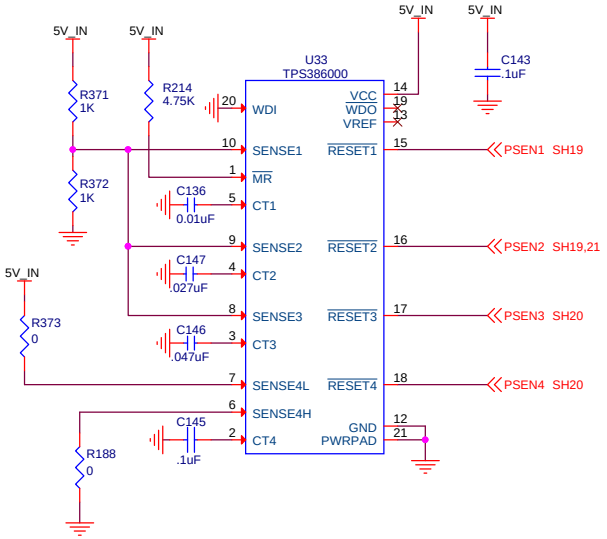

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SEQUENCER

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Size B	Document Number	Rev B
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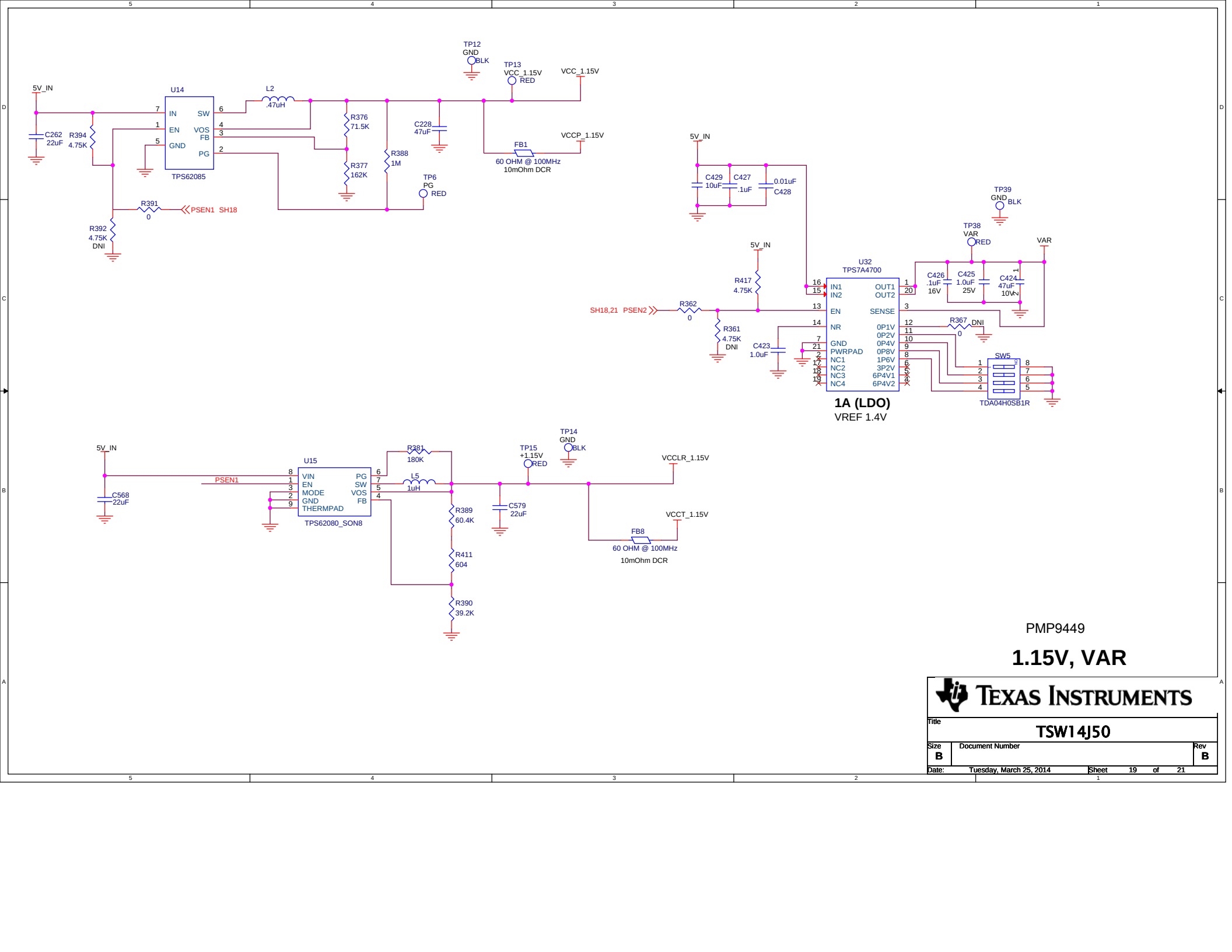

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1.15V, VAR

TEXAS INSTRUMENTS

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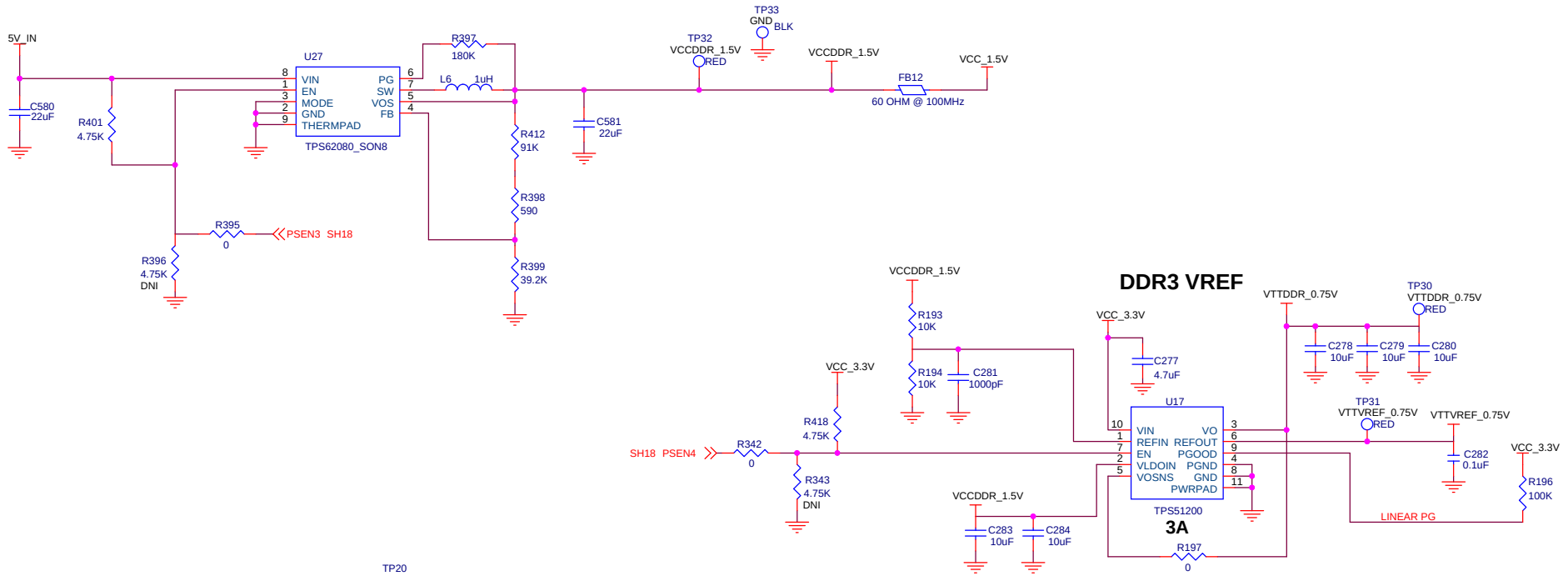

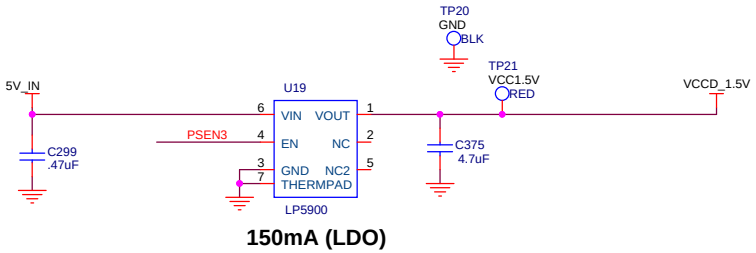

150mA (LDO)

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0.75V, 1.5V

TEXAS INSTRUMENTS

Title: TSW14J50		
Size: B	Document Number	Rev: A
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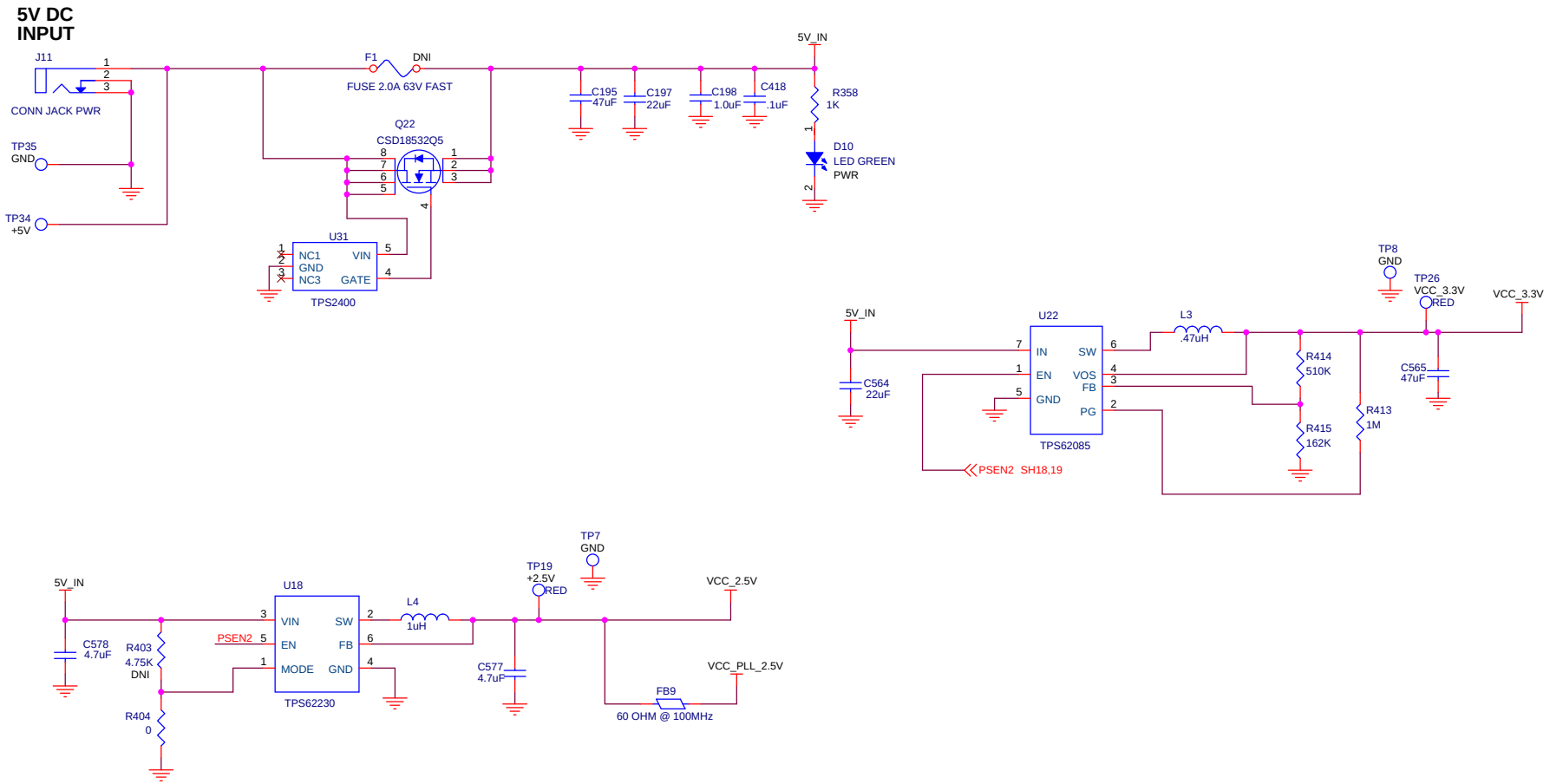

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3.3V, 2.5V

TEXAS INSTRUMENTS

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