**NOTES:**
1) R18 for test purposes only
2) R2, R3 causes 50uA bias each
3) built on PCB PMP5638RevA

**REV B:**
1) adjusted loop & RC snubber R7
2) added additional input caps externally
3) added C200

**ASSEMBLY:**
1) C6, C21, D1, J5, R23, R13 OPEN
2) L100 mounted externally, scratch trace at pad C6
3) pull up R100 mounted externally

**EXPECTED OUTPUT RIPPLE:**
30mVpp (16SVPE470M - expected 23mV)

**TPS40170**
1) 5V Sync Buck
2) 3.3V enabled
3) short to disable

**VIN CONNECTIVITY:**
- Master: VIN
- Slave 180 deg = GND
- Slave 0 deg = OPEN

**SWITCHING FREQUENCY:**
100kHz

**EXPECTED PERFORMANCE:**
- Short circuit multiplier, Vin 36Vdc to 44Vdc set to "x 7"
- Vref 600mV
- 9.83Arms each LS FET
- 23.23A sat
- 4.45amps
- winding losses 1281mW
- core losses 8mW
- AC losses 1mW
- total losses 1290mW
- temperature rise 26K

**ENGINEER:**
- B. Geck

**DRAWN BY:**
- B. Geck

**DATE:**
- 6/18/2012

**FILENAME:**
- PMP7165RevB.sch

**SIZE:**
- B

**NUMBER:**
- PMP7165

**REVISION:**
- A
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