The Stackup Legend below this is static.
If you change the stackup, update the Legend.

Layer Stack Up Detail for: Ref_Design.PcbDoc

Layer Name	Gerber Document	Copper Thickness	Dielectric Material
Top Solder Mask	(.GTS)		Solder Resist
Top Layer	(.GTL)	1.4mil	FR-4
Bottom Layer	(.GBL)	1.4mil	
Bottom Solder Mask	(.GBS)		Solder Resist

DESIGN INFORMATION

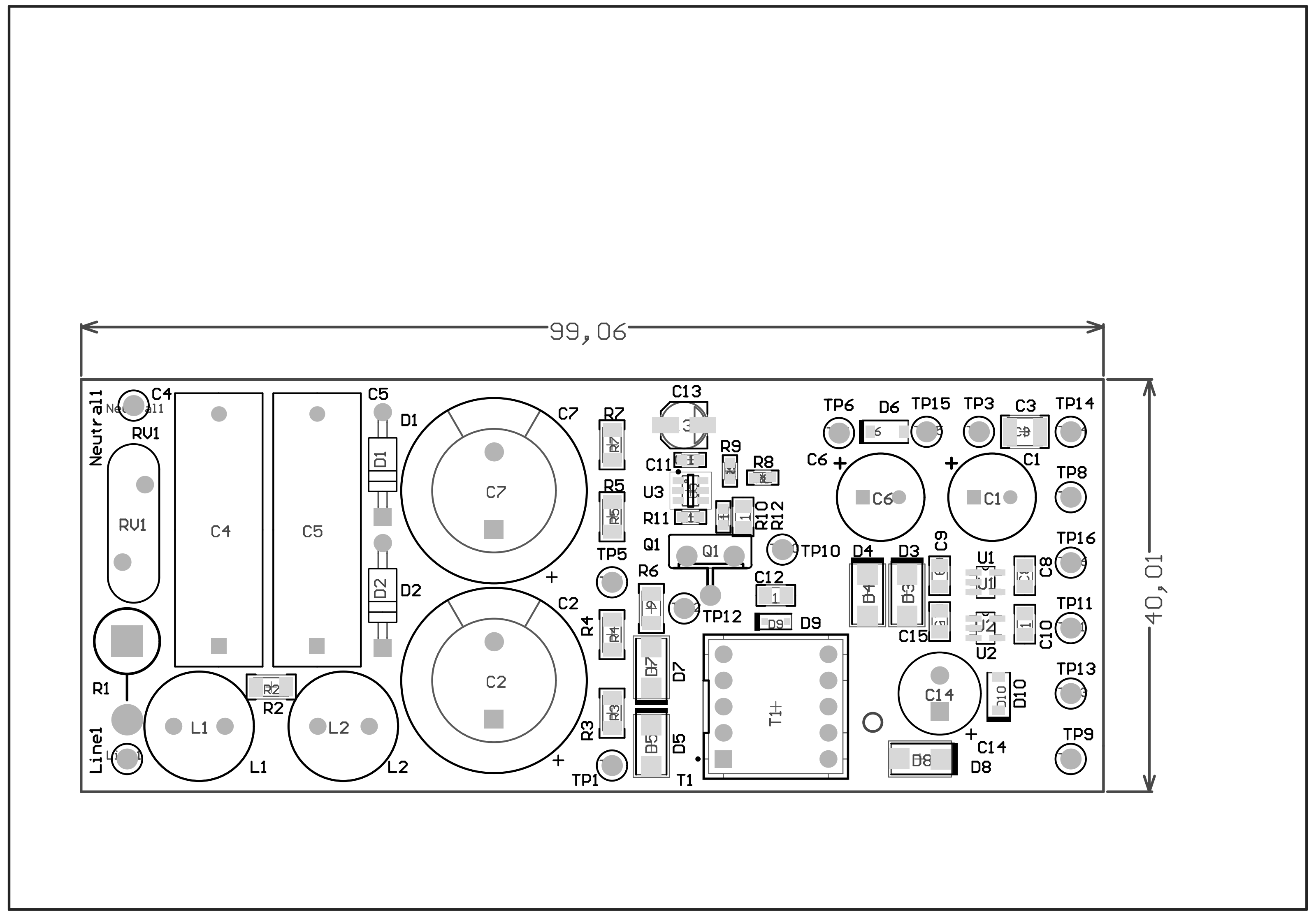
BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
3450MIL X 4950MIL

Number of Layers : 2
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 8 MIL
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
COPPER THICKNESS (FINISHED):
OUTER: [X] 1.4MIL (1oz) [ ] 2MIL (1.4oz) [ ] 2.8MIL (2oz)
INNER SIGNAL: [X] 1.4MIL (1oz) [ ] 2.8MIL (2oz) [ ] N/A
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR:
[X] GREEN [ ] BLUE [ ] OTHER
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK

This document can handle board shapes up to 7.9in x 10in, although
our panel vendors top out at 7in x 10in.
To re-size the board shape, do the following:
Select lines on M1 Board Outline and delete (easy in single layer mode...shift+s)
Draw a rectangle using lines (example will be for a 4 x 6 board
Enter Place Line mode (keyboard pl)
keyboard jo to jump to origin, hit enter
keyboard jl to jump to location, set x to 6000, hit enter twice
keyboard jl to jump to location, set x to 6000 and y to 4000, hit enter twice
keyboard jl to jump to location, set x to 0 and y to 4000, hit enter twice
keyboard jo to jump to origin, hit enter
Hit ESC twice to exit place line mode
Select lines on M1 Board Outline
Menu Design|Board Shape|Define from Selected Objects (keyboard dsd)
To define a Keep-Out that mirrors the board outline:
Menu Design|Board Shape|Create Primitives From Board Shape (keyboard dsp)
Set the Keep-Out Layer as the layer, set width as preferred
Ensure Route Tool Outline is selected, hit enter

If you re-size the board, don't forget to move the drill table strings on the
Drill Drawing Layer...they should be just to the right of your board shape



←1000 (mil)→

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK VIEWED FROM TOP SIDE | BOARD #: PMP10055 | REV: n/a
LAYER NAME = Top Overlay | IGNORE
PLOT NAME = Top Assembly Drawing | GENERATED : 07 OCT 2015 17:04:00 | TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

PROJECT TITLE:
140V...440V Non-isolated Flyback + 2 x LDO

DESIGNED FOR:

FILE NAME:
PMP10055 Rev_A AC Stacking Layout.PcbDoc

ENGINEER:
R. Scibilia

LAYOUT BY:
R. Scibilia

SCALE: 1.00

ALTIUM DESIGNER VERSION:
10.0.0.27009

The Stackup Legend below this is static.
If you change the stackup, update the Legend.

Layer Stack Up Detail for: Ref_Design.PcbDoc

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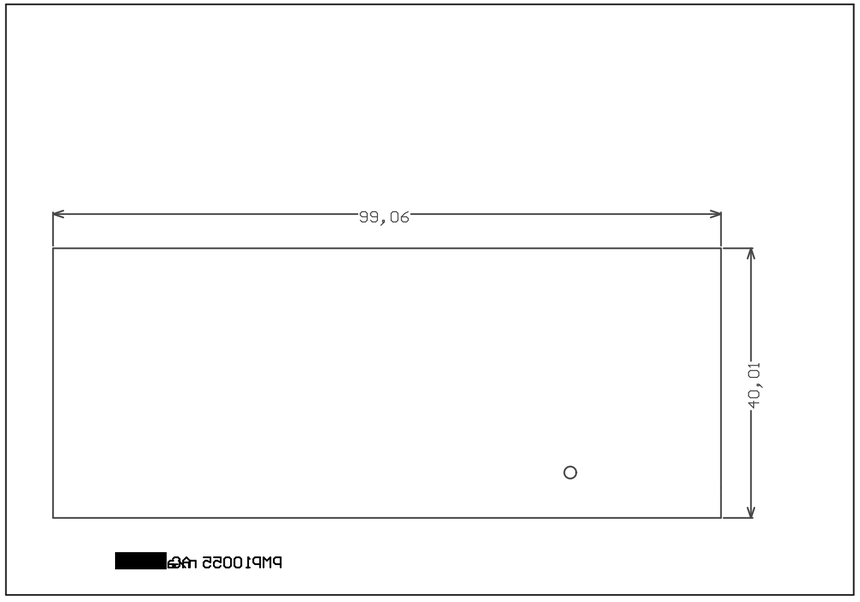
INNER SIGNAL: [X] 1.4MIL (1oz) [ ] 2.8MIL (2oz) [ ] N/A
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER _____
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR:
[X] GREEN [ ] BLUE [ ] OTHER _____
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK



1000 (mil)

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

Texas Instruments

PROJECT TITLE: 140V...440V Non-isolated Flyback + 2 x LDO	
DESIGNED FOR:	
FILE NAME: PMP10055 Rev_A AC Stacking Layout.PcbDoc	
ENGINEER: R. Scibilia	LAYOUT BY: R. Scibilia
SCALE: 1.00	ALTIUM DESIGNER VERSION: 10.0.0.27009

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