

Design goal: All parts excluding Test Interface in 25 mm by 16 mm "Box"

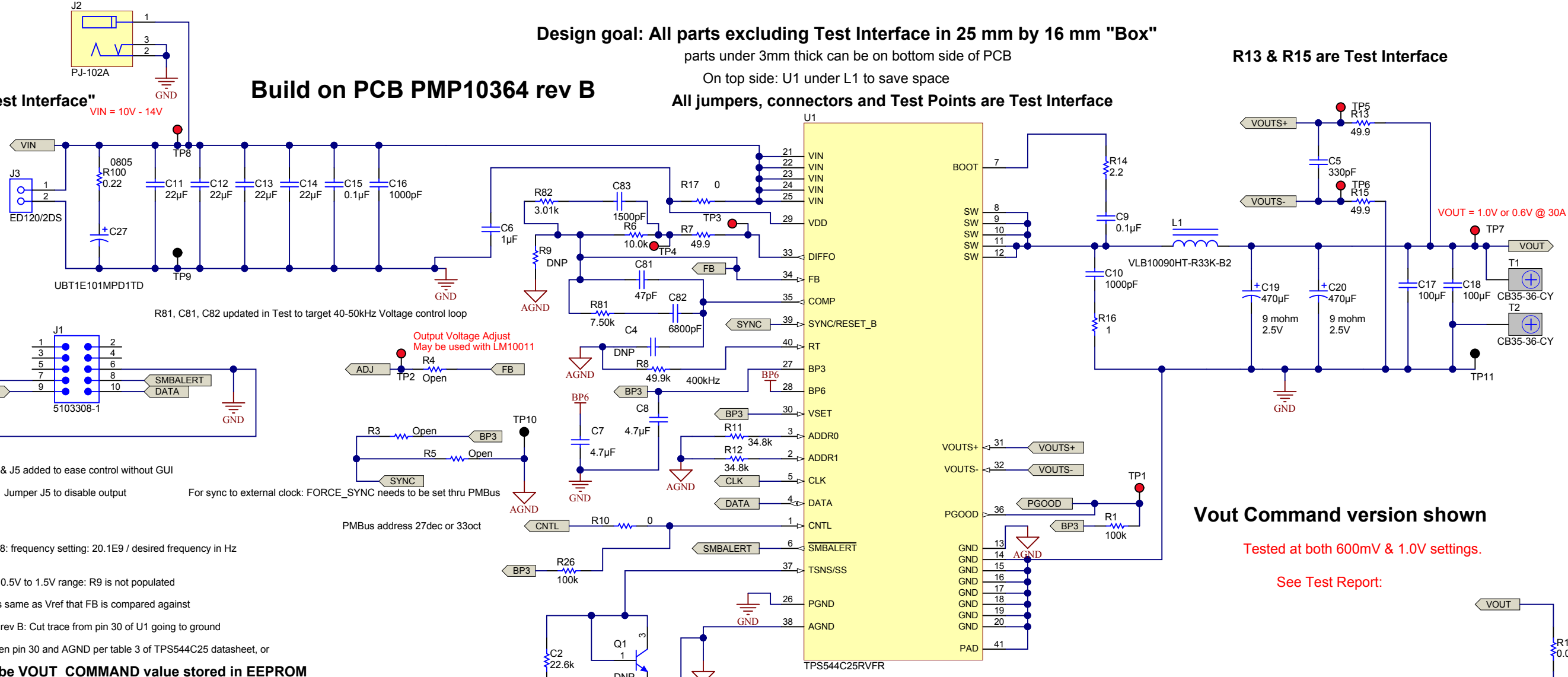
parts under 3mm thick can be on bottom side of PCB
On top side: U1 under L1 to save space

All jumpers, connectors and Test Points are Test Interface

R13 & R15 are Test Interface

R100 & C27 are "Test Interface"

Build on PCB PMP10364 rev B



Vout Command version shown

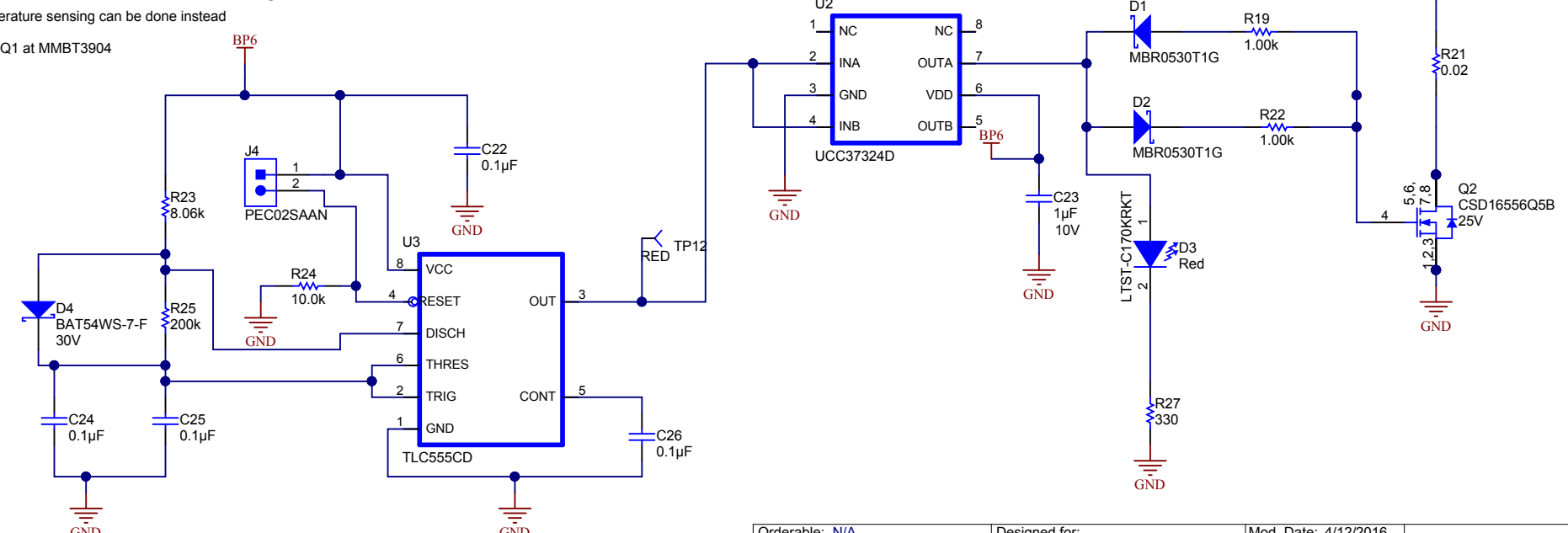
Tested at both 600mV & 1.0V settings.

See Test Report:

~15A pulses off 1.0V with 2-3 usec rise/fall with values shown

For 600mV output R18, R20, R21 each become 10mOhms

Dynamic Test Load: All parts are "Test Interface"



5% duty cycle to keep load from overheating 30-40 Hz

A
B
C
D

A
B
C
D

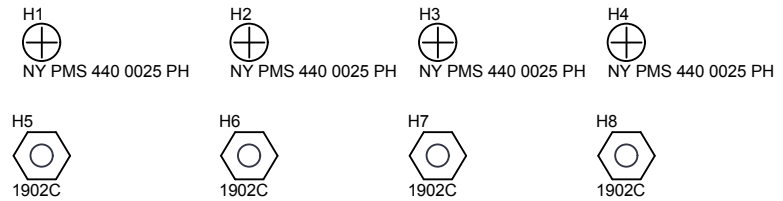
For TPS544C25: R8: frequency setting: 20.1E9 / desired frequency in Hz
For Vout in the 0.5V to 1.5V range: R9 is not populated
Target Vout is same as Vref that FB is compared against
On PCB PMP10364 rev B: Cut trace from pin 30 of U1 going to ground
Solder in resistor (Rvset) between pin 30 and AGND per table 3 of TPS544C25 datasheet, or

tie pin 30 to BP3 to have Vref be VOUT_COMMAND value stored in EEPROM

for 600mV version, tie pin 30 to BP3 as shown for VOUT_COMMAND mode.

Output caps C19 & C20 as shown for 2V outputs and lower
For higher Vouts: use 220uF 6.3V 18mOhms such as 6TPE220MI POSCAP

Dynamic load resistors will change with Vout
 $R18 + R20 + R21 = [Vout / \text{desired step load}] \text{ minus } 5\text{mOhms}$



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Orderable: N/A	Designed for: PMP20023	Mod. Date: 4/12/2016
TID #: PMP20023	Project Title: TPS544C25 Voltage Mode Inductor on Top	
Number: PMP20023	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 1 of 1
Drawn By:	File: PMP20023_TPS544C25_Vcommand.SchDoc	Size: B
Engineer: Josh Mandelcom	Contact: http://www.ti.com/support	© Texas Instruments 2015



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