(a) The MCU (diagnostics) is not part of this schematics. An interface is provided for the corresponding diagnostic and monitoring signals. The interface is compatible to the C2000 LaunchPad.

(b) The STO_1 subsystem is designed for CMOS input IGBT gate drivers ISO5852S and ISO5452 and pin-compatible derivative ISO5X5X. Other CMOS IGBT gate drivers like UCC21750 and UCC53xx family as well as 5V CMOS input signals can be considered too, and require modification to the schematic according to the desired IGBT gate driver.

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**NOTES**

- a) The MCU (diagnostics) is not part of this schematics. An interface is provided for the corresponding diagnostic and monitoring signals. The interface is compatible to the C2000 LaunchPad.
- b) The STO_1 subsystem is designed for CMOS input IGBT gate drivers ISO5852S and ISO5452 and pin-compatible derivative ISO5X5X. Other CMOS IGBT gate drivers like UCC21750 and UCC53xx family as well as 5V CMOS input signals can be considered too, and require modification to the schematic according to the desired IGBT gate driver.
STO_1 and STO_2: Input voltage is between 0 V and 24 V nominal with worst-case of 3.6 V as logic low and 20.4 V as logic high. No intermediate voltage is expected.

Power supply

24VIN: The 24 V input supply for the P24V is assumed to be protected against fault and remains within ±20% tolerance. If out of spec, it will be shut down to 0 V.

*Note: Not part of the TLEF concept review, needs to be a protected supply. (Refer to the TDOA-0156_STO_Concept_FMBA_1v5.docx)

NOTE: STO_1 subsystem designed for CMOS input IGBT gate drivers: ISO65355 and pin-compatible derivatives. Other CMOS gate drivers like UC28110 and UC3843 can be considered too, and require modification to the schematic according to the desired IGBT gate driver pin-out.

Drawn By: [Signature]

Contact: http://www.ti.com/support

File:

Size:

Date:

Rev:

TID #: TIDA-01599

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TIDA-01599.Safe Torque Off. SchDoc

STO_2

STO_1

Note: R15, R22 are carbon MELF resistor (pulse proof). Refer to application note slu4063 on TI.com regarding the surge protection level.
STO_2_FB threshold:
Logic 0: 0V~14V
Logic 1: ~14V~28.8V

STO_1_FB threshold:
Logic 0: 0V~2V
Logic 1: ~2V~3.9V

STO_FB is assumed to be between 0 V and 24 V nominal with worst case of 3.6 V as logic low and 20.4 V as logic high. The external supply voltage (Safe PLC 24V) to the 24V ST0-FB is assumed to be protected against over-voltage and is required to remain within 24 V ±30% tolerance.
Variant/Label Table

<table>
<thead>
<tr>
<th>Variant</th>
<th>Label Text</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>Production</td>
</tr>
</tbody>
</table>

Assembly Note

- **ZZ1**: This Assembly Note is for PCB labels only.
- **ZZ2**: These assemblies are ESD sensitive. ESD precautions shall be observed.
- **ZZ3**: These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- **ZZ4**: These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.
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