Generic Buck Design for TI Power Workshop / FAE training, using TPS40200, controlling P MOS FET, nonsynchronous rectification

Vin 8V to 16V, nominal 12V

PMOS, gate loop in between Vdd and gate drive (!)

Notes:
- Please refer to PMP7154 RevC
- All calculations for 12Vin / 1Aout
- R8 for loop test purposes only
- Q2, non-auto - just use Si2307CDS
- vout = 100mArms
- _TSS 2ms

Revised to add pseudo load page 2

R1 = 68.1k
R2 = 100k

C1 = 22uF 25V
C2 = 68uF 35V
C113 = 0.1µF 50V
C112 = 0.1µF 50V

GndOut

12V0

Wall adapter 12V

12V0

by using wall adapter check output ripple

Notes:
- Q2, non-auto - just use Si2307CDS
- vout = 100mArms

Revision History

Revision | Notes
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A | PMP7154RevC "reloaded" plus tiny load page 2 squeezed loop / tuned RC snubber
A2 | PMP7154RevC "reloaded" plus tiny load page 2 squeezed loop / tuned RC snubber

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"Easy-To-Use" electronic load, supports small transients up to 500mA

- LDO, 8Vout
- square wave generator 1kHz
- "enable transient" FET driver
- needed min. ESR around 1kHz/50%
- channel 1 & trigger, use differential probe for channel 2 for Vout
- remove bias from 12V to measure effcy
- 100mA to 500mA each & remove bias from 5V to measure effcy
- constant load
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