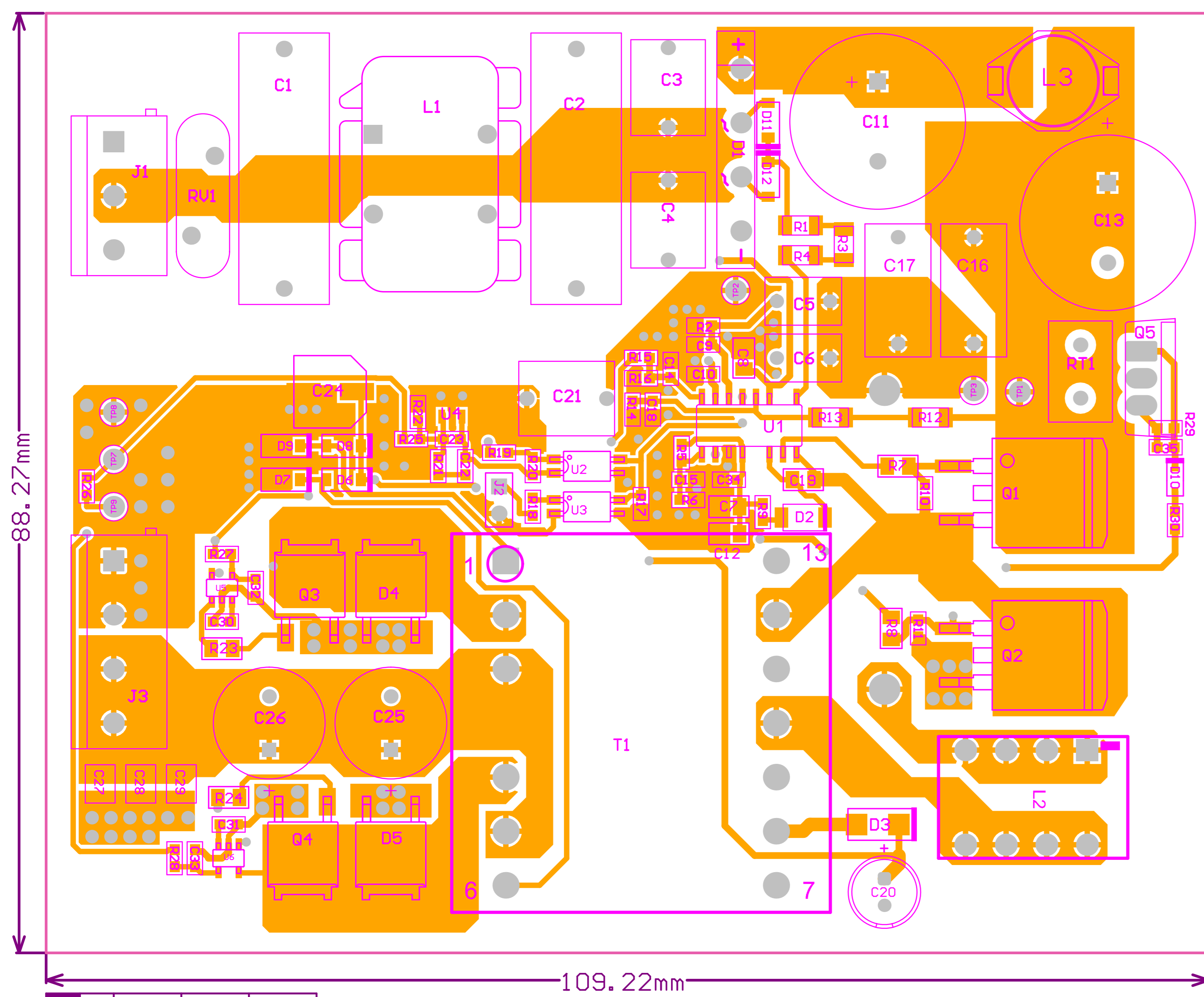


## The reference design PMP30522 Rev\_A has been built on PMP30307 Rev\_A PCB



M1 Board Outline  
 Top Layer  
 M2 Board Dimensions  
 M9 Title Sheet

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
 ASSEMBLY VARIANT: [No Variations]

| DESIGN INFORMATION  |   |
|---|---|
| MIN. TRACK WIDTH:   | 8 MIL   |
| MIN. CLEARANCE:   | 0.2 mm  |
| MIN. VIA PAD SIZE:  | 24 MIL  |
| MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL<br>PER IPC-D-275 CLASS 2 LEVEL C  |   |
| REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL<br>HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL  |   |
| MATERIAL:   |   |
| <input type="checkbox"/> FR-408 <input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER _____   |   |
| THICKNESS:  | <input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER _____  |
| TOLERANCE:  | <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2<br><input type="checkbox"/> OTHER +/- _____  |
| BOW & TWIST:  | <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2<br><input type="checkbox"/> OTHER +/- _____  |
| DRILLING:   |   |
| REFERENCE:  | <input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES   |
| PTH COPPER THICKNESS:   | <input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER _____   |
| BOARD FINISH:   |   |
| SILKSCREEN:   | <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM  |
| SILKSCREEN COLOR:   | <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER _____  |
| SOLDER RESIST COLOR:  | <input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER _____<br><input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS                     |
| SURFACE FINISH:   | <input checked="" type="checkbox"/> IMMERSION GOLD (ENIG) <input type="checkbox"/> ENEPIG<br><input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER _____ |
| ARRAY/PANEL:  | <input type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE<br><input type="checkbox"/> N.C. ROUTE <input checked="" type="checkbox"/> V. SCORE                                      |
| CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  |   |
| <input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3<br><input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER |   |
| ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.<br>PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER  |   |
| ADDITIONAL REQUIREMENTS:  |   |
| MICROSECTION: <input type="checkbox"/> YES  |   |
| BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER  |   |
| <input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  |   |
| <input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  |   |
| <input type="checkbox"/> OUTER XX MIL VIAS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  |   |
| <input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE<br>TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE  |   |

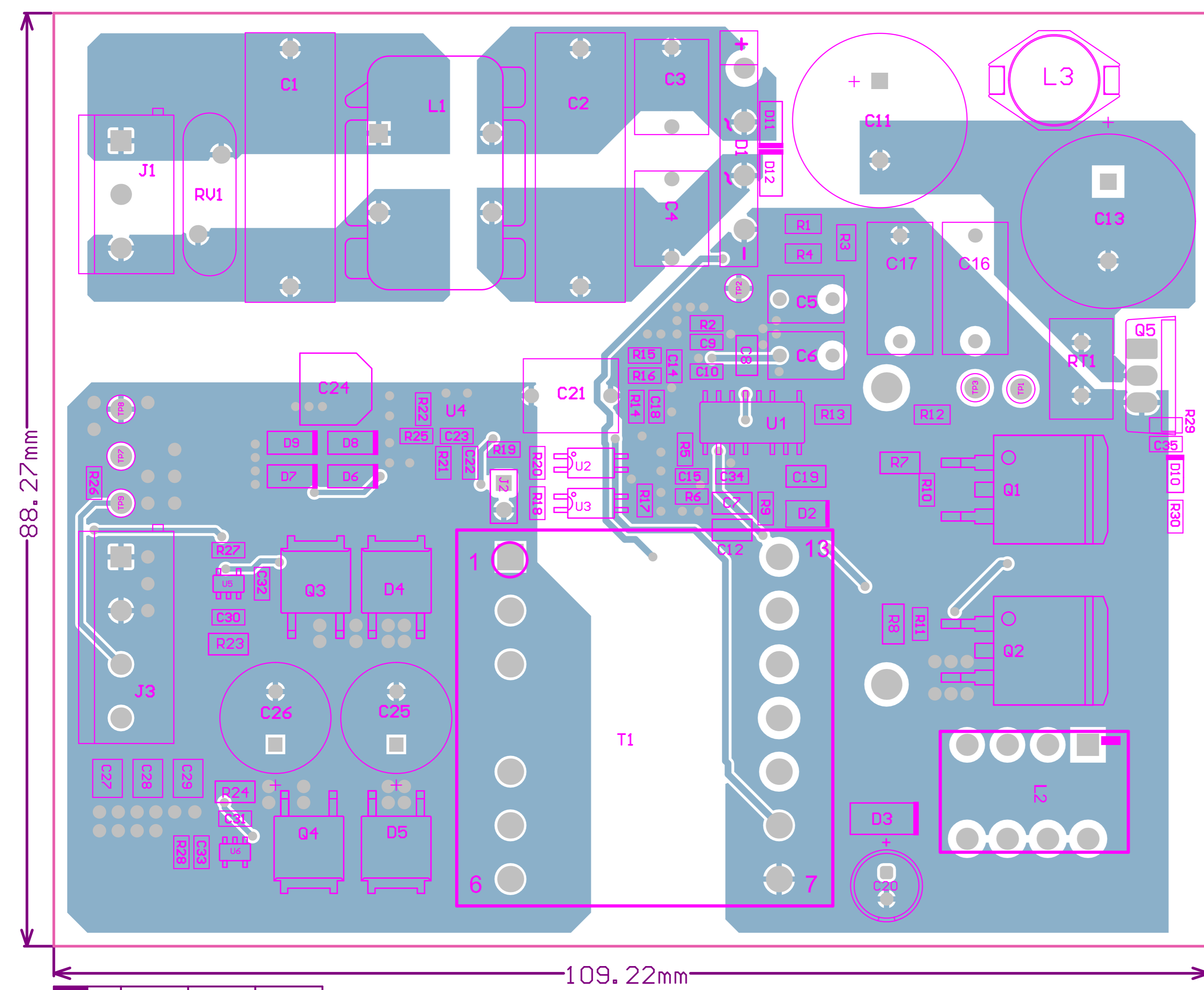


PROJECT TITLE:  
 Low-line 100VAC-127VAC 75W LLC

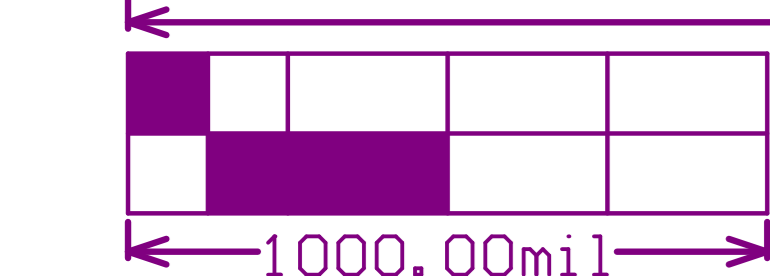
DESIGNED FOR:  
 Public Release

FILE NAME:  
 PMP30307 Rev\_A PCB.PcbDoc

|                                       |                                   |                   |                                |  |                          |  |
|---------------------------------------|-----------------------------------|-------------------|--------------------------------|--|--------------------------|--|
| PCB VIEWED FROM TOP SIDE              | BOARD #: PMP30522                 | REV: A            | SUN REV: Not In VersionControl | Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application. | ENGINEER:<br>R. Scibilia | LAYOUT BY:<br>PMP30307 Rev_A           |
| M10 Fab Notes                         | TID #: N/A                        |                   |                                |  | SCALE: 1.00              | ALTIUM DESIGNER VERSION:<br>17.1.5.472 |
| PLOT NAME = Top LayerAssembly Drawing | GENERATED : 11/26/2018 4:28:24 PM | TEXAS INSTRUMENTS |                                |  |                          |  |



M1 Board Outline  
 M2 Board Dimensions  
 Bottom Layer  
 M9 Title Sheet



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
 ASSEMBLY VARIANT: [No Variations]



|  |  |
|--|--|
| PROJECT TITLE:<br>Low-line 100VAC-127VAC 75W LLC |  |
| DESIGNED FOR:<br>Public Release                  |  |
| FILE NAME:<br>PMP30307_Rev_A_PCB.PcbDoc          |  |
| ENGINEER:<br>R. Scibilia                         | LAYOUT BY:<br>PMP30307_Rev_A           |
| SCALE: 1.00                                      | ALTIUM DESIGNER VERSION:<br>17.1.5.472 |

|  |                                   |                   |                                |
|--|-----------------------------------|-------------------|--------------------------------|
| PCB VIEWED FROM TOP SIDE                 | BOARD #: PMP30522                 | REV: A            | SUN REV: Not In VersionControl |
|  | TID #: N/A                        |                   |                                |
| PLOT NAME = Bottom LayerAssembly Drawing | GENERATED : 11/26/2018 4:28:24 PM | TEXAS INSTRUMENTS |                                |

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