Cascade Radar Host Processor Board

System Description

- **Host Processor**: TDA25X ADS6 Sec
- **CPU**: Dual-Core ARM A15, 1.176 MHz
- **ISP**: 2x C66x, 750 MHz
- **EVE Co-Processor**: 8x EVE Matrix Co-Processor, 532 MHz
- **IVA Co-Processor**: 2x IVA Image Co-Processor, 532 MHz

- **Memory**: 2x 32-bit, 2GB DDR3, 1600 MHz SDRAM (one bank CC-capable)
- **USB**: USB 3.0 Host and USB 2.0 Host
- **Video Out**: 3x HDMI, 1x DisplayPort, 1x Gigabit Ethernet
- **Connectivity**: 1x Gigabit Ethernet, USB 2.0 Serial Port (TI RTOS/Linux Console)

- **Data Storage**: PCIe 2.0 x2 Connector (M-Key), 1x Gigabit NFS Flash, MicroSD Card

- **Mechanical**: 180mm x 140mm - Tier Automotive Rated Board to Board Connectors

- **Software**: TI RTOS with Radar SDK Packages, TI Processor SDK for Linux Distribution with Radar SDK Packages

Cascade Radar Host Processor Board Block Diagram
System 12V DC Power Input

Design Note: System intended to operate with minimum of 12V, 5A (60W) AC to DC converter. Fuse limited to 8A.

Design Note: 12VDC Receptacle Input 5A max, 2.10mm ID (0.083"), 5.50mm OD (0.217")

Design Note: 12VDC Terminal Block Input 12V, 4A max input, 16-30 AWG Wire

Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.

Design Note: LM74610 and CSD18513 N-Channel FET form reverse polarity protection circuit. SMCJ28A TVS diodes perform function of transient over/under-voltage protection. +/-31V

Design Note: System intended to operate with minimum of 12V, 5A (60W) AC to DC converter. Fuse limited to 8A.

Design Note: Ground test points - place throughout system for easy access at major components.
TPS43351 - System 5.0V and System 3.3V Primary Supplies

**System Pushbutton Turn-On/Off**

- **Vin.CONNECT**: VIN, VIN+ and VIN- are connected to the host processor's VIN, VIN+ and VIN- pins.
- **GND**: GND is connected to the host processor's GND pin.
- **RST**: RST is connected to the host processor's RST pin.
- **F**: F is connected to the host processor's F pin.

**Design Note**: VIN, VIN+, and VIN- are connected to the host processor's VIN, VIN+, and VIN- pins. GND is connected to the host processor's GND pin. RST is connected to the host processor's RST pin. F is connected to the host processor's F pin.

**Vin.CONNECT 12V**

- **VIN+**: VIN+ is connected to the host processor's VIN+ pin.
- **VIN-**: VIN- is connected to the host processor's VIN- pin.
- **GND**: GND is connected to the host processor's GND pin.

**Design Note**: VIN+ and VIN- are connected to the host processor's VIN+ and VIN- pins. GND is connected to the host processor's GND pin.

**References**

- Host Processor design specification.
- TPS43351 - System 5.0V and System 3.3V Primary Supplies
- System 12V
- VIN and VREG decoupling must be 
  into low-power mode at light loads.
- Design Note: Select high-current 
  output voltage state to drive KILL pin.
- Design Note: KILL and INT elected 
  together allow for the SYSTEM_3V3 
  output voltage state to drive KILL pin.
- Design Note: INT can also be used as 
  an input power-good monitor that will 
  shut down the board if voltage drops 
  below a predetermined level.
- Design Note: SHDN and SHDN can 
  be used in conjunction with a 
  power-good monitor to provide 
  protection against overvoltage.
- Design Note: SHDN can also be used as 
  a power-good monitor for the 
  SYSTEM_5V output voltage state.
- Design Note: SHDN can also be used as 
  a power-good monitor for the 
  SYSTEM_3V3 output voltage state.
- Design Note: Select high-current 
  output voltage state to drive KILL pin.
References

Based on the TDA2x Evaluation Board Power Architecture
Design Note: 4-way resistor divider. This feeds the enable input of the TPS22965 GPIO4 outputs the "REGEN_3V3_TDA2" signal.

This feeds enable input of the 3.3V TPS22965 GPIO4 outputs the "REGEN_3V3_TDA2" signal.

Design Note: resistor divider. This feeds the enable input of the TPS22965 GPIO4 outputs the "REGEN_3V3_TDA2" signal.

Design Note: resistor divider. This feeds the enable input of the TPS22965 GPIO4 outputs the "REGEN_3V3_TDA2" signal.

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Design Note: resistor divider. This feeds the enable input of the TPS22965 GPIO4 outputs the "REGEN_3V3_TDA2" signal.

TPS659039-Q1 TDA2 PMIC - Digital Power, Clock, Reference and Control

Follow all layout guidelines as presented in Chapter 9 of datasheet.

References TPSS9741L-Q User Guide

TPS659039-Q1 TDA2 PMIC - Digital Power, Clock, Reference and Control

TPS659039-Q1 TDA2 PMIC - Digital Power, Clock, Reference and Control

TPS659039-Q1 TDA2 PMIC - Digital Power, Clock, Reference and Control

TPS659039-Q1 TDA2 PMIC - Digital Power, Clock, Reference and Control
Follow all layout guidelines as presented in Chapter 9 of datasheet.

TDAPMIC_VDDSHV5 is a 3.3V, 300mA LDO not assigned to power anything on the design.

Recommend tying to system 3.3V.

Test points for checking LDO input and output voltage rails. Place near requisite loads.

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TPS659039-Q1 TDA2 PMIC - SMPS Buck Converters: SMPS1, SMPS2, SMPS3, SMPS4 and SMPS5

Follow all layout guidelines as presented in Chapter 9 of datasheet

Sheet ... Route as differential pair.
Test points for checking SMPS output voltage nets. Place near respective loads.

VDD_MPU Remote Feedback

VDD_MPU feedback should be routed to BGA decoupling for best feedback response. Route as differential pair.

VDD_EVE Remote Feedback

VDD_EVE feedback should be routed to BGA decoupling for best feedback response. Route as differential pair.

Test points for checking SMPS output voltage nets. Place near respective loads.
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References

1. TDA2 - Fixed 3.3V I/O Supply
   A load switch is used to allow the primary TDA2 PMIC to control when its 3.3V supply is used, as well as 3.3V I/O supply and pull-ups, which interfaces to the TDA2 device to prevent leakage during power-on/off. Also used to power the Lattice CrossFire FPGA 3.3V I/O Power.

2. SMPS6 - TDA2 VDD_GPU - AVS Supply
   SMPS7 - TDA2 VDD_CORE - AVS Supply
   SMPS8 - TDA2 VDD_IVA - AVS Supply
   SMPS9 - TDA2 VDD1V8 - Fixed 1.8V Supply

3. SMPS6 used to power TDA2 VDD_GPU AVS power net.
   SMPS7 used to power TDA2 VDD_CORE AVS power net.
   SMPS8 used to power TDA2 VDD_IVA AVS power net.
   SMPS9 used to power TDA2 VDD1V8 AVS power net.

4. TPS22965-Q1 Load Switch - TDA2 and System Fixed 3.3V Supply

5. TPS22965-Q1 Load Switch - TDA2 and System Fixed 3.3V Supply
Design Note: Open-drain power good will enable LED indicator.

IN, enable pin toggled using the SYSTEM_5V power net.

Design Note: VOUT = 0.8 × (1 + R1 / R2).

0.8V × (1 + 3.57kohm / 1.69kohm) = 2.489V

Design Note: EN, enable, pin toggled using the SYSTEM_1V8 power net.

Design Note: SS, softstart, pin will determine start-up time. Floating this pin will result in a 200us start-up time. 270pF will result in 0.5ms start-up time.

Design Note: Regulator should be placed near the Ethernet PHY.

Design Note: Voltage = 0.8 × (1 + R1 / R2).

0.8V = (1 + 3.57kohm / 1.69kohm) = 1.068V

Design Note: VOUT = 0.8 × (1 + R1 / R2).

0.8V × (1 + 3.57kohm / 1.69kohm) = 2.489V

Test points for checking LDO input/output voltage nets. Place near respective loads.

TPS74801QRGWRQ1 - Ethernet PHY 1.1V and 2.5V LDO Supplies

TPS74801QRGWRQ1 - Ethernet PHY 1.1V and 2.5V LDO Supplies

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Design Note: VREF power net should be routed as large plane to the entire SDRAM array and TDA2.

Follow TDA2 reference layout example.

VSENSE resistor divider calculation:
\[
\frac{\text{VSENSE}}{\text{VIN}} = \frac{R_1}{R_1 + R_2}
\]

\[
\frac{1}{1+\frac{11\ \text{kohm}}{16\ \text{kohm}}} = 0.8 \quad \text{VSENSE} = 1.35 \text{ V}
\]

EN: enable pin is controlled from the SDRAM array and TDA2.

Follow TDA2 reference layout example.
Follow all layout guidelines as presented in these documents.

**Design Note:** TDA0482 decoupling caps on this page shall placed directly under the BGA, with minimum distance from via to pad.

**Design Note:** TDA0482 decoupling caps on this page shall placed directly under the BGA.

**Design Note:** Select PWR/GND/BSA, parts that are at the center of each of the power net BGA instead to be as a feedback point for the TDA PMIC.

**Design Note:** Select PWR/GND/BSA parts that are at the center of each of the power net BGA instead to be as feedback point for the TDA PMIC.

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**Design Note:** Select PWR/GND/BSA parts that are at the center of each of the power net BGA instead to be as feedback point for the TDA PMIC.
Follow all layout guidelines as presented in these documents.
Design Note: These decoupling caps should be placed directly under the BGA, or close to package (as spacing allows with 0603 package), with minimal distance from via to pad.

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Follow all layout guidelines as presented in these documents.

**References**
- TDA2 Evaluation Board
- Vayu Power Integrity Analysis - (INTERNAL ONLY)
- TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
- TDA2 Evaluation Board - BoM (CDDS INTERNAL ONLY)

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Follow all layout guidelines as presented in these documents.
TDA2 - Clock and Reset Signals

Follow all layout guidelines as presented in these documents.

Design Note: OSC0 used as primary and only output for the core and peripheral PLLs.

Design Note: OSC1 used for MCASP audio sampling - unsupported

Design Note: RTC ISO used for MFCAP audio sampling - unsupported

Design Note: TDA2 - CPU RESET - reset assertion generated from other push buttons or the reset line input signal.

Design Note: Alternatively all of these PORz and ISO signals can be driven directly by the PORz_RSTOUTN pin. The logic is not supported.

TDA2 - CPU and Ethernet PORz

Design Note: OSC0 used as primary and only output for the core and peripheral PLLs.

Design Note: RTC ISO used for MFCAP audio sampling - unsupported

TDA2 - CPU Reset

Design Note: OSC1 used for MCASP audio sampling - unsupported

Design Note: RTC ISO used for MFCAP audio sampling - unsupported

References

Texas Instruments

Contact: Alec Schott

Alec Schott

File: PROC055A_TDA2_Clocks_Reset.SchDoc

Sheet: 1

Sheet Title: TDA2 Evaluation Board - BoM (CDDS NTERAL ONLY)

Project Title: Cascade Radar Host Processor Board

Orderable: TDA2-0106

Assembly Variant: TDA2-0107

Number: 19-09-2019

Size:

REV: 2019

AC14

FD23

AE16

AC16

AD16

AF15

AC15

AF14

AC13

AC12

AC11

AC10

AC9

AC8

AC7

AC6

AC5

AC4

AC3

AC2

AC1

A

B

C

D

E

Follow all layout guidelines as presented in these documents.

TDA2 - Clock and Reset Signals

Follow all layout guidelines as presented in these documents.

Design Note: OSC0 used as primary and only output for the core and peripheral PLLs.

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Design Note: Alternatively all of these PORz and ISO signals can be driven directly by the PORz_RSTOUTN pin. The logic is not supported.

TDA2 - CPU and Ethernet PORz

Design Note: OSC0 used as primary and only output for the core and peripheral PLLs.

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TDA2 - CPU Reset

Design Note: OSC1 used for MCASP audio sampling - unsupported

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References

Texas Instruments

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Alec Schott

File: PROC055A_TDA2_Clocks_Reset.SchDoc

Sheet: 1

Sheet Title: TDA2 Evaluation Board - BoM (CDDS NTERAL ONLY)

Project Title: Cascade Radar Host Processor Board

Orderable: TDA2-0106

Assembly Variant: TDA2-0107

Number: 19-09-2019

Size:
Follow all layout guidelines as presented in these documents.

TPS3808 #1 - VDD MPU, System Supply and Pushbutton POR

TPS3808 #2 - VDD MPU and Pushbutton RESET

References

http://www.ti.com

Cascade Radar Host Processor Board

Project Title:

Designed for:

Public Release

Assembly Variant:

001

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Drawn By:

Engineer:

Alec Schott

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Not in version control

SVN Rev:

PROC055A_TDA2_Reset_Buttons.SchDoc

Sheet Title:

Size:

Mod. Date:

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Drawn By:

Engineer:

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Follow all layout guidelines as presented in these documents.

Design Note: Test points for checking VIN interface. Please place close to TDA2 RX, inline with trace, no stubs.

Design Note: Test points for checking FPGA interface.

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TDA2 - VIN3A and SYSBOOT_MUX

**References**

SN74CBTLV3257 4-bit 2:1 MUX - B1->A
SN74CBTLV3257 4-bit 2:1 MUX - B2->A
SN74CBTLV16210 20-bit 2:1 MUX #2 - B2 -> A1

**Design Note:** MUXing and Delay Matching

The VIN3A signal is multiplexed with the SYSBOOT pin used for selecting the bootmode configuration of the TDA2 device.

This MUX set is used to select between the boot mode operation and functional mode operation.

Because some of the VIN3A signals are multiplexed all of the VIN3A signals must be controlled to ensure best delay matching across the bus. The same delays on the 3257 are used for this purpose. The 3257 and the G125 act as a multiplexer.

**Delay Matching FET Switches**

Follow all layout guidelines as presented in these documents.
DIP Switches and Pullup/Pulldown

Design Note: SYSBOOT[15] - Interface and devices boot list
- See TRM Table 39-2 "Booting Devices Order".
- SYSBOOT[13:10] - GPMC Unused - Tied Low
- SYSBOOT[9:8] - 0b01 -> 20 MHz XO frequency
- SYSBOOT[9:8] - System Clock - SYS_CLK1 Speed Selection
- SYSBOOT[7:6] - 0b00 -> Redundant SBL image offset set to 64KByte
- SYSBOOT[7:6] - Sector offset for the location of the redundant SBL images in QSPI
- SYSBOOT[5:0] - 0b110110 -> selects QSPI_1 bootmode.
- SYSBOOT[5:0] - Interfaces and devices boot list

DIP Switches and Pullup/Pulldown

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- SYSBOOT[5:0] - 0b110110 -> selects QSPI_1 bootmode.
- SYSBOOT[5:0] - Interfaces and devices boot list
TDA2 - VOUT1, EMU and JTAG Top

Design Note: MUX'ing and Delay Matching

The VOUT1 bus is mux'd with the EMU port and many other GPIO signals used throughout the system.

References
Follow all layout guidelines as presented in these documents.
TDA2 - JTAG and Emulation/Trace Bus and Header

TDA2 - JTAG

TDA2 - VOUT1 and EMU Bus
TDA2 - VOUT1, EMU and GPIO MUX

Design Note: MUXing and Delay Matching

The VOUT1 bus is muxed with the EMU port and many other GPIO signals used throughout the system.

**References**

- SN74CBT16212CDGVR
- PROC055A_TDA2_VOUT_JTAG_EMU_MUX.SchDoc
- SN74CBTLV3257 4-bit 2:1 MUX - B2->A

---

**Design Note: MUX Operation**

SYSBOOT_MUX_SELECT = low: EMU Port and GPIO to TDA2s

SYSBOOT_MUX_SELECT = high: VOUT1 Port to ECP5 FPGA.

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**Delay Matching FET Switches**

- PIU59015
- PIU59013
- PIU59014
- PIU59011
- PIU5906
- PIU5905
- PIU5603
- PIU5605
- PIU57024
- PIU57020
- PIU57016
- PIU57011
- PIU5709
- PIU55021
- PIU55013
- PIU55049
- PIU55048
- PIU55052
- PIU55054

**References**

- Design Note: MUXing and Delay Matching
- The VOUT1 bus is muxed with the EMU port and many other GPIO signals used throughout the system.

---

**Design Note: MUX Operation**

SYSBOOT_MUX_SELECT = low: EMU Port and GPIO to TDA2s

SYSBOOT_MUX_SELECT = high: VOUT1 Port to ECP5 FPGA.

---

**Delay Matching FET Switches**

- PIU59015
- PIU59013
- PIU59014
- PIU59011
- PIU5906
- PIU5905
- PIU5603
- PIU5605
- PIU57024
- PIU57020
- PIU57016
- PIU57011
- PIU5709
- PIU55021
- PIU55013
- PIU55049
- PIU55048
- PIU55052
- PIU55054

**References**

- Design Note: MUXing and Delay Matching
- The VOUT1 bus is muxed with the EMU port and many other GPIO signals used throughout the system.
Design Note: All Data, Mask and Data-Strobe signals shall be routed point to point.
Follow all layout guidelines as presented in these documents.

Design Note: All Data, Mask and Data-Strobe signals shall be routed point to point.
TDA2 - VIN1A and VIN2A Interfaces

Design Note: Test points for checking VIN interface. Please place close to TDA2 RX.

Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

Design Note: Remainder of VIN4A interface is MUX'd with GPIO block. See "TDA2 Serial Ports" schematic page.

Design Note: MCASP ports unused and is MUX'd with GPIO block. See "TDA2 Serial Ports" schematic page.

Design Note: FPGA CRESETN moved from D26 to F14.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

TDA2 - SATA/PCIe Controller

References
- TDA2 Evaluation Board
- TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
- TDA2 Evaluation Board
- TDA2 Evaluation Board - BoM (CDDS INTERNAL ONLY)
- TDA2 Evaluation Board - Schematic (CDDS INTERNAL ONLY)
- Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

Design Note:
When an attached host drives VBUS high, this will drive the USB1_VBUS_DET pin high for the TDA2 to detect that the host is initiating the bus.

When an attached host drives VBUS high, this will drive the USB1_VBUS_DET pin high for the TDA2 to detect that the host is initiating the bus.

Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

Design Note: See Vayu EVM notes concerning TRSTN and NTRST resistor population.

Design Note: The TDA_DBG_EMU_RSTN signal provides a method of issuing a CPU reset from the JTAG emulator and CCS session.

This signal is routed to the AND gate circuit input that generates the TDA2 RESETZ signal.

This signal is routed to the AND gate circuit input that generates the TDA2 RESETZ signal.
Follow all layout guidelines as presented in these documents.

**RJ45_SIGNALS**

- RGMII_PHY_TD_A_P
- RGMII_PHY_TD_A_N
- RGMII_PHY_TD_B_P
- RGMII_PHY_TD_B_N
- RGMII_PHY_TD_C_P
- RGMII_PHY_TD_C_N
- RGMII_PHY_TD_D_P
- RGMII_PHY_TD_D_N
- RGMII_PHY_LED_0
- RGMII_PHY_LED_1
- RGMII_PHY_LED_2

**Ethernet TVS ESD Protection**

- UC2
- TC20
- TC21
- TC22
- TC23
- TC24
- TC25

**Ethernet Activity LED2**

- LD2
- LD3

**References**

- RJ45_SIGNALS
- RGMII_PHYSIGNALS PORJ450SIGNALS0RGMII0PHY0LED00 PORJ450SIGNALS0RGMII0PHY0LED01 PORJ450SIGNALS0RGMII0PHY0TD0C0P PORJ450SIGNALS0RGMII0PHY0TD0D0N PORJ450SIGNALS0RGMII0PHY0TD0D0P

Design Note: All NC pins are opposite of the D-side pins.
Follow all layout guidelines as presented in these documents.

**References**

- TDA2 Evaluation Board - Schematic (TIDA-INTERNAL ONLY)
- TDA2 Evaluation Board - BoM (TIDA-INTERNAL ONLY)
- Vayu Power Integrity Analysis - (INTERNAL ONLY)
- TDA2 Evaluation Board - (TIDA-INTERNAL ONLY)

**Design Note:** Follow device datasheet routing recommendations for best USB3.0 signal integrity.

**Design Note:** Signals pass through between the SxA side and Sx side of the device pinout.

**Design Note:** Include grounded screw hole to allow for possible chassis mounting to enclosure.

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**USB3.0 EMI Suppression**

- Class/Name: TDA_USB1_Super_Speed

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**USB ESD Protection**

- Class/Name: TDA_USB1_Super_Speed

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**USB3.0 Type-A Host Connector**

- Class/Name: TDA_USB1_Super_Speed
## HDMI EMI Suppression

### Design Note:
- Follow device datasheet routing recommendations for best HDMI signal integrity.
- Use pull-ups on both the 3.3V and 5.0V side.

### References
- Class Name: TDA_HDMI1
- Class Name: TDA_HDMI1

## Signal Integrity.

### Routing Recommendations for Best HDMI
- Design Note: Follow device datasheet routing recommendations for best HDMI signal integrity.

### HDMI Control and ESD Protection

### Design Note:
- Include grounded traces from every pin for ground plane continuity.
- Place near the device chassis mounting to enclosure.

### HDMI Host Connector

### Design Note:
- Place near the device power pins.
Follow all layout guidelines as presented in these documents.

**Design Note:** Pull-up to set default state of Chip-Select# and Write-Protect# pins.

**Design Note:** RTCLK is a clock delay time feedback path back to the TDA2 QSPI controller. RTCLK should be placed at QSPI pin C termination.

**Design Note:** TDA RSTOUTN pin used to reset the flash memory as well.
TDA2 - m.2 PCIE/SATA Connector & EEPROM

m.2 Socket 3 (M-K eyed) PCIE SSD Connector

The PCIe SSD drives do need to be of type: M.2 2280 (22mm x 80mm) in order to be fastened down with the included drill holes. A single sided SSD card would be best desired so that there is max clearance for components located on PCIe. Due to height of some components height of SSD should not exceed a bottom thickness of 1.35mm. With a total thickness (height) of 2.45mm.

Recommended device:
Name: NVMe SSD 960 Pro M.2 512GB
Part #: M2VW512HM4Q

Design Note: DEVICE IS NOT WRITE PROTECTED SINCE PRINT IS PULLED DOWN.

Design Note: m.2 socket layout should include compatibility for m.2 card types:
- 2260
- 2280
PCB will accept only single-sided 2 SSD cards due to height restrictions.

Follow all layout guidelines as presented in these documents.

Texas Instruments
Follow all layout guidelines as presented in these documents.

MicroSD ESD Protection

MicroSD Card Connector
Follow all layout guidelines as presented in these documents.

Design Note: Interface provides 12V and up to 2A.

Design Note: Interface brings out the VOUT1 interface, I2C5 and two I2C GPIO expander pins to allow for interfacing to a separate Lattice ECP5 FPGA card which will perform VOUT to 10GBase-KR bridging.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
FPGA VCC, VCCAUX 2.5V and VCCGPLL Decoupling
Follow all layout guidelines as presented in these documents.

Design Note: FPGA SPI interface run in SLAVE mode or MASTER mode. Pin names indicate MASTER mode operation.

NOR and NAND functionality is assigned in SLAVE mode, allowing for SPI programming from external SW. Use XIO-M Programming Cable or TDI2 boot processor.

Design Note: Flash WP and HOLD disabled.

Design Note: After internal POR circuit indicates power down or EM/RESET low to high transition will start NVCM boot sequence.

Design Note: After internal POR circuit indicates power down or EM/RESET low to high transition will start NVCM boot sequence.

Design Note: Flash WP and HOLD disabled.
Follow all layout guidelines as presented in these documents.
Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #1 CSI2.0 Interface, FPGA1/4 Power Supplies

Follow all layout guidelines as presented in these documents.

FPGA VCC, VCCAUX 2.5V and VCCGPLL Decoupling

FPGA VCCA_PHY[1:0], VCCPLL_DPHY[1:0] and DPHY[1:0]

FPGA VCC, VCCAUX 2.5V and VCCGPLL
Design Note: FPGA SPI interface runs in SLAVE mode or MASTER mode. Pre-names indicate MASTER mode operation.

NOR and MSD functionality are assigned in SLAVE mode, allowing for SPI programming from a TI SPI or USB Programming Cable or TDA2 host processor.

Design Note: After internal POR circuit indicates good power, FPGA resets low to high transition will start NVC M boot sequence.

Design Note: After internal POR circuit indicates good power, FPGA resets low to high transition will start NVC M boot sequence.

Design Note: Flash WP and HOLD disabled

Design Note: Running QSPI capable NOR flash in x1 SPI (XIO-SPI) mode.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Design Note: FROM AWR devices

Design Note: TO AWR devices

*Design Note: The AWR RF board provides the 3.3V I/O PMIC as a "power good" signal

Follow all layout guidelines as presented in these documents.

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Design Note: All screw holes should be connected to PCB GND to allow for possible chassis mounting to enclosure.
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