System 12VDC Power Input

Design Note: System intended to operate with minimum of 12V, 5A (60W) AC to DC converter. Fuse limited to 8A.

Design Note: 12VDC Receptacle Input 12V, 8A max input, 16-30 AWG Wire

Design Note: 12VDC Receptacle Input 5A max, 2.10mm ID (0.08"), 5.59mm OD (0.217")

Design Note: Ground test points - place throughout system for easy access at major components.

Design Note: LMF74610 and CSD18513 N-Channel FET form reverse polarity protection circuit.
SMCJ28A TVS diodes perform function of transient over-under-voltage protection, +/-31V

Design Note: System 12VDC Power Input

Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.
**TPS43351 - System 5.0V and System 3.3V Primary Supplies**

**System Pushbutton Turn-On/Off**
- **Design Note:** The **VIN** (5.0V) & **VOUT** (3.3V) power supplies are enabled when power is applied to the **1V** connector input.

**Buck-A: System 3.3V Power Supply**
- **Design Note:** Select high current output devices within the 3.3V power plane as needed.

**Buck-B: System 5.0V Power Supply**
- **Design Note:** Select high current output devices within the 5.0V power plane as needed.

**Route Feedback**
- **Reference the calculations for buck feedback and PGOOD to GND plane - lowest possible inductance.**

**System Design Considerations**
- **References:**
  - *Follow all layout guidelines as presented in Chapter 10 of datasheet*
  - *Note: All IC pins with lowest inductance paths placed as close as possible to regulator and 5V connector input.
  - *RT: grounded, sets 400kHz buck control switching frequency.*
  - *ENA/B internal pull-up to enable buck shut-down the board if voltage drops below 25V.*
  - *NC: Circuit is not connected.*

**NOTES:**
- *For optimum performance, the design should be submitted to Texas Instruments for evaluation. The final design will be determined by Texas Instruments and the customer is responsible for its production capability.*
References

Based on the TDA2x Evaluation Board Power Architecture

TPS659039-Q1 TDA2 PMIC - Top Level Schematic

PMIC digital power control, bootstrapping, etc.

PMIC LDO array input and outputs

PMIC first page of buck-converters

PMIC second page of buck-converters

TPS43351 PGOOD
TDA_ON_OFF
TDA_RSTOUTN

TDAPMIC_GPIO4
TDAPMIC_GPIO6
TDAPMIC_INT
TDAPMIC_RESET_OUT
I2C1

POWER_TDA2_PMIC_LDO
PROC055B_Power_TDA2_PMIC_LDO.SchDoc

POWER_TDA2_PMIC_SMPS1
PROC055B_Power_TDA2_PMIC_SMPS1.SchDoc

POWER_TDA2_PMIC_SMPS2
PROC055B_Power_TDA2_PMIC_SMPS2.SchDoc

POWER_TDA2_PMIC_CONTROL_CLOCKS
PROC055B_Power_TDA2_PMIC_Control_Clocks.SchDoc

TPS659039-Q1 TDA2 PMIC - Top Level
PMIC digital power, control, bootstrapping... etc.
PMIC LDO array input and outputs
PMIC first page of buck-converters
PMIC second page of buck-converters
Follow all layout guidelines as presented in Chapter 9 of datasheet.
TPS659039-Q1 TDA2 PMIC - LDO Input and LDO Output

LDOSUSB - TDA2VUSB3V3 - Fixed 3.3V USB PHY Supply
LDOSVRTC - TDA2VDDARTC1V8 - Fixed 1.8V RTC Supply
LDOSVANA - UNASSIGNED
LDOS1 - TDA2VDDSHV5 - Fixed 3.3V IO Supply
LDOS2 - TDA2VDDSHV8V - Fixed 3.3V IO Supply
LDOS3 - TDA2VDDAPHY1V8 - Fixed 1.8V USB PHY Supply
LDOS9 - TDA2TDA2VDDRTC1V05 - Fixed 1.05V RTC Supply
LDOLN - TDA2VDDAPLL1V8 - Fixed 1.8V PLL Supply

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Follow all layout guidelines as presented in Chapter 9 of datasheet.

SMPS[3:1] - TDA2 VDD_MPU - AVS Supply
SMPS[5:4] - TDA2 VDD_EVE - AVS Supply

TPS659039-Q1 TDA2 PMIC - SMPS Buck Converters: SMPS1, SMPS2, SMPS3, SMPS4 and SMPS5

VDD_MPU Remote Feedback

VDD_EVE Feedback should be routed to BGA decoupling for best feedback response. Route as differential pair.

Test points for checking SMPS output

VDD_MPU feedback should be routed to BGA decoupling for best feedback response. Route as differential pair.

Test points for checking SMPS output

Follow all layout guidelines as presented in Chapter 9 of datasheet.
TPS659039-Q1 TDA 2 PMIC - SMPS Buck Converters: SMPS6, SMPS7, SMPS9 and SMPS9 and TDA/System 3.3V Switch

SMPS6 - TDA2 VDD_GPU - AVS Supply
SMPS7 - TDA2 VDD_CORE - AVS Supply
SMPS8 - TDA2 VDD_IVA - AVS Supply
SMPS9 - TDA2 VDD1V8 - Fixed 1.8V Supply

SMPS used to power TDA2 VDD_CORE 1.8V power net.

SMPS used to power TDA2 VDD_IVA 1.8V power net.

Also used to power the Lattice CrossFire FPGA 3.3V I/O Power

Test point for checking SMPS output voltage now. Please note respective loads

Reference information should be considered to ensure the accuracy of components in the specification of any power management system. Texas Instruments assumes no responsibility for any inaccuracies.

Follow all layout guidelines as presented in datasheets
Follow all layout guidelines as presented in the device datasheet.
Follow all layout guidelines as presented in the device datasheet.

- EN enable pin is controlled from the TDA2 PMIC GPIO6 output.
- CCU2 - 5K selects a max frequency
- CCUT- 10K selects a max soft-start
- RT/CLK: 86.6K selects a frequency

SDRAM array, routed as large plane to the entire
SDRAM array and TDA2.

Follow TDA2 reference layout example.

Design Note: VREF power net should be routed as large plane to the entire
SDRAM array and TDA2.

Follow TDA2 reference layout example.
Texas Instruments makes no representations or warranties with respect to the accuracy or completeness of the content contained in this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Users are cautioned to verify the parameters and requirements relevant to their application.

The design shown in this schematic is a representation of the TDA2. Actual implementation may vary due to design constraints, fabrication processes, and other factors. The design may not meet all specifications, may not be suitable for all applications, and may not be appropriate for all purposes. Texas Instruments and/or its subsidiaries do not warrant that this design will meet specifications, will be suitable for your application, or will operate in an implementation. Texas Instruments and/or its subsidiaries do not warrant that the design is production-worthy. You should completely validate and test your design implementation to confirm the system functionality for your specific application.
Follow all layout guidelines as presented in these documents.

**Design Note:** Those 0402 decoupling capacitors on this page shall be placed as close as possible to the BGA, with minimal distance between to pads.

**Design Note:** Those larger decoupling and bypass capacitors on this page shall be placed as close as possible to the BGA.

**Design Note:** Apply PW/SOS/SGS BGA pads that are in the center of each of the ground net BGA sections to act as a feedback point for the TDA PMIC.

TDA - Core Power Nets and Decoupling

TDA2 - Reserved Pins
Follow all layout guidelines as presented in these documents.

Design Note: These decoupling caps should be placed directly under the BGA, or close to package (as spacing allows with 0603 package), with minimal distance from via to pad.
TDA2 - Peripheral 3.3V and 1.8V Power Nets and Decoupling

---

Peripheral 3.3V Power Nets and Decoupling

---

Peripheral 1.8V Power Nets and Decoupling

---

M L B P Power/Clocking
TDA2 - Internal LDO External Output Capacitors

Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

References
- TDA2 - Ground Return
- TDA2 - Ground Return - Schematic (INTERNAL ONLY)
- Vayu Power Integrity Analysis - (INTERNAL ONLY)
- TDA2 Evaluation Board - BoM (INTERNAL ONLY)
- TDA2 Evaluation Board - Schematic (INTERNAL ONLY)

Notes:
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- Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your specific application.
Follow all layout guidelines as presented in these documents.

Design Note: OSC0 used to drive the PMIC RESET_OUT pin. The logic is only needed if a push-button POR=false cycle is required.

Design Note: Alternatively all of these PORs and TDO signals can be driven directly by the PMIC TDO\_RESET\_OUT pin. The logic is only

Design Note: CBO\_POR used with MCF5299 radio sampling - untested

Design Note: CBO\_POR used with MCF5299 radio sampling - untested

Design Note: CBO\_POR used with MCF5299 radio sampling - untested

Design Note: CBO\_POR used with MCF5299 radio sampling - untested

Design Note: CBO\_POR used with MCF5299 radio sampling - untested

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Design Note: CBO\_POR used with MCF5299 radio sampling - untested

Design Note: CBO\_POR used with MCF5299 radio sampling - untested

Design Note: CBO\_POR used with MCF5299 radio sampling - untested
References
- TDA Evaluation Board
- TDA Evaluation Board - Schematic (INTERNAL ONLY)
- Vayu Power Integrity Analysis - (INTERNAL ONLY)

Follow all layout guidelines as presented in these documents.

TPS3808 #1 - Generates a reset based on the status of the system level 5.0V and 3.3V supply power good signal TPS43351_PGOOD and the status of the TDA_VDD_MPU SMPS rail. Pushbutton used to pull the MR pin low for PORz toggle.

TPS3808 #2 - Generates a reset based on the status of the TDA_VDD_MPU SMPS rail. Pushbutton used to pull the MR pin low for PORz toggle.
References
- SN74LVC1G125 Single Bus Buffer Gate
- COTP186
- TDA_VIN3A_CLK0
- P1R51901
- TDA_VIN3A_D[23..0]
- TDA_SYSBOOT[15..0]
- R514
- 0.1μF
- SN74LVC1G125DBVT
- C631

Follow all layout guidelines as presented in these documents.

Design Note: MUXing and Delay Matching
The VIN3A data path is multiplexed with the SYSBOOT pins used for selecting the boot mode configuration of the TDA2.
This MUX set is used to select between the boot mode operation and functional mode operation.

Design Note: MUXing and Delay Matching
The VIN3A/SYSBOOT signals to TDA2 - VIN3A and SYSBOOT MUX. The VIN3A signals from FPGA #3 run through a similar MUX architecture to route these delay matching across the SON.

Design Note: MUX/Selection
The extra channels on the 16212 are used to route the VIN3A signals. The TDA2 - VIN3A and SYSBOOT MUX.

The VIN3A/SYSBOOT signals from FPGA #3.

SYSBOOT state from boot selection switches.

VIN3A signals from FPGA #3.

SYSBOOT state from boot selection switches.

VIN3A signals from FPGA #3.
DIP Switches and Pullup/Pulldown

Design Note: SYSBOOT[15] - Interfaces and devices boot list
- See TRM Table 29-9: "Booting Devices Order"
- SYSBOOT[15]: 0b01010101 selects QSPI bootmode.

Design Note: SYSBOOT[14] - Tied low per datasheet.
- SYSBOOT[7:6] - Sector offset for the location of the redundant SBL images in QSPI.
- SYSBOOT[9:8] - Selects the SYS_CLK1 clock speed.
- SYSBOOT[5:0] - Selects interfaces for the booting list
- SYSBOOT[15..0] pins latched on PORz de-assertion.

Design Note: SYSBOOT[15] - Must be pulled to VDD for proper device operation.
- SYSBOOT[14] - Must be pulled to VSS for proper device operation (SR2.0).

Design Note: SYSBOOT[13] - Select System Clock - SYS_CLK1 Speed Selector
- SYSBOOT[13]: 0b001 -> 20 MHz XO frequency
- SYSBOOT[13]: 0b011 -> 40 MHz XO frequency
- SYSBOOT[13]: 0b101 -> 60 MHz XO frequency
- SYSBOOT[13]: 0b111 -> 80 MHz XO frequency

Design Note: SYSBOOT[12] - GPMC VSS - GPMC VDD
- SYSBOOT[12]: 0b001 -> GPMC VSS
- SYSBOOT[12]: 0b000 -> GPMC VDD

Design Note: SYSBOOT[10] - TIE high
- SYSBOOT[10]: 0b001 -> TIE high
- SYSBOOT[10]: 0b000 -> TIE low

Design Note: SYSBOOT[9] - TIE low
- SYSBOOT[9]: 0b001 -> TIE low
- SYSBOOT[9]: 0b000 -> TIE high

Design Note: SYSBOOT[8] - TIE low
- SYSBOOT[8]: 0b001 -> TIE low
- SYSBOOT[8]: 0b000 -> TIE high

Design Note: SYSBOOT[7] - Select GPMC interface
- SYSBOOT[7]: 0b001 -> GPMC VDD
- SYSBOOT[7]: 0b000 -> GPMC VSS

Design Note: SYSBOOT[5] - Pullup/Pulldown
- SYSBOOT[5]: 0b001 -> Software re-configuration of pull resistors is allowed.
- SYSBOOT[5]: 0b000 -> Software re-configuration of pull resistors is not allowed.
References

Follow all layout guidelines as presented in these documents.

Design Note: MUX'ing and Delay Matching

The VOUT1 bus is mux'd with the EMU port and many other GPIO signals used throughout the system.

References

Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

References
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TDA - J TAG and Emulation/Trace Bus and Header

TDA - J TAG

TDA - VOUT1 and EMU Bus
References

Design Notes: MUXing and Delay Matching

The VOUT1 bus is used with the EMU port and many other GPIO signals used throughout the system.

TDA2 - VOUT1, EMU and GPIO MUX

SELECTN Generation

Delay Matching FET Switches
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

Design Note: All Data, Mask and Data-Strobe signals shall be routed point to point.

Design Note: All Clock, Address, Command and Control signals to be routed as DDR3L "Fly-By" signals. Source and return AC termination to be placed at 50% "Fly-By" routing.
Follow all layout guidelines as presented in these documents.

Design Note: Test points for checking VIN interface. Please place close to TDA2 RX.

Design Note: Test points for checking VIN interface. Please place close to TDA2 RX.
Follow all layout guidelines as presented in these documents.

**TDA2 - VIN1A and VIN2A Interfaces**

**Design Note:** MCASP ports unused and not connected. See "TDA2 Serial Ports" schematic page.

**Design Note:** FPGA CRESETN instead of DD to 014

**Design Note:** Test points for checking VIN interface. Please place close to TDA2 RX.

**Class Name:** VIN1A

**Class Name:** VIN2A
Follow all layout guidelines as presented in these documents.
I2C GPIO Expander

Class Name: VIN4A

Design Note: FROM AWR devices

UART1 - AWR\[4:1\] MUX

Class Name: TDA_UART1

Design Note: TO TDA2 receiver

References

Class Name: TDA_SPI1

Design Note: TO AWR devices

NOTES

- Drawn By: Alec Schott
- © Texas Instruments 2023
- Mod. Date: 13.09.2022
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

TDA2 - USB3 Interface

TDA2 - USB3.0 Super-Speed Interface

USB3 Device Mode VBUS Detect

USB3 Host Mode VBUS Generation

Design Note:

When an attached host drives VBUS high, this will drive the USB1_VBUS=0.5V pin high. This may be desirable for two reasons:

1. In some circumstances, driving VBUS high may be necessary for compatibility with certain USB-OTG hosts.
2. Driving VBUS high may help to prevent noise on the VBUS line, which can improve the overall USB performance.

Design Notes:

1. TDA_USB1_DRV_VBUS on the host is driven high to enable the TPS2077 power switch enabling the 5V VBUS for a connected device.

2. The TDA_USB1_DRV_VBUS pin on the host is driven high to enable the TPS2077 power switch providing 5V VBUS for a connected device.

Notice that this design will meet the specifications, and will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production-worthy. You should completely validate and test your design implementation to confirm the system functionality for your specific application.

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Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
TDA2 - J TAG and EMU Debug Header

Follow all layout guidelines as presented in these documents.

Design Note: The TDA_DBG_EMU_RSTN signal provides a method of issuing a CPU reset from the JTAG emulator and CCS.

This signal is routed to the AND gate circuit output that generates the TDA2 RESETZ signal.

Design Note: See Vayu EVM notes concerning TRSTN and NTRST resistor population.
TDA2 - RGMII 1Gigabit Ethernet RJ45 Magnetics

Follow all layout guidelines as presented in these documents.

Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.

Design Note: TVS ESD protection placed in-line with PHY signals - no NC. NC pins are opposite the D出生于 pins.

Design Note: LED activity indicator for possible chassis mounting in enclosures.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.

Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.
Follow all layout guidelines as presented in these documents.

Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.

Design Note: Follow device datasheet routing recommendations for best HDMI signal integrity.

Design Note: Follow device datasheet routing recommendations for best HDMI signal integrity.

Design Note: Follow device datasheet routing recommendations for best HDMI signal integrity.

Design Note: Place near the device power pins.

Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.

Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.

Design Note: Include grounded screw hole to allow for possible chassis mounting to enclosure.
Follow all layout guidelines as presented in these documents.

Design Note: RTCLK is a clock delay time feedback path back to the TDA2 QSPI controller. RTCLK should be placed at QSPI pin C termination.

Design Note: TDA_RSTOUTN pin used to reset the flash memory as well.

Design Note: Pull-up to set default state of Chip-Select# and Write-Protect# pins.
PCIE SSD drives note

The PCIe SSD drive needed is m.2 Socket 3 (Mechanical Key M).
Dimensions of SSD need to be of Type: 2280 (22mm x 89mm) in order to be flooded down with the included drill holes.
A single sided SSD card would be best desired so that there is max clearance for components located on PCB.
Due to height of some components height of SSD should not exceed a bottom thickness of 1.35mm. With a total thickness height of 2.45mm.
Recommended device:
Name: Wintec SSD 960 Pro M.2 512GB
Part: MZVKNF128HMJP
Follow all layout guidelines as presented in these documents.

MicroSD ESD Protection

MicroSD Card Connector

Design Note: ESD protection routed in line with the MMC signals.

TDA_MMC1, SPI2 and SPI4 and SDCard Connector

References

TDA2 - MMC1, SPI2 and SPI4 and SDCard Connector

TDA2 Evaluation Board - Design Note: ESD protection routed in-line with the MMC signals.
TDA2 - VOUT1 Lattice ECP5 FPGA Prototyping Connector

Follow all layout guidelines as presented in these documents.

Design Note: Interface provides 12V and up to 2A.

Design Note: Interface bridges the VOUT1 interface, DC5 and two 24GHz/5GHz radar plans to allow for interfacing to a separate Lattice ECP5 FPGA and relays will pump VOUT to VOUT0 for 6.3V/6.4V.

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Follow all layout guidelines as presented in these documents.
Lattice L1F6000 FPGA CSI2.0 to VIN Bridge - FPGA #1 CSI2.0 Interface, FPGA1/4 Power Supplies

Follow all layout guidelines as presented in these documents.

FPGA VCC, VCCAUX 2.5V and VCCGPLL Decoupling

FPGA VCCA_PHY[0:1], VCCPLL_DPHY[0:1] and DPHY[0:1]

FPGA VCC, VCCAUX 2.5V and VCCGPLL

FPGA1/4 VCCAUX 2.5V Supply

FPGA1/4 VCC 1.2V Supply
Follow all layout guidelines as presented in these documents.

Lattice LIFM D600 FPGA CSI 2.0 to VIN Bridge - FPGA #1
FPGA VIN, SPI and Configuration Interface

Design Note: FPGA SPI interface runs in Slave mode or Master mode. Pin-names indicate Master mode operation.
MISO and MORN functionality swapped in Slave mode, allowing for SPI programming from Lattice HW-USBN-2B Programming Cable or TDA1 host processor.

Design Note: After internal POR circuit indication, good practice is to ensure that high resistance will start NVCM boot sequence.

Design Note: Running QSPI capable NOR flash in xSPI(ND-SPI) mode

Follow all layout guidelines as presented in these documents.

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References

Follow all layout guidelines as presented in these documents.

Design Note: CRESETN broadcast from TDA2 to all FPGA and all FPGA connectors.
Follow all layout guidelines as presented in these documents.
Lattice L1FM D6000 FPGA CSI2.0 to VIN Bridge - FPGA #2

FPGA VIN, SPI and Configuration Interface

- Design Note: FPGA SPI interface runs in SLAVE mode as MASTER mode. Parameters indicate MASTER mode operation.
- MSIO and MISO functionality swapped in SLAVE mode, allowing for SPI programming from Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge.

FPGA VIN Interface

- Design Note: After internal POR circuit resets, good power on CRESETN will start SDIO host sequence.
- Design Note: After internal POR circuit resets, good power on CRESETN will start SDIO host sequence.

FPGA SPI/Config Interface

- Design Note: Flash WP and HOLD disabled.
- Design Note: Running QSPI capable NOR flash in SLI SPI(I0)-SPI mode.

FPGA and NOR Flash Programming Header

- Design Note: FPGA SPI interface runs in SLAVE mode as MASTER mode. Parameters indicate MASTER mode operation.
- MSIO and MISO functionality swapped in SLAVE mode, allowing for SPI programming from Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge.

TDA2/Programmer SPI CS Jumper

- Design Note: After internal POR circuit resets, good power on CRESETN will start SDIO host sequence.
- Design Note: After internal POR circuit resets, good power on CRESETN will start SDIO host sequence.

References

- Lattice LIFMD6000 FPGA CSI2.0 to VIN Bridge - FPGA #2
- Texas Instruments Lattice CrossFire FPGA Configuration Guide

Disclaimer

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Design Note: Running QSPI capable NOR flash in SLI SPI(I0)-SPI mode.

Design Note: Flash WP and HOLD disabled.

Design Note: FPGA SPI interface runs in SLAVE mode as MASTER mode. Parameters indicate MASTER mode operation.

Design Note: After internal POR circuit resets, good power on CRESETN will start SDIO host sequence.

Design Note: After internal POR circuit resets, good power on CRESETN will start SDIO host sequence.

Design Note: After internal POR circuit resets, good power on CRESETN will start SDIO host sequence.

Design Note: After internal POR circuit resets, good power on CRESETN will start SDIO host sequence.
Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Lattice LIFMD 6000 FPGA CSI 2.0 to VIN Bridge - FPGA #3
FPGA VIN, SPI and Configuration Interface

Follow all layout guidelines as presented in these documents.

Design Note: FPGA SPI/Config Interface

Design Note: FPGA SPI Interface uses the XIO-SPI interface. The names indicate the master mode operation.

MISO and MOSI functionality swapped in the XIO-SPI mode allowing for SPI programming from Lattice SN USB-28 Programming Cable or EDS file present.

Design Note: After internal POR circuit is completed, good power is detected the VIN20 pin will drive always will start NVCM boot sequence.

Design Note: Running QSPI capable NOR flash in x1 SPI (NOR-MSPI) mode.

Design Note: Flash WP and HOLD disabled.

References

Follow all layout guidelines as presented in these documents.

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Follow all layout guidelines as presented in these documents.
Follow all layout guidelines as presented in these documents.
Lattice LIFM D600 FPGA CSI2.0 to VIN Bridge - FPGA #4
FPGA VIN, SPI and Configuration Interface

Design Note: FPGA SPI interface ran in SLAV mode of MASTER mode. The names indicate MASTER mode operation. MISO and MOSI functionality swapped in SLAV mode allowing for SPI programming from Lattice MH-USBN-2B Programming Cable or TDS-USB host-present.

Design Note: Flash WP and HOLD disabled.

Design Note: After internal POR circuit indicates good power or C126/0 is high transition will start NVCM boot sequence.

Design Note: After internal POR circuit indicates good power or C126/0 is high transition will start NVCM boot sequence.

Design Note: Running SPI capable NOR Flash in x1 SPI (XIO-SPI) mode.
TDA2 AWR RF Board Connector 1 - Power, Control and Data Interfaces

Mates to AWR RF Board P1
Follow all layout guidelines as presented in these documents.

Design Note: The AWR RF board provides the 3.3V I/O PMIC 3.3V as a "power good" signal.

Design Note: TDA I2C5 interfaces to secondary AWR PMIC I2C port and RF board temperature sensors.

Design Note - TDA I2C5 interface to secondary AWR PMIC I2C port and RF board temperature sensors.

Design Note: TDA GPIO2[10:13] interface to secondary AWR4_RESETN and TDA2_RF.

Design Note: TO AWR devices
Design Note: All screw-holes should be connected to PCB GND to allow for possible-chassis mounting to enclosure.

Assembly Note ZZ2
These assemblies are ESD sensitive. ESD precautions shall be observed.

Assembly Note ZZ3
These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.

Assembly Note ZZ4
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Assembly Note ZZ5
INDICATION FOR COMPONENTS D* (WITH 2 PINS) ARE GIVEN AT THEIR CATHODE SIDE.

Assembly Note ZZ6
MP1 must be soldered down to the "Top Layer" of PCB.

Assembly Note ZZ7
Refer to Test Procedure Document for installing uSD, H9, and SSD Drive

Design Note: All screw-holes should be connected to PCB GND to allow for possible-chassis mounting to enclosure.
# Bill of Materials

## Bill of Materials For Variant [001] of Project [PROC055B_Cascade_Radar_Host.PrjPcb]

(No PCB Document Selected)

### Approved Notes

- M8AIG
- ABM3B
- M8AIG
- N
- DSG0008B
- TPS22965DSG
- CMP-0073676-2
- U35
- PW0024A_N
- 12BIN_FBGA
- DSG0008B
- N
- RTE0016F
- SOP-0603_HV
- SRP4012TA
- IND_TAIYO-A
- 516121
- R1000
- JAE_SM3ZS
- Hirose_FX23-0402S
- 0201L Capacitor
- 5NNNC_0402
- 0805L
- 0402S
- PCA9306IDCUR
- DCKR
- TI-TPD2E001-
- TPS62262DRV6-
- 15
- MOSFET_N_D5
- BDN10-
- D-RA-L-TR
- os-4Shld
- 1001
- NNC
- BB221
- C0603C331K5R
- GRM033C71C1
- CC0402KRX7R8
- 75KE11D
- 06KE11L
- 05KA03K
- 4KA57D
- CMP-0005313-2
- U70
- CMP-0048585-2
- U60, U61
- CMP-0051684-2
- U56, U63
- Single Inverter
- DCK0005A, LARGE T&R 2
- CMP-0051712-2
- U53
- CMP-0051588-2
- U31
- CMP-0002300-2
- S1, S2, S3
- 0000755-1
- CMP-0082233-1
- Q6
- CMP-0008262-2
- C164, C165, C466
- CMP-0006623-
- R218, R219, R220, R221, R222, R223,
- R85, R86, R87, R89, R90, R91, R92, R93,
- Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14,
- C171, C172, C173, C185, C186, C187,
- C108, C111, C114, C117, C120, C123,
- C448, C451, C452, C453, C454, C455,
- C342, C343, C344, C345, C346, C364,
- C210, C211, C212, C213, C214, C215,
- C158, C178, C193, C198, C202, C203,
- C1, C2, C137, C168, C170, C184, C624,
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