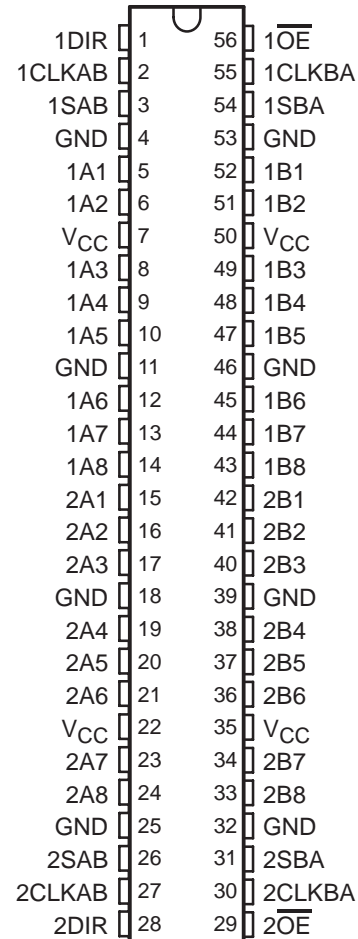- **Members of the Texas Instruments Widebus™ Family**

- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**

- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**

- **Support Unregulated Battery Operation Down to 2.7 V**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**

- **I_{off} and Power-Up 3-State Support Hot Insertion**

- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**

- **Flowthrough Architecture Optimizes PCB Layout**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

SN54LVT16646 . . . WD PACKAGE
SN74LVT16646 . . . DGG OR DL PACKAGE
(TOP VIEW)

Pin			Pin	
1DIR	1		56	1$\overline{OE}$
1CLKAB	2		55	1CLKBA
1SAB	3		54	1SBA
GND	4		53	GND
1A1	5		52	1B1
1A2	6		51	1B2
V_{CC}	7		50	V_{CC}
1A3	8		49	1B3
1A4	9		48	1B4
1A5	10		47	1B5
GND	11		46	GND
1A6	12		45	1B6
1A7	13		44	1B7
1A8	14		43	1B8
2A1	15		42	2B1
2A2	16		41	2B2
2A3	17		40	2B3
GND	18		39	GND
2A4	19		38	2B4
2A5	20		37	2B5
2A6	21		36	2B6
V_{CC}	22		35	V_{CC}
2A7	23		34	2B7
2A8	24		33	2B8
GND	25		32	GND
2SAB	26		31	2SBA
2CLKAB	27		30	2CLKBA
2DIR	28		29	2$\overline{OE}$

description/ordering information

The 'LVT16646 devices are 16-bit bus transceivers and registers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16646 devices.

ORDERING INFORMATION

T_A	PACKAGE†			ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube		SN74LVT16646DL	LVT16646
		Tape and reel		SN74LVT16646DLR	
	TSSOP – DGG	Tape and reel		SN74LVT16646DGGR	LVT16646
−55°C to 125°C	CFP – WD	Tube		SNJ54LVT16646WD	SNJ54LVT16646WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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description/ordering information (continued)

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified[†]	Store A, B unspecified[†]
X	X	X	↑	X	X	Unspecified[†]	Input	Store B, A unspecified[†]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at $\overline{OE}$ and DIR. Data input functions always are enabled; i.e., data at the bus pins are stored on every low-to-high transition of the clock inputs.

OE	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A

OE	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B

OE	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

OE	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B
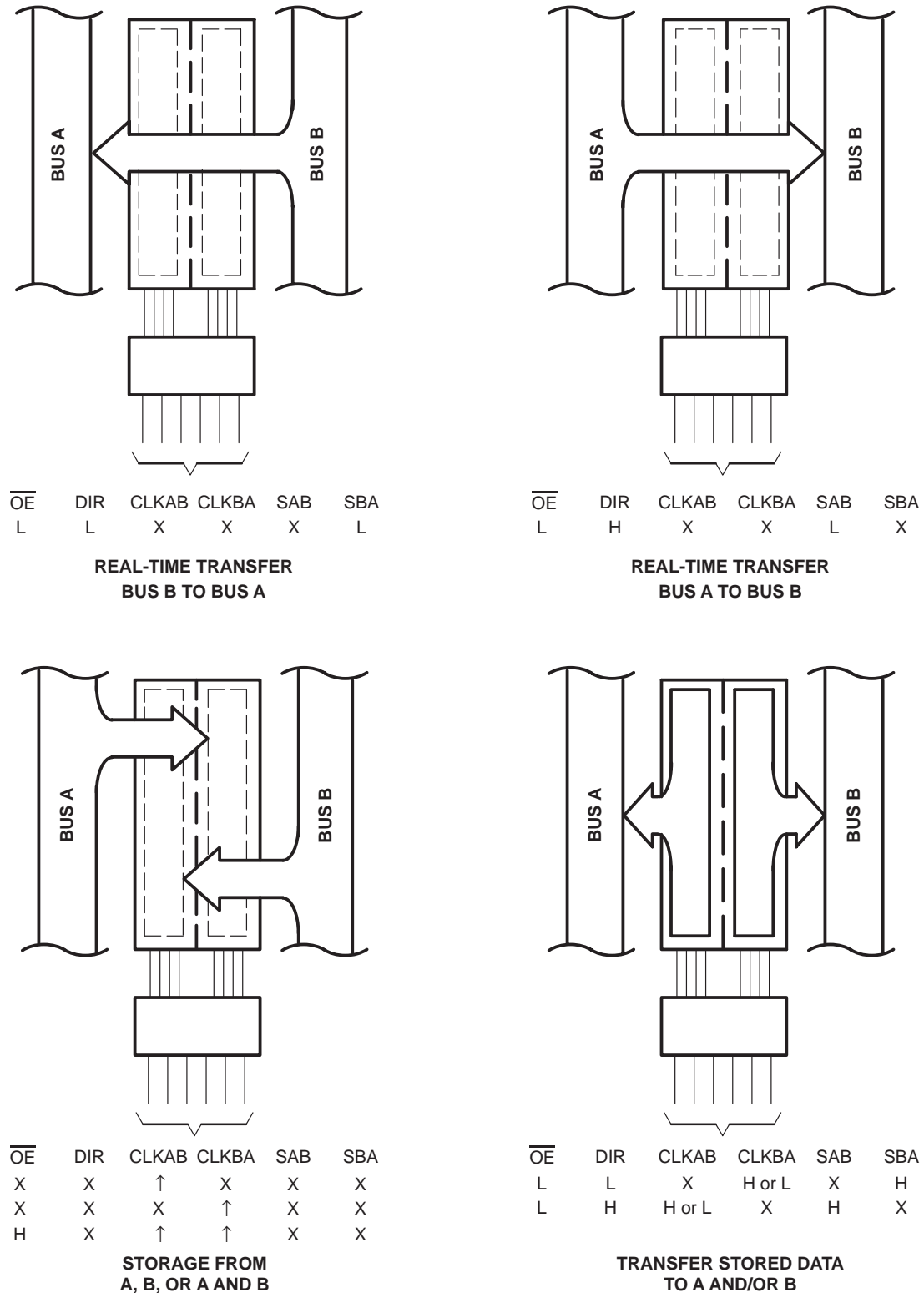
Figure 1. Bus-Management Functions

3

logic diagram (positive logic)
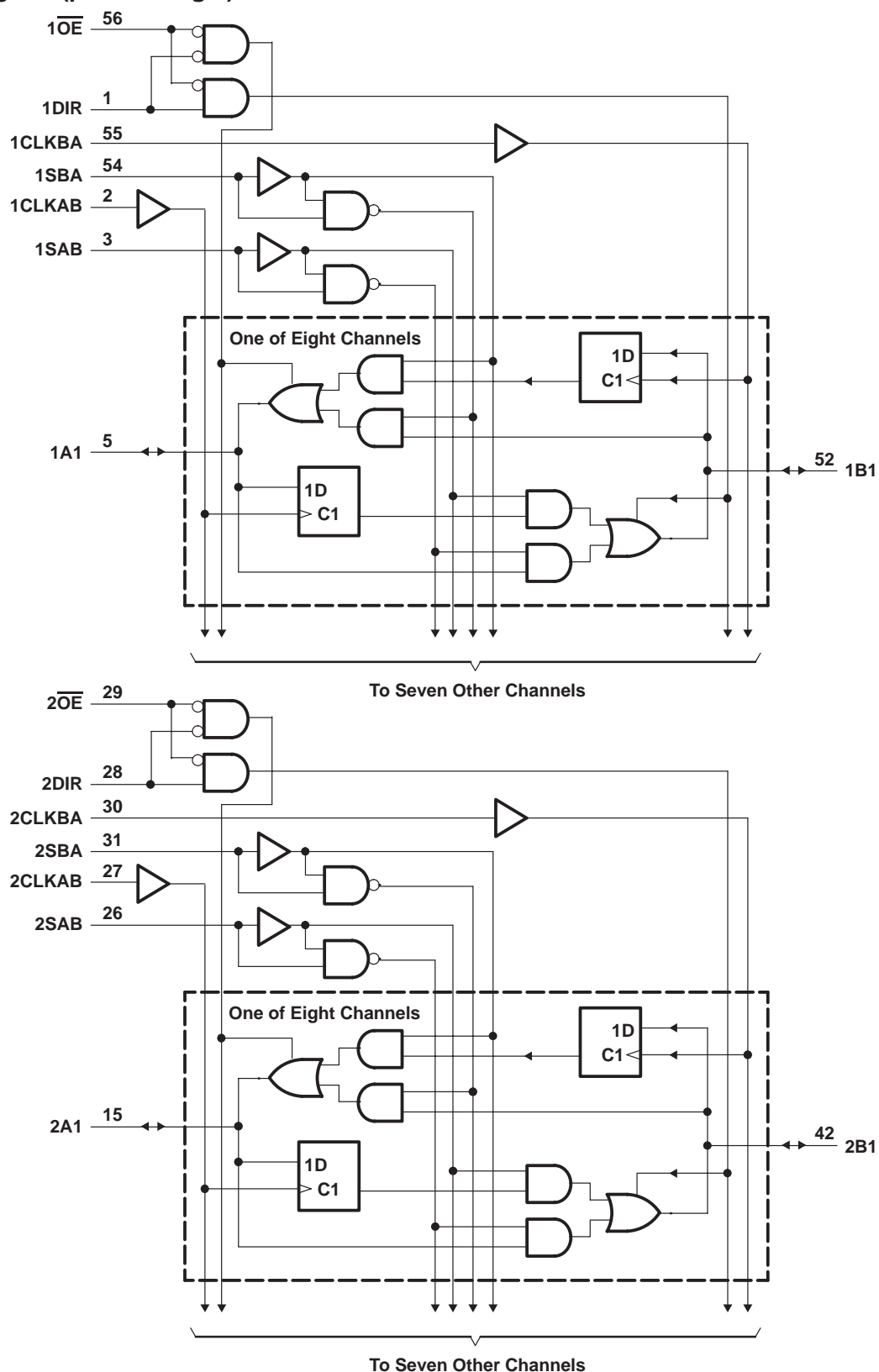
To Seven Other Channels

To Seven Other Channels

![Texas Instruments logo]

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V

Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V

Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) . . . . −0.5 V to 7 V

Current into any output in the low state, I_O: SN54LVT16646 . . . . 96 mA

SN74LVT16646 . . . . 128 mA

Current into any output in the high state, I_O (see Note 2): SN54LVT16646 . . . . 48 mA

SN74LVT16646 . . . . 64 mA

Input clamp current, I_{IK} (V_I < 0) . . . . −50 mA

Output clamp current, I_{OK} (V_O < 0) . . . . −50 mA

Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . 64°C/W

DL package . . . . 56°C/W

Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51–7.

recommended operating conditions (see Note 4)

			SN54LVT16646		SN74LVT16646		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t / \Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16646			SN74LVT16646			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = − 24 mA		2						
		I_{OH} = − 32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	$V_I = V_{CC}$ or GND	Control inputs			±1			±1	µA
	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	A or B ports§			20			20	
		$V_I = V_{CC}$				5			5	
		V_I = 0				−10			−10	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A or B ports	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				1			1	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−1			−1	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, $V_I = V_{CC}$ or GND		Outputs high			0.12			0.12	mA
			Outputs low			5			5	
			Outputs disabled			0.12			0.12	
ΔI_{CC}¶	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} − 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				3.5			3.5		pF
C_{io}	V_O = 3 V or 0				12			12		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

			SN54LVT16646				SN74LVT16646				UNIT
			$V_{CC} = 3.3\ V$ $\pm 0.3\ V$		$V_{CC} = 2.7\ V$		$V_{CC} = 3.3\ V$ $\pm 0.3\ V$		$V_{CC} = 2.7\ V$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.3		1.4		1.3		1.4		ns
		Data low	2.4		3		2.4		3		
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high	0.5		0		0.5		0		ns
		Data low	0.6		0.5		0.5		0.5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16646				SN74LVT16646					UNIT
			$V_{CC} = 3.3\ V$ $\pm 0.3\ V$		$V_{CC} = 2.7\ V$		$V_{CC} = 3.3\ V$ $\pm 0.3\ V$			$V_{CC} = 2.7\ V$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150				150					MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.8	6		6.9	1.8	3.8	5.7		6.7	ns
t_{PHL}			2.1	5.9		6.6	2.1	3.9	5.7		6.5	
t_{PLH}	A or B	B or A	1.3	4.9		5.6	1.3	3	4.7		5.4	ns
t_{PHL}			1	4.8		5.8	1	3.1	4.7		5.6	
t_{PLH}	SBA or SAB‡	A or B	1.4	6.4		7.4	1.4	4	6.2		7.2	ns
t_{PHL}			1.4	6.4		7.4	1.4	4.3	6.2		7.2	
t_{PZH}	$\overline{OE}$	A or B	1	5.7		7.4	1	3	5.4		6.4	ns
t_{PZL}			1	6.5		7.5	1	3.1	5.6		6.5	
t_{PHZ}	$\overline{OE}$	A or B	2.3	6.7		7.1	2.3	4.6	6.5		6.9	ns
t_{PLZ}			2.2	6		6.5	2.2	4.5	5.8		5.9	
t_{PZH}	DIR	A or B	1	5.9		7.7	1	3.3	5.7		6.7	ns
t_{PZL}			1.2	5.9		7.3	1.2	3.5	5.8		6.7	
t_{PHZ}	DIR	A or B	1.7	7.3		8.5	1.7	4.7	7.2		8.3	ns
t_{PLZ}			1.5	7.8		7.4	1.5	4.9	6.6		7.2	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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PARAMETER MEASUREMENT INFORMATION
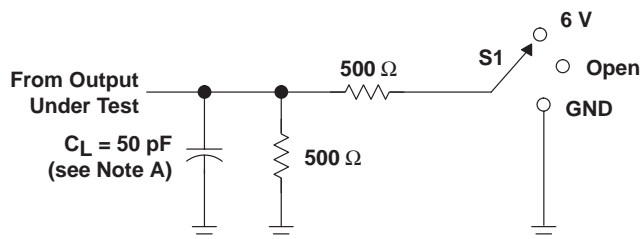
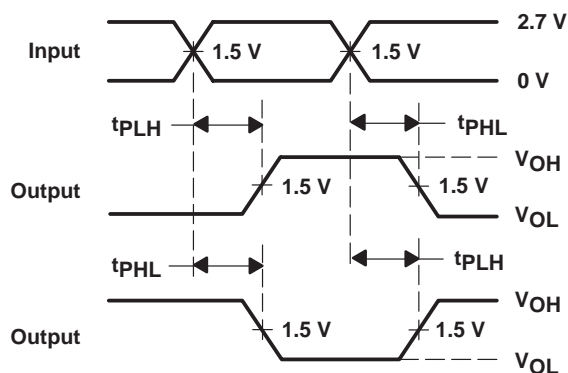LOAD CIRCUIT FOR OUTPUTS

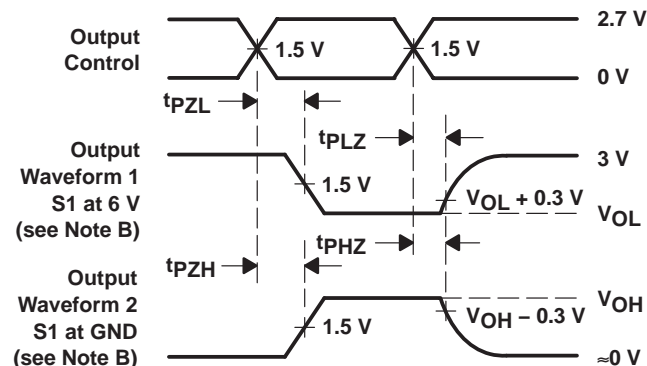| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND
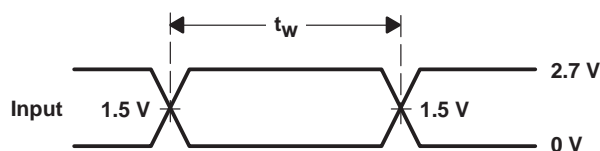
VOLTAGE WAVEFORMS
PULSE DURATION
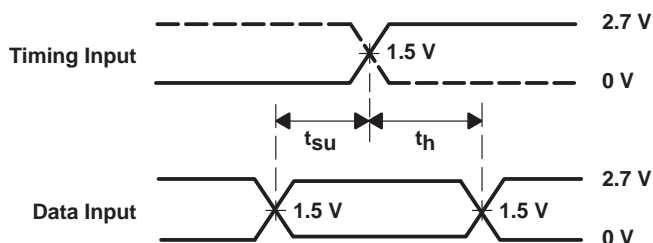
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number (1)	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVT16646DL	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16646
SN74LVT16646DL.B	Active	Production	SSOP (DL) | 56	20 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16646

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVT16646DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74LVT16646DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

56   29

0.420 (10,67)
0.395 (10,03)

0.010 (0,25)
0.005 (0,13)

0.299 (7,59)
0.291 (7,39)

Gage Plane

0.010 (0,25)

0°−8°

1   28

0.730 (18,54)
0.720 (18,29)

0.040 (1,02)
0.020 (0,51)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

0.004 (0,10)

4040048−4/F 05/13
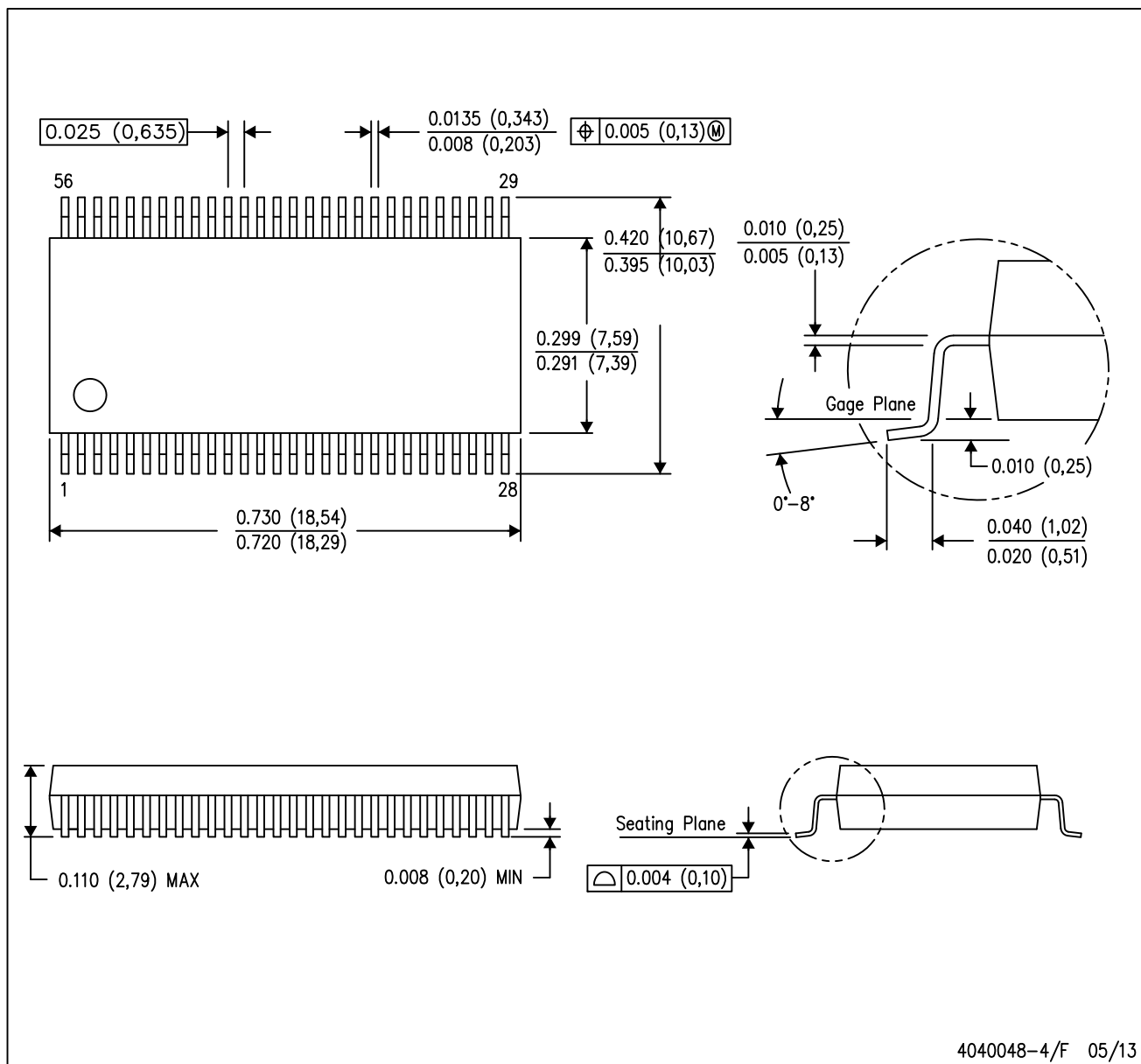
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO−118

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