TEXAS INSTRUMENTS

TS3DV642

SCDS343D – MAY 2013 – REVISED DECEMBER 2015

TS3DV642 12-Channel 1:2 MUX/DEMUX with 1.8 V Compatible Control and Power-Down Mode

1 Features

- Switch Type: 2:1 or 1:2
- Dynamic Characteristics
  - Differential Bandwidth (−3 dB)
    - Port A: 6.9 GHz Typical
    - Port B: 7.5 GHz Typical
  - Crosstalk (at 1.7 GHz): −40 dB
  - Isolation (at 1.7 GHz): −23 dB
  - Insertion Loss (DC)
    - Port A: −0.75 dB
    - Port B: −1.0 dB
  - Return Loss (at 1.7 GHz): −15.9 dB
  - Intra-Pair (Bit-Bit) Skew
    - Port A: 2 ps
    - Port B: 6 ps
  - R_{ON}
    - Port A: 6.5 Ω
    - Port B: 8.2 Ω
  - C_{ON} at 1 GHz: 0.5 pF (Typical)
- V_{CC} Range: 2.6 V to 4.5 V
- I/O Voltage Range: 0 V to 5 V
- Special Features
  - I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{CC} = 0 V)
- ESD Performance
  - 2-kV Human Body Model (A114B, Class II)
  - 1-kV Charged Device Model (C101)
- 42-pin WQFN Package (9 mm x 3.5 mm, 0.5 mm pitch)

2 Applications

- HDMI 2.0 With Support for 4k2k up to 60 Hz
- DVI 1.0 Signal Switching
- DisplayPort 1.2a Signal Switching
- General Purpose TMDS Signal Switching
- General Purpose LVDS Signal Switching
- General Purpose High-Speed Signal Switching

3 Description

The TS3DV642 is a 12 channel 1:2 or 2:1 bi-directional multiplexer/demultiplexer. The TS3DV642 operates from a 2.6 V to 4.5 V supply, making it suitable for battery-powered applications. It offers low and flat on-state resistance (R_{ON}) as well as low I/O capacitance which allows it to achieve a typical bandwidth of up to 7.5 GHz. The device provides the high bandwidth necessary for HDMI and DisplayPort applications.

The TS3DV642 offers a power-down mode, in which all channels become Hi-Z and the device operates with minimal power.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3DV642	WQFN (42)	9.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
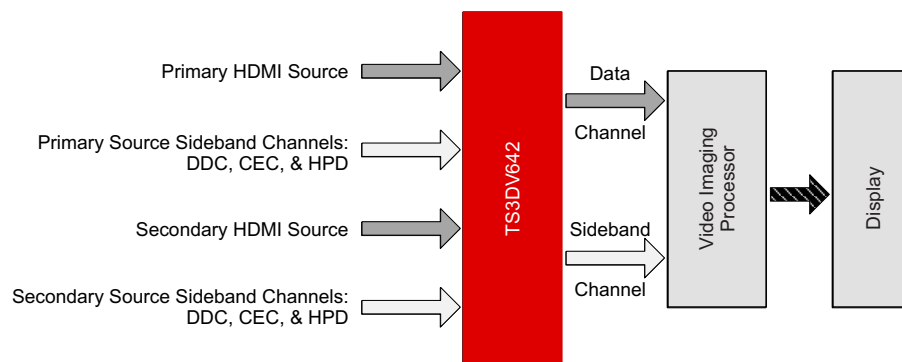
Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2014) to Revision D   **Page**

- Changed the storage temperature to the *Absolute Maximum Ratings* table 5

Changes from Revision B (August 2013) to Revision C   **Page**

- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. 1
- Deleted row from ABS MAX table: Package thermal impedance 5
- Added the Handling Ratings table, deleted the T_{stg} row Absolute Maximum ratings table and added to Handling Ratings table. 5

Changes from Revision A (July 2013) to Revision B   **Page**

- Changed Application From: HDMI 1.4/DVI 1.0 Signal Switching To: HDMI 1.4b with support for 4k2k up to 30 Hz 1
- Added Application: DVI 1.0 Signal Switching 1
- Changed Application From: DisplayPort 1.2 Signal Switching To: DisplayPort 1.2a Signal Switching................................. 1
- Added Eye Pattern and Time Interval Error Histogram graphics, Figure 10 to Figure 13 9

Product Folder Links: *TS3DV642*

5 Pin Configuration and Functions

RUA Package
42 Pin WQFN With Exposed Thermal Pad
Top View
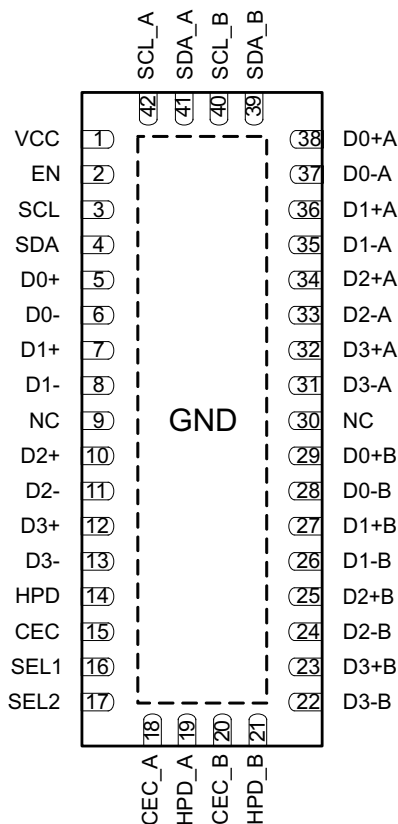
Pin Functions

PIN		Type	DESCRIPTION
NAME	NO.		
VCC	1	Power	Supply Voltage
SEL1	16	I	Select Input 1
SEL2	17	I	Select Input 2
EN	2	I	Output Enable
D0+A	38	I/O	Port A, Channel 0, +ve signal
D0–A	37	I/O	Port A, Channel 0, –ve signal
D1+A	36	I/O	Port A, Channel 1, +ve signal
D1-A	35	I/O	Port A, Channel 1, –ve signal
D2+A	34	I/O	Port A, Channel 2, +ve signal
D2–A	33	I/O	Port A, Channel 2,–ve signal
D3+A	32	I/O	Port A, Channel 3, +ve signal
D3–A	31	I/O	Port A, Channel 3, –ve signal
SCL_A	42	I/O	Port A, DDC Clock
SDA_A	41	I/O	Port A, DDC Data
HPD_A	19	I/O	Port A, Hot Plug Detects
CEC_A	18	I/O	Port A, Consumer Electronics Control
D0+B	29	I/O	Port B, Channel 0, +ve signal

Product Folder Links: *TS3DV642*

Pin Functions (continued)

PIN		Type	DESCRIPTION
NAME	NO.		
D0–B	28	I/O	Port B, Channel 0, –ve signal
D1+B	27	I/O	Port B, Channel 1, +ve signal
D1–B	26	I/O	Port B, Channel 1, –ve signal
D2+B	25	I/O	Port B, Channel 2, +ve signal
D2–B	24	I/O	Port B, Channel 2,–ve signal
D3+B	23	I/O	Port B, Channel 3, +ve signal
D3–B	22	I/O	Port B, Channel 3, –ve signal
SCL_B	40	I/O	Port B, DDC Clock
SDA_B	39	I/O	Port B, DDC Data
HPD_B	21	I/O	Port B, Hot Plug Detects
CEC_B	20	I/O	Port B, Consumer Electronics Control
D0+	5	I/O	Common Port, Channel 0, +ve signal
D0–	6	I/O	Common Port, Channel 0, –ve signal
D1+	7	I/O	Common Port, Channel 1, +ve signal
D1–	8	I/O	Common Port, Channel 1, –ve signal
D2+	10	I/O	Common Port, Channel 2, +ve signal
D2–	11	I/O	Common Port, Channel 2, –ve signal
D3+	12	I/O	Common Port, Channel 3, +ve signal
D3–	13	I/O	Common Port, Channel 3,–ve signal
SCL	3	I/O	Common Port, DDC Clock
SDA	4	I/O	Common Port, DDC Data
HPD	14	I/O	Common Port, Hot Plug Detects
CEC	15	I/O	Common Port, Consumer Electronics Control
NC	9, 30	NC	No Connect
GND	PowerPad	GND	Ground

Product Folder Links: *TS3DV642*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	5.5	V
$V_{I/O}$	Analog voltage range [2][3][4]	All I/O	−0.5	5.5	V
V_{IN}	Digital input voltage range [2][3]	SEL1, SEL2, EN	−0.5	5.5	V
$I_{I/OK}$	Analog port diode current	$V_{I/O} < 0$		−50	mA
I_{IK}	Digital input clamp current	$V_{IN} < 0$		−50	mA
$I_{I/O}$	On-state switch current [5]		−128	128	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, [1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, [2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.6	4.5	V
$V_{I/O}$	Input/Output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

(1) All unused control inputs of the device must be held at VDD or GND to ensure proper device operation. Refer to the *TI application report, Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.

6.4 Thermal Information

	THERMAL METRIC[1]	TS3DV642	UNIT
		RUA	
		42 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.5	°C
			W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.2	°C
			W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.5	°C
			W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C
			W
Ψ_{JB}	Junction-to-board characterization parameter	5.4	°C
			W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Product Folder Links: *TS3DV642*

Thermal Information (continued)

THERMAL METRIC[1]		TS3DV642	UNIT
		RUA	
		42 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.	°C
			W

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS[1]	MIN	TYP[2]	MAX	UNIT
PORT A							
R_{ON}	ON-state resistance	D0 to D3	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40 mA		6.5	9.5	Ω
		SCL, SDA, HPD, CEC			6	9.5	Ω
$R_{ON(flat)}$[3]	ON-state resistance flatness	All I/O	V_{CC} = 3 V, $V_{I/O}$ = 1.5 V and V_{CC}, $I_{I/O}$ = –40 mA		1.5		Ω
ΔR_{ON}[4]	On-state resistance match between high-speed channels	D0 to D3	VCC = 3 V, 1.5 V ≤ VI/O ≤ V_{CC}, $I_{I/O}$ = –40 mA		0.4	1	Ω
I_{OFF}	Leakage under power off	All outputs	V_{CC} = 0 V, $V_{I/O}$ = 0 to 3.6 V, V_{IN} = 0 V to 5.5 V			±10	µA
PORT B							
R_{ON}	ON-state resistance	D0 to D3	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40 mA		8.2	10.5	Ω
		SCL, SDA, HPD, CEC			6	9.5	Ω
$R_{ON(flat)}$[3]	ON-state resistance flatness	All I/O	V_{CC} = 3 V, $V_{I/O}$ = 1.5 V and V_{CC}, $I_{I/O}$ = –40 mA		1.5		Ω
ΔR_{ON}[4]	On-state resistance match between high-speed channels	D0 to D3	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40 mA		0.4	1	Ω
I_{OFF}	Leakage under power off	All outputs	V_{CC} = 0 V, $V_{I/O}$ = 0 V to 3.6 V, V_{IN} = V to 5.5 V			±10	µA
DIGITAL INPUTS (SEL1, SEL2, EN)							
V_{IH}	High-level control input voltage	SEL1, SEL2, EN		1.4			V
V_{IL}	Low-level control input voltage	SEL1, SEL2, EN				0.5	V
I_{IH}	Digital input high leakage current	SEL1, SEL2, EN	V_{CC} = 3.6 V , V_{IN} = V_{DD}			±10	µA
I_{IL}	Digital input low leakage current	SEL1, SEL2, EN	V_{CC} = 3.6 V, V_{IN} = GND			±10	µA
SUPPLY							
I_{CC}	VCC supply current		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Normal Operation Mode, EN = H		50		µA
I_{CC}, PD	VCC supply current in power-down mode		V_{CC} = 3.6 V, $I_{I/O}$ = 0, EN = L		6		µA

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $R_{ON(FLAT)}$ is the difference of R_{ON} in a given channel at specified voltages.
(4) ΔR_{ON} is the difference of RON from center port to any other ports.

6.6 Dynamic Characteristics

Over recommended operation free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
C_{IN}	Digital input capacitance	f = 1 MHz, V_{IN} = 0 V		6		pF
Coff	Switch OFF capacitance	f = 1 GHz, $V_{I/O}$ = 0 V, Output is open, Switch is OFF		0.3		pF

(1) All Typical Values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

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Dynamic Characteristics (continued)

Over recommended operation free-air temperature range, V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
Con	Switch ON capacitance	f = 1 GHz, $V_{I/O}$ = 0 V, Output is open, Switch is ON		0.5		pF
Xtalk	Differential Crosstalk	R_L = 50 Ω at 1.7 GHz (See Figure 17)		−40		dB
		R_L = 50 Ω at 2.7 GHz (See Figure 18)		−40		
OISO	Differential Off Isolation	R_L = 50 Ω at 1.7 GHz (See Figure 18)		−23		dB
		R_L = 50 Ω at 2.7 GHz (See Figure 18)		−28		
IL	Insertion Loss	Port A at DC		−0.75		dB
		Port B at DC		−1		dB
BW	Differential Bandwidth (−3 dB)	Port A	R_L = 50 Ω, All channels (See Figure 19)		6.9		GHz
		Port B	R_L = 50 Ω, All channels (See Figure 19)		7.5		

6.7 Switching Characteristics

over recommended operation free-air temperature range, V_{CC} = 3.3 V± 0.3 V (unless otherwise noted)

PARAMETER				TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
t_{ON}[2]	Switch turn-on time		All I/O	See Figure 14				100	µs
t_{SWITCH}[3]	Switching time between channels		All I/O	See Figure 15			20		µs
t_{pd}	Propagation Delay	Port A	D0 to D3	See Figure 16			30		ps
			SCL, SDA, HPD, CEC				30		
		Port B	D0 to D3				40		
			SCL, SDA, HPD, CEC				30		
t_{SKEW}	Inter-pair Skew	Port A	D0 to D3	Between +ve and −ve signals of each Channel			2		ps
		Port B					2		
	Intra-pair Skew	Port A		Between Channel 0, 1, 2, or 3			2		
		Port B					6		

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) t_{ON} is the time it takes the output to recover after enabling switches
(3) t_{SWITCH} is the time it takes for the output to recover after the state is changed

6.8 Typical Characteristics

m1
freq=1.600MHz
dB(S(2,1))=-0.925

m2
freq=6.649GHz
dB(S(2,1))=-3.925
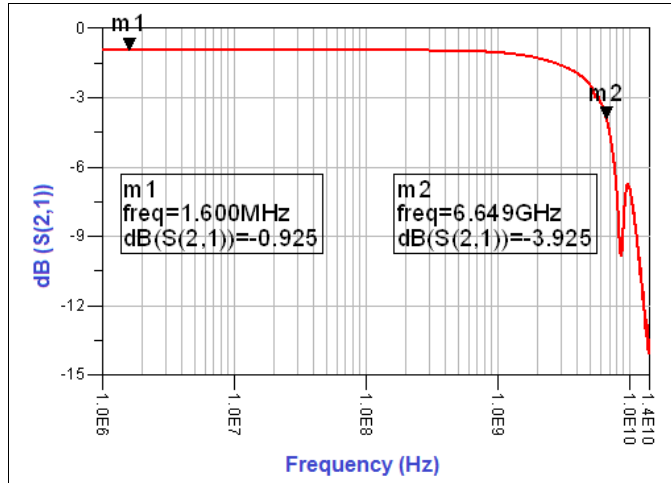
Figure 1. Differential S21 vs Frequency for Port A

m3
freq=1.700MHz
dB(S(4,3))=-0.827

m4
freq=7.730GHz
dB(S(4,3))=-3.827
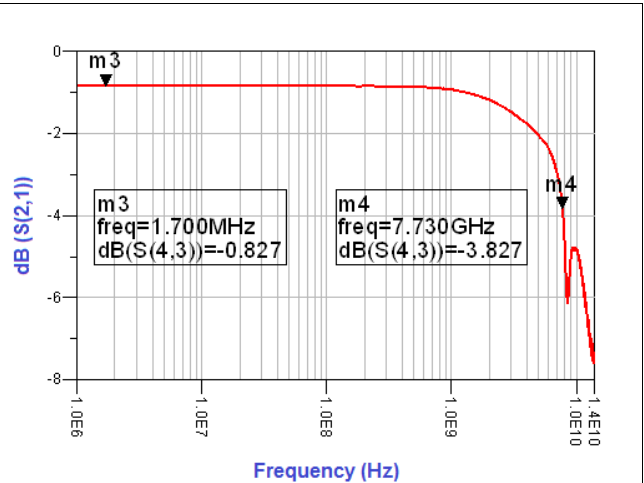
Figure 2. Differential S21 vs Frequency for Port B
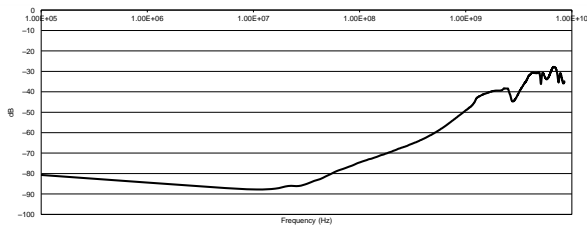
Figure 3. XTALK Port A
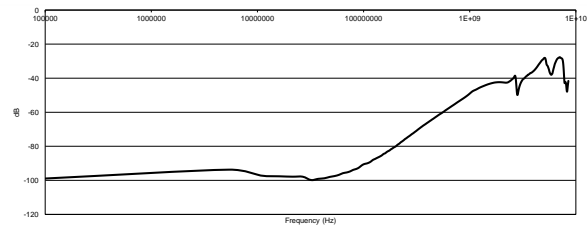
Figure 4. XTALK Port B
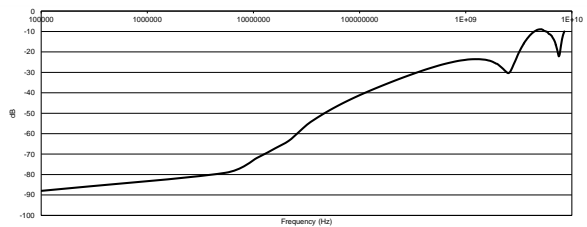
Figure 5. Off-State Isolation (OISO) for Port A
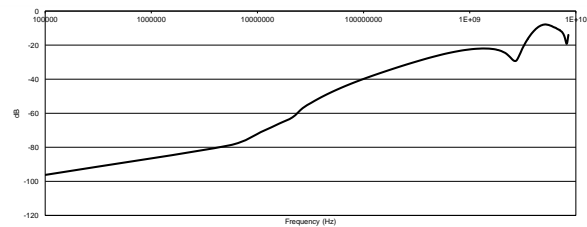
Figure 6. Off-State Isolation (OISO) for Port B

Product Folder Links: *TS3DV642*

Typical Characteristics (continued)
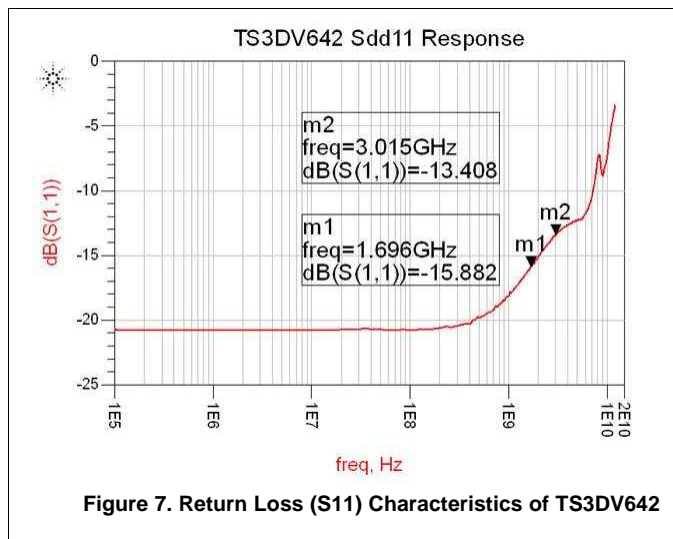
Figure 7. Return Loss (S11) Characteristics of TS3DV642
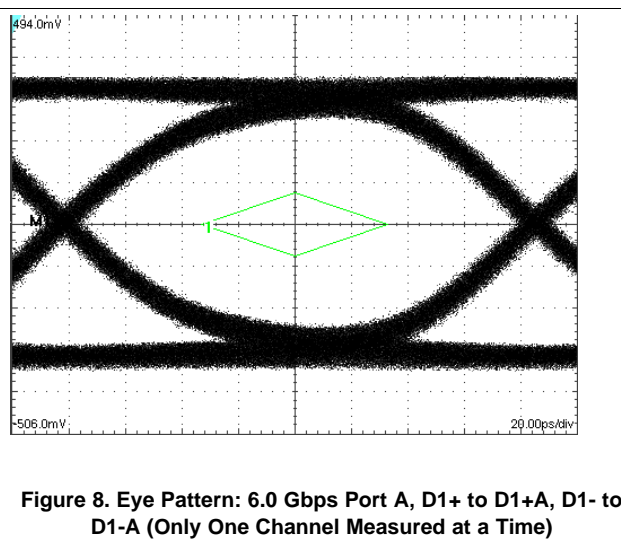
Figure 8. Eye Pattern: 6.0 Gbps Port A, D1+ to D1+A, D1- to D1-A (Only One Channel Measured at a Time)
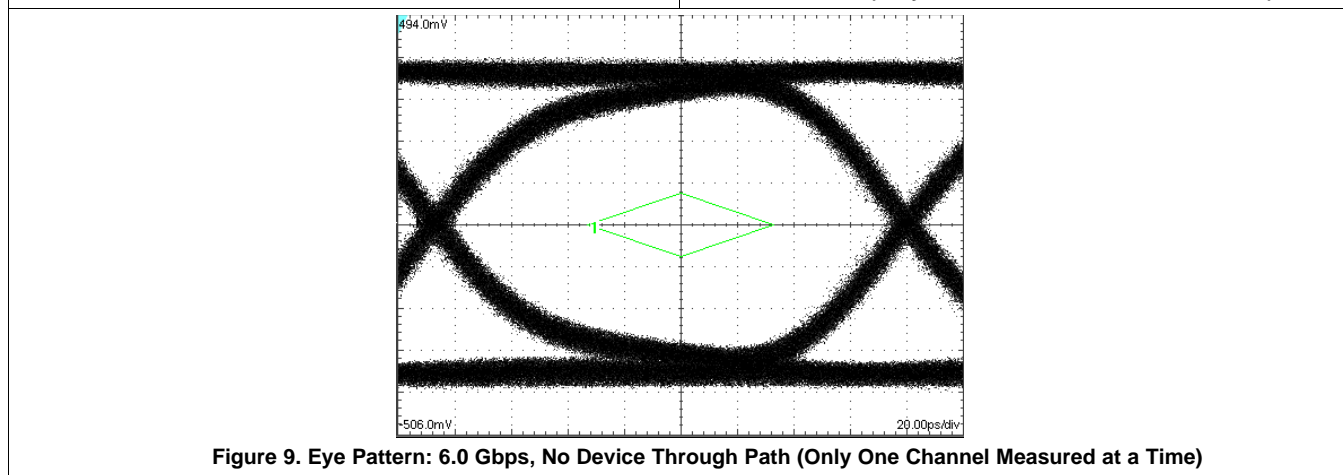
Figure 9. Eye Pattern: 6.0 Gbps, No Device Through Path (Only One Channel Measured at a Time)
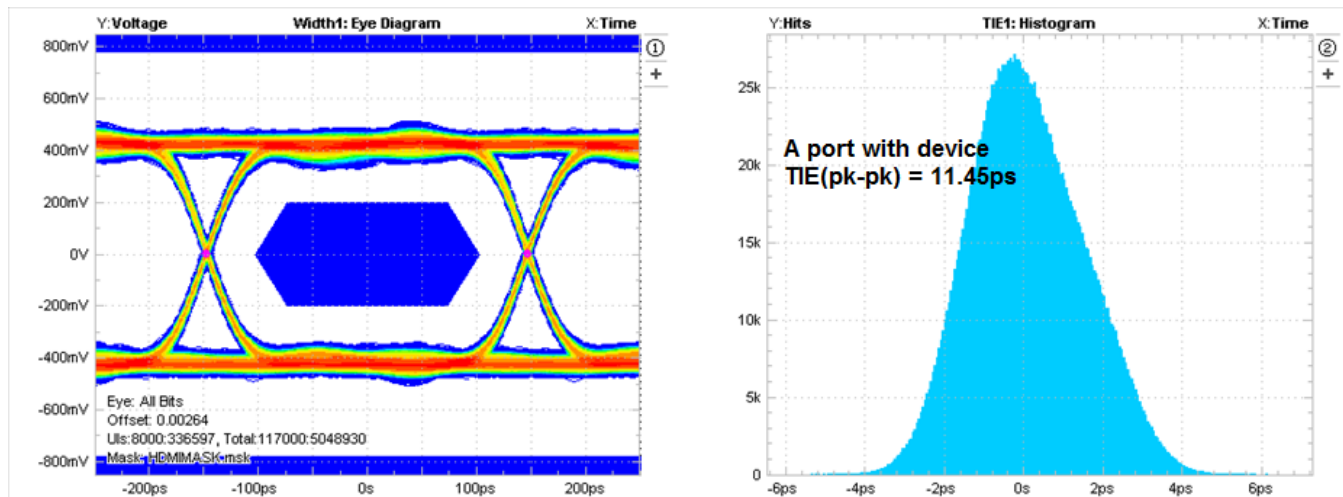
Figure 10. Eye Pattern and Time Interval Error Histogram: 3.4 Gbps Port A, With Device
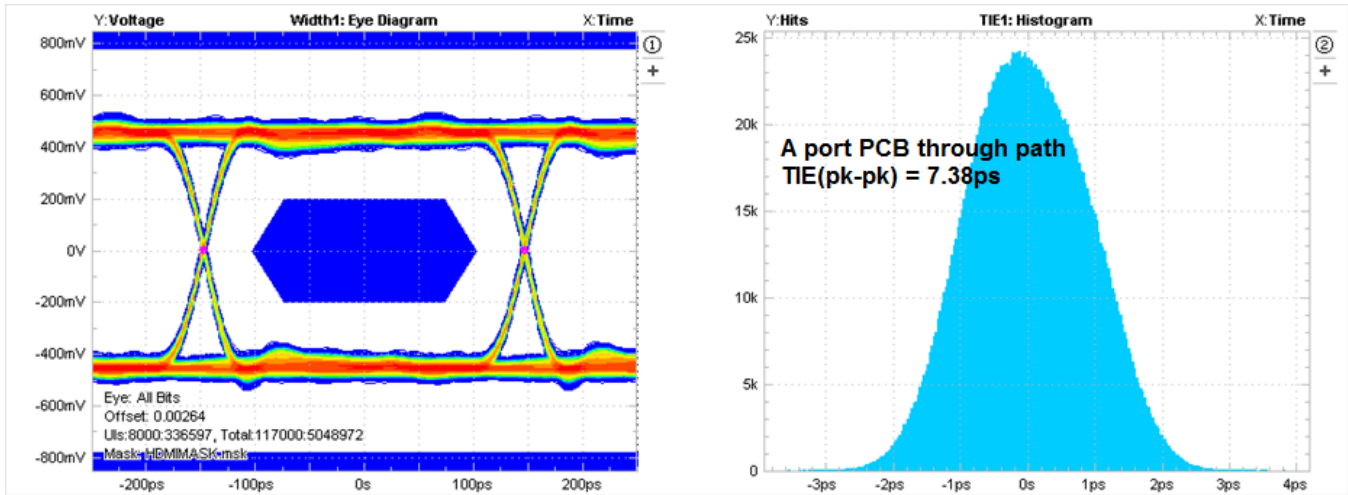
Figure 11. Eye Pattern and Time Interval Error Histogram: 3.4 Gbps, No Device Through Path
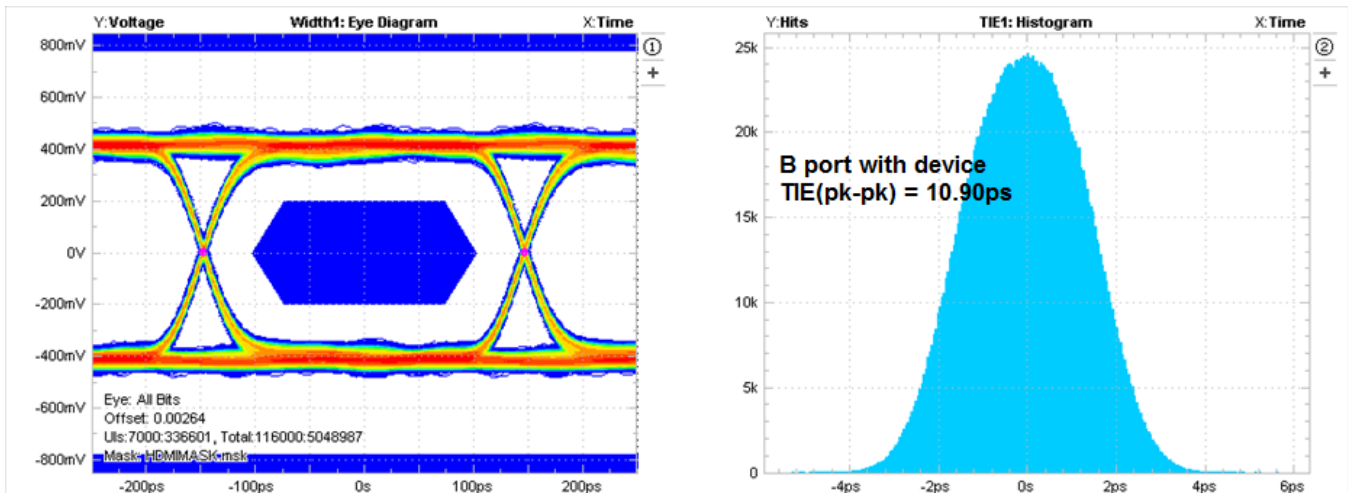
Figure 12. Eye Pattern and Time Interval Error Histogram: 3.4 Gbps Port B, With Device
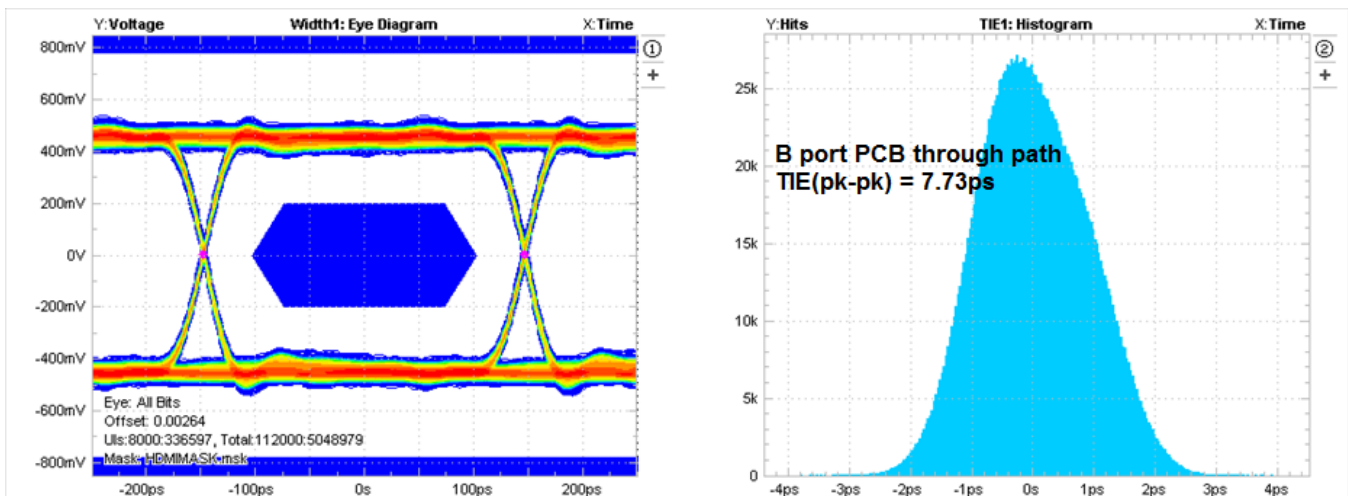
Figure 13. Eye Pattern and Time Interval Error Histogram: 3.4 Gbps Port B, No Device

7 Parameter Measurement Information
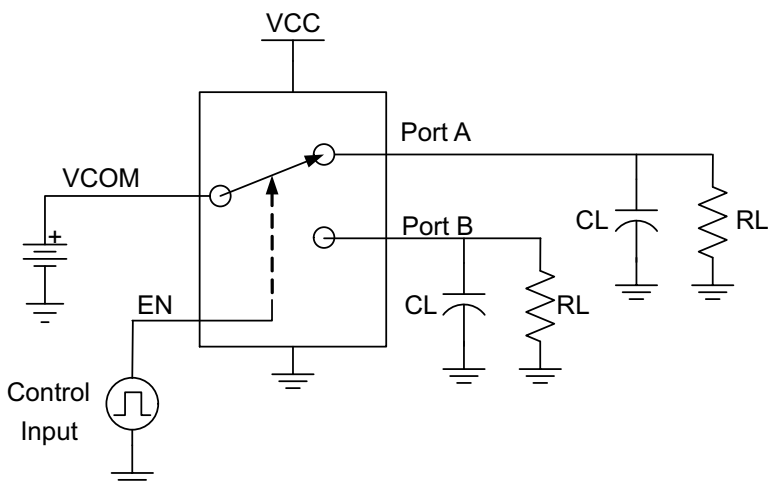
RL	CL	VCOM
50 Ω	4 pF	VCC

*CL includes probe, cable, and board capacitance
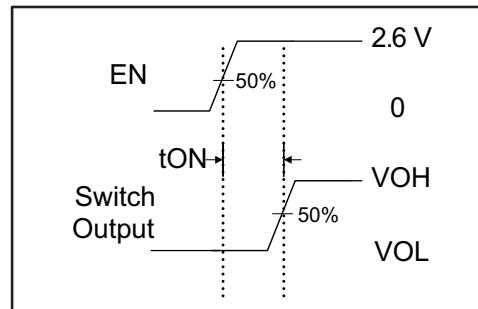
Figure 14. Switch Turn-On Time (t$_{ON}$)
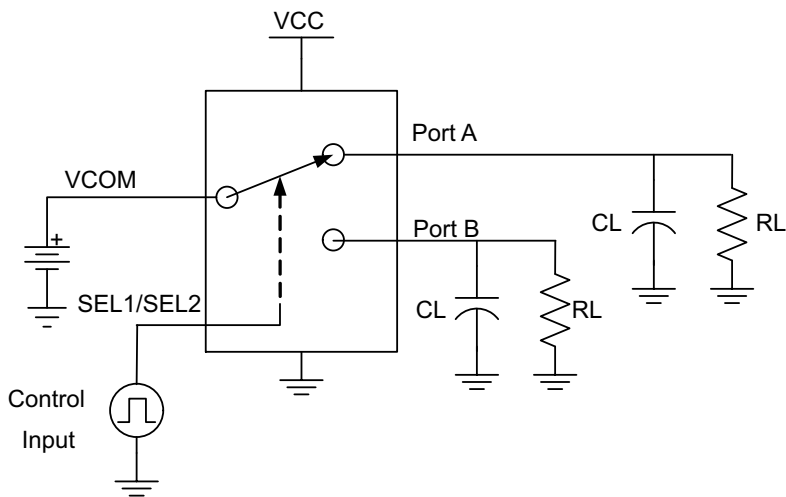
RL	CL	VCOM
50 Ω	4 pF	Vcc

*CL includes probe, cable, and board capacitance
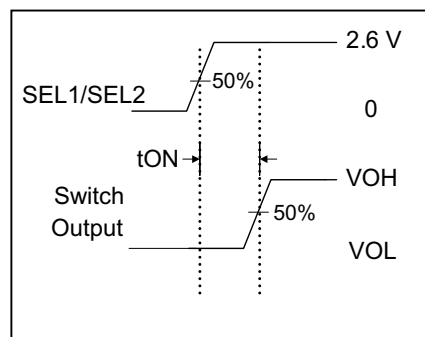
Figure 15. Switching Time Between Channels (t$_{SWITCH}$)
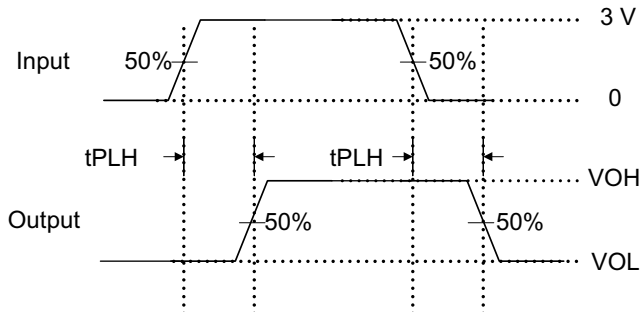
$$tpd = (tPLH + tPLH) / 2$$

Figure 16. Propagation Delay (t$_{pd}$)

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Parameter Measurement Information (continued)
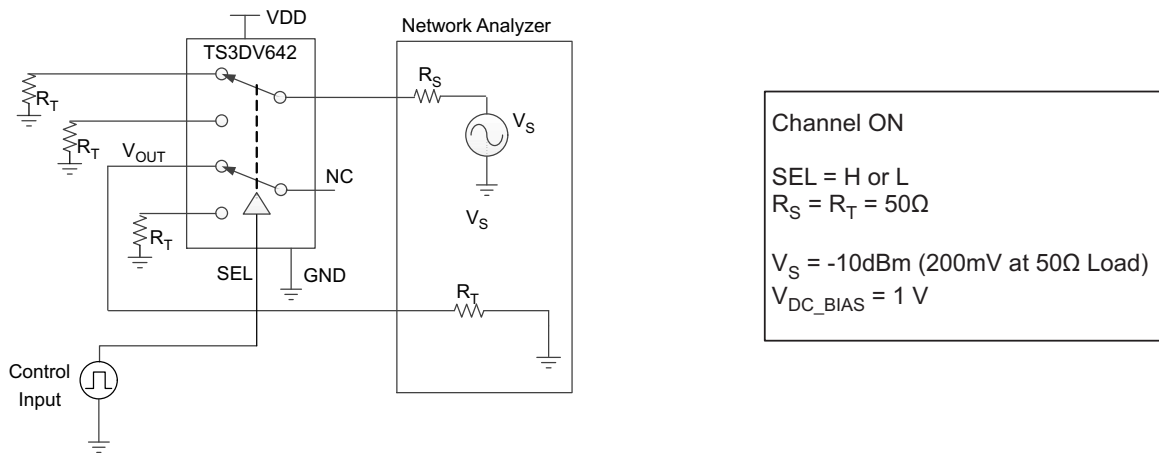
Figure 17. Crosstalk (Xtalk)
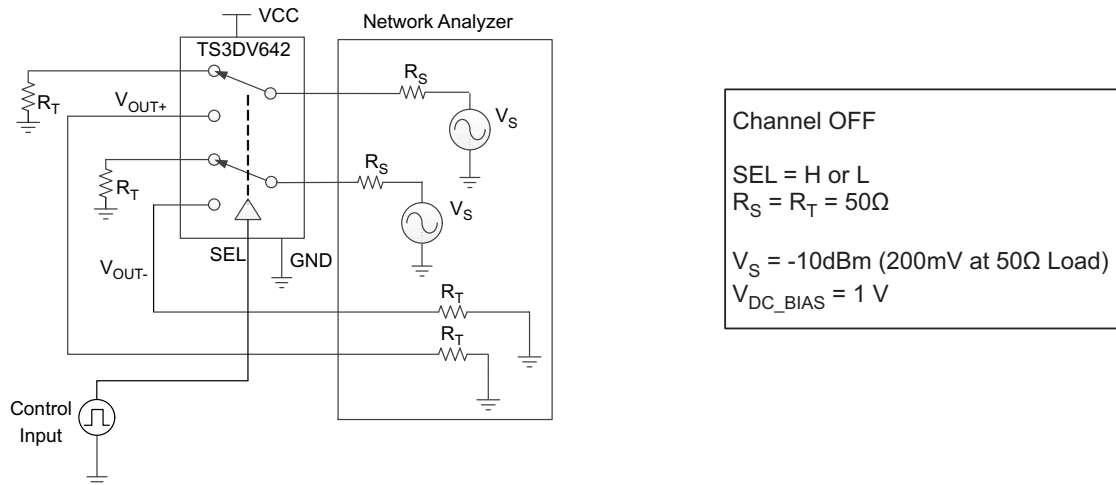
Figure 18. Differential Off-Isolation (OISO)
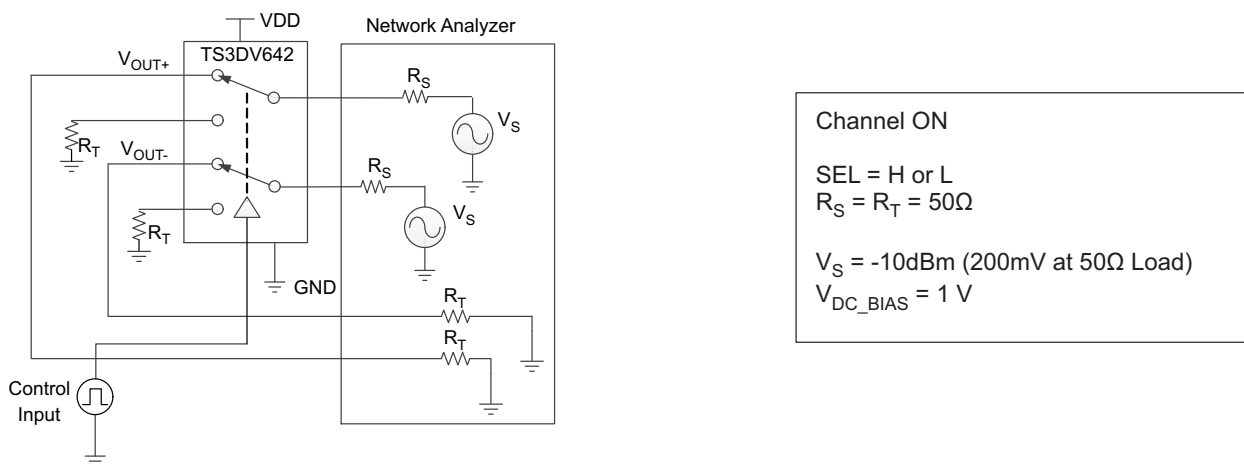
Figure 19. Differential Bandwidth (BW)

Product Folder Links: *TS3DV642*

8 Detailed Description

8.1 Overview

TS3DV642 is a 12-channel 1:2 or 2:1 bidirectional multiplexer/demultiplexer. The TS3DV642 operates from a 2.6 to 4.5 V supply, making it suitable for battery-powered applications. It offers low and flat on-state resistance as well as low I/O capacitance which allows it to achieve a typical bandwidth of up to 7.5 GHz. The device provides the high bandwidth necessary for HDMI and DisplayPort applications.

8.2 Functional Block Diagram
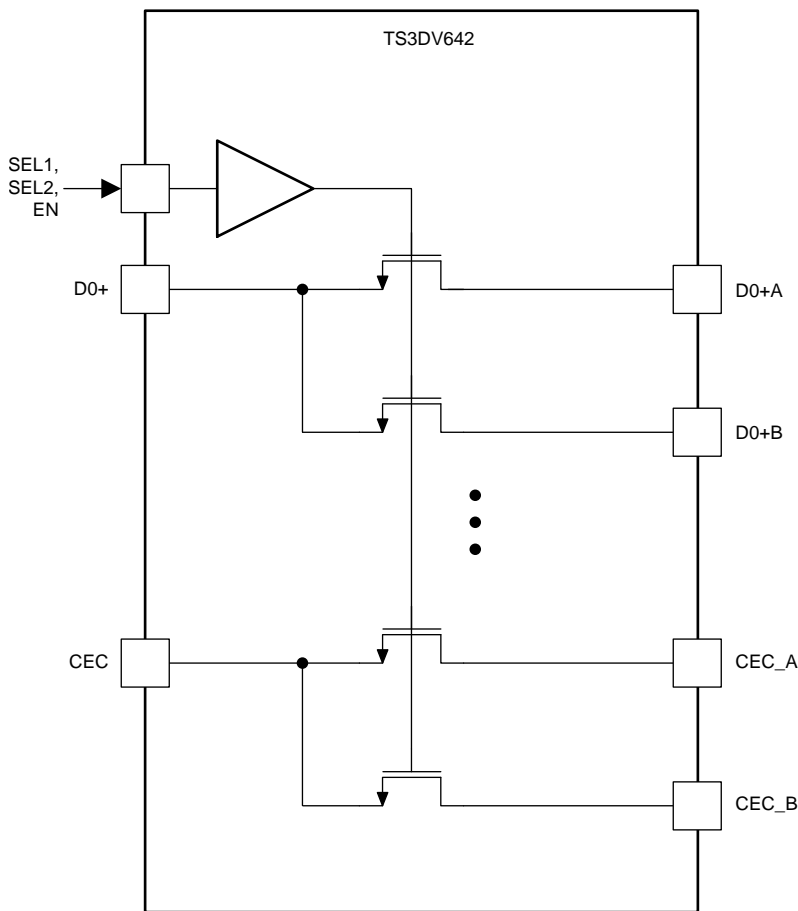
8.3 Feature Description

The TS3DV642 is based on proprietary TI technology which uses FET switches driven by a high-voltage generated from an integrated charge-pump to achieve a low on-state resistance. TS3DV642 has 12-channel bidirectional switches with a high bandwidth (~ 7.5 GHz). TS3DV642 uses an extremely low power technology and uses only 50 µA I_{CC} in active mode. The device has integrated ESD that can support up to 2-kV Human-Body Model (HBM) and 1-kV Charge Device Model (CDM). TS3DV642 is offered in a 42-pin QFN package (9 mm x 3.5 mm) with 0.5 mm pitch. The device can support analog I/O signal in 0 to 5 V range. TS3DV642 also has a special feature that prevents the device from back-powering when the V_{CC} supply is not available and an analog signal is applied on the I/O pin. In this situation this special feature prevents leakage current in the device. The TS3DV642 is not designed for passing signals with negative swings; the high-speed signals need to be properly DC biased (usually ~1 V) before being passed to the TS3DV642. The differential S21 characteristics as a function of frequency for Port A and Port B are shown in Figure 1 and Figure 2, respectively. The figures show a differential bandwidth of 6.7 GHz and 7.7 GHz for Port A and Port B, respectively. The cross-talk (XTALK) characteristics as a function of frequency are shown in Figure 3 and Figure 4, respectively. The off-state isolation (OISO) characteristics for Port A and Port B are shown in Figure 5 and Figure 6, respectively. The return loss

Feature Description (continued)

characteristics (S11) are shown in Figure 7. The eye pattern and Time Interval Error (TIE) histogram at 3.4 Gbps (for HDMI 1.4 applications) with TS3DV642 in path for Port A is shown in Figure 10. The eye pattern and Time Interval Error (TIE) histogram at 3.4 Gbps through path (no TS3DV642) for Port A is shown in Figure 11. The eye pattern and Time Interval Error (TIE) histogram at 3.4 Gbps (for HDMI 1.4 applications) with TS3DV642 in path for Port B is shown in Figure 12. The eye pattern and Time Interval Error (TIE) histogram at 3.4 Gbps through path (no TS3DV642) for Port A is shown in Figure 13. The eye pattern at 6.0 Gbps (for HDMI 2.0 applications) with TS3DV642 in path for Port A is shown in Figure 8. The eye pattern at 6.0 Gbps (for HDMI 2.0 applications) through path (no TS3DV642) for Port A is shown in Figure 9. Note that the eye patterns are measured with only one channel on at a time.

8.4 Device Functional Modes
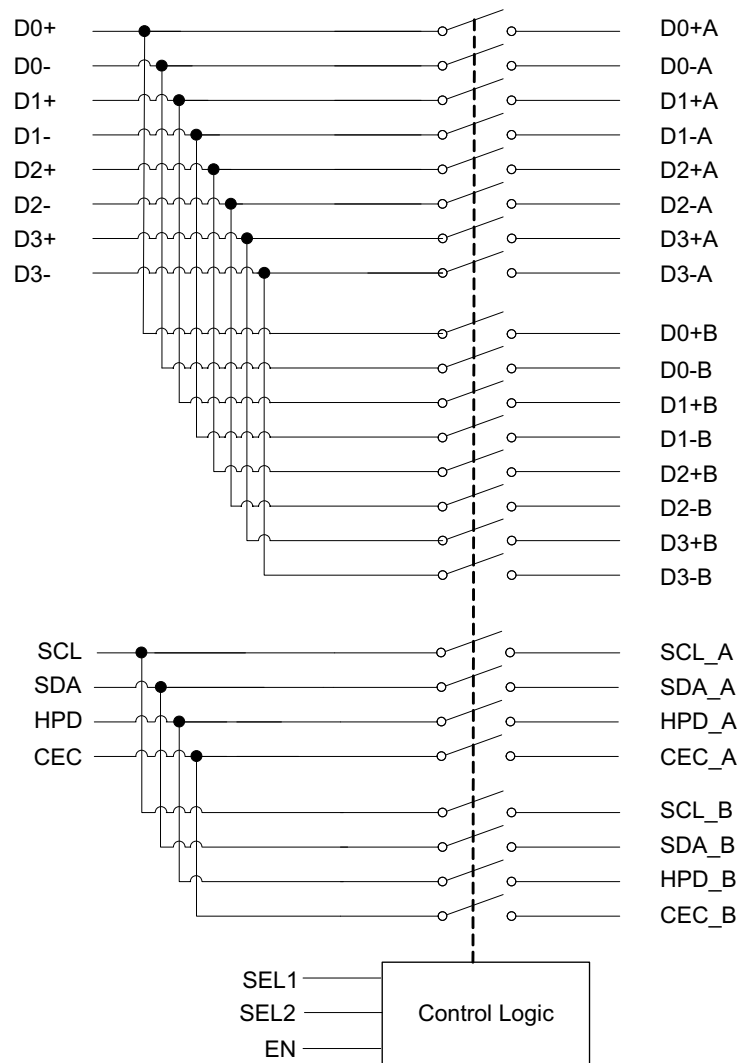
Figure 20. Logic Diagram

Table 1 lists the device functions for the TS3DV642 device.

Table 1. Functional Table

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch disabled. All channels are Hi-Z.

Device Functional Modes (continued)

Table 1. Functional Table (continued)

EN	SEL1	SEL2	FUNCTION
H	L	L	Channel D0+/D0− to D0+A/D0−A is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z.
H	L	H	Channel D0+/D0− to D0+B/D0−B is ON. All the other channels (D1+/D1-, D2+/D2-, D3+/D3-, SCL, SDA, HPD, CEC) are Hi-Z.
H	H	L	All A channels are enabled. All B channels are Hi-Z.
H	H	H	All B channels are enabled. All A channels are Hi-Z.

9   Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1   Application Information

TS3DV642 can be used for two typical DisplayPort applications. Figure 21 describes a DisplayPort (DP) application where TS3DV642 is used to switch between two different graphic & memory controllers on a single DP connector. Figure 24 shows a docking application where TS3DV642 is used to switch signals from a single graphic and memory controller to a display port and docking station connector. Note that the TS3DV642 is not designed for passing signals with negative swings; the high-speed signals need to be properly DC biased (usually ~1 V from the graphic controller side) before being passed to the TS3DV642.

9.2   Typical Application

9.2.1   Display Port (DP) Application

Display port (DP) application with TS3DV642 used to switch between two different graphic & memory controllers on a single DP connector

Product Folder Links: *TS3DV642*

Typical Application (continued)
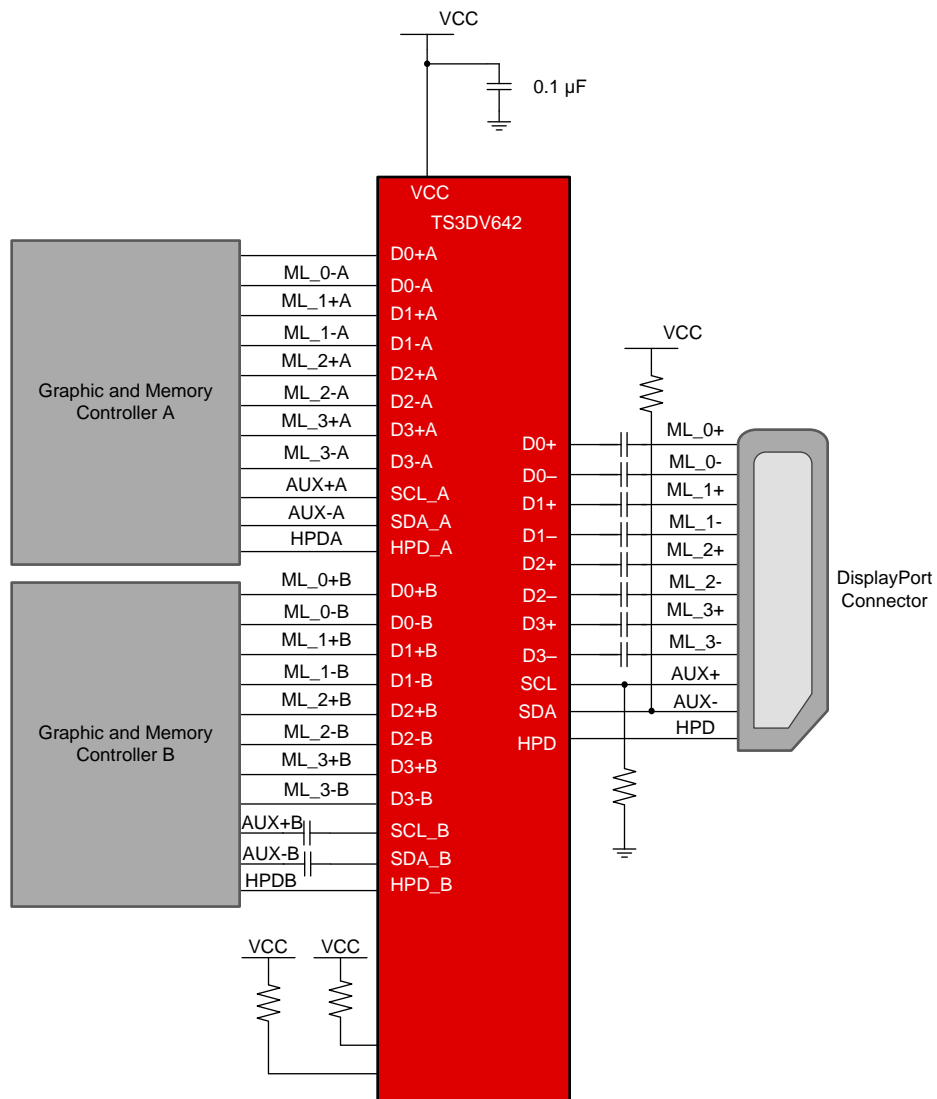
Figure 21. Display Port Schematic

Typical Application (continued)

9.2.1.1 Design Requirements

Table 2. Design parameters for Display Port application

Design parameter	Example value
V_{CC}	2.6 V to 4.5 V
VCC decoupling capacitor	0.1 µF
MainLink (ML) and AUX coupling capacitor	75 nF to 200 nF
AUX Pull-up / Pull-down resistors	10 kΩ to 100 kΩ
Pull-up / Pull-down resistors for SEL1 / SEL2 pins	10 kΩ

9.2.1.2 Detailed Design Procedure

The TS3DV642 is designed to operate with 2.6 V – 4.5 V power supply. The wide power supply range allows flexibility for battery powered applications. If a higher power supply is used in the system, a voltage regulator can be used to bring down the voltage to 2.6 V – 4.5 V range. Decoupling capacitors may be used to reduce noise and improve power supply integrity. AC coupling capacitors in 75 nF – 200 nF range must be placed on the MainLink (ML) and AUX lanes. In this particular application the AC coupling capacitors are shown on the connector side. The AC coupling capacitors may also be placed on the signal path on controller side. The AUX+ line must be pulled-down weakly through a resistor to ground and the AUX– line must be pulled-up weakly through a resistor to VCC.
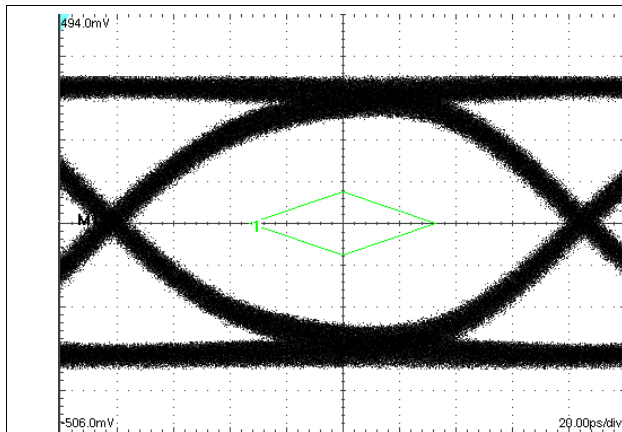
9.2.1.3 Application Curves
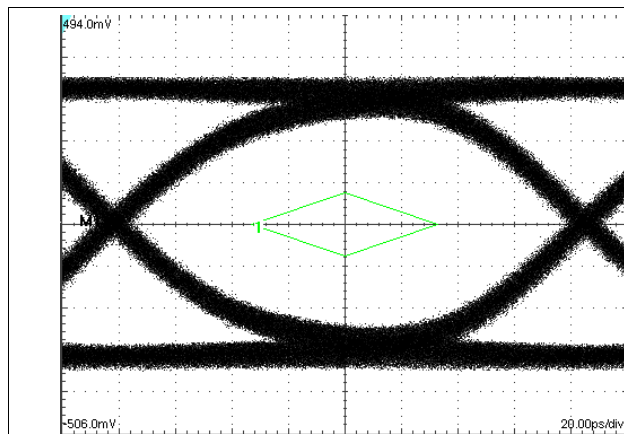
Figure 22. Eye Pattern: 6.0 Gbps Port A, D1+ to D1+A, D1- to D1-A (Only One Channel Measured at a Time)
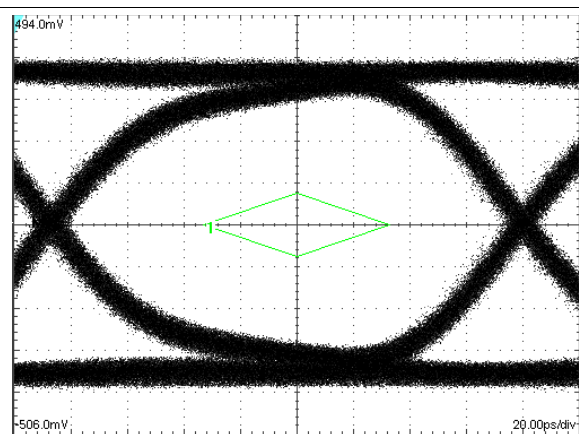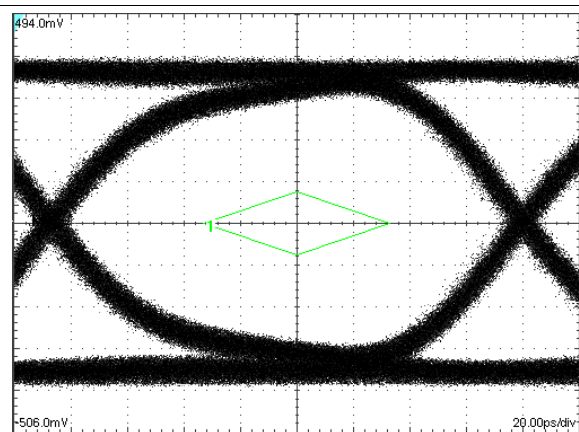
Figure 23. Eye Pattern: 6.0 Gbps, No Device Through Path (Only One Channel Measured at a Time)

Product Folder Links: *TS3DV642*

9.2.2 Docking Application

Docking Application with TS3DV642 used to switch signals from a single graphic and memory controller to a display port and docking station connector.
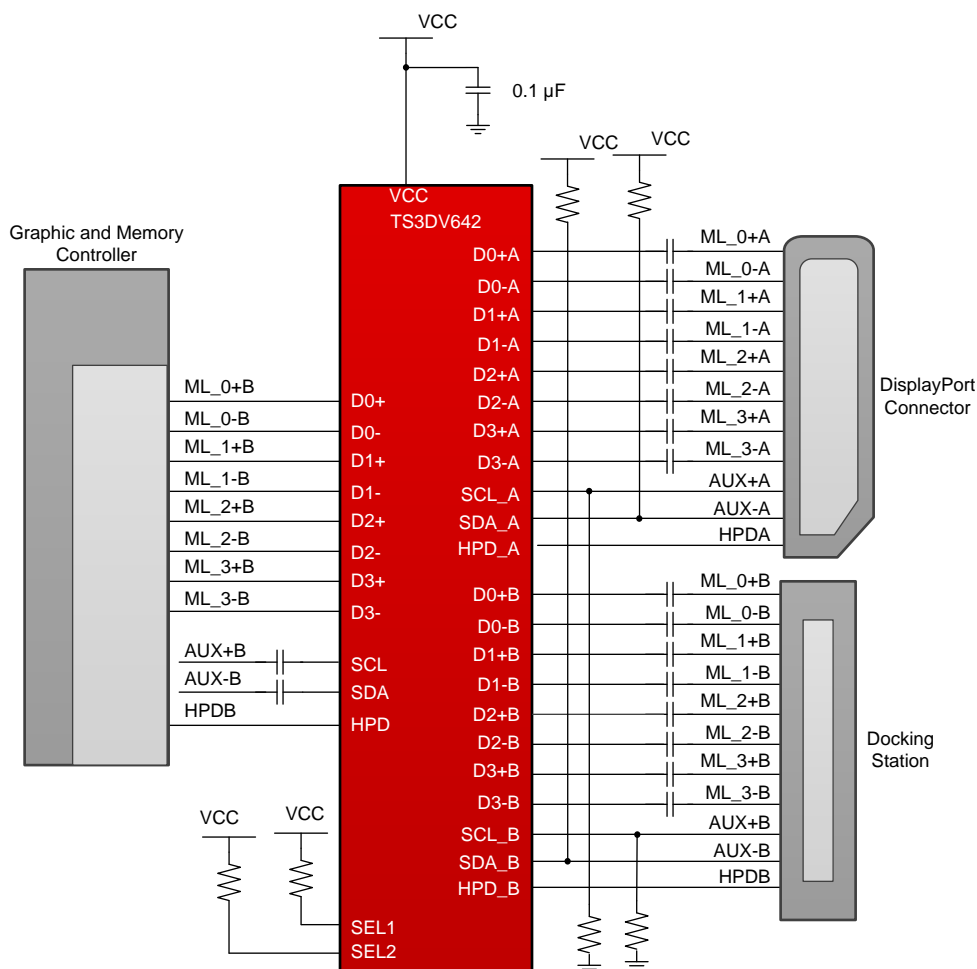
Figure 24. Docking Application Schematic

9.2.2.1 Design Requirements

Table 3. Design parameters for docking application

Design parameter	Example value
V_{CC}	2.6 V to 4.5 V
VCC decoupling capacitor	0.1 µF
MainLink (ML) and AUX coupling capacitor	75 nF to 200 nF
AUX Pull-up / Pull-down resistors	10 kΩ to 100 kΩ
Pull-up / Pull-down resistors for SEL1 / SEL2 pins	10 kΩ

9.2.2.2 Detailed Design Procedure

The TS3DV642 is designed to operate with 2.6 V – 4.5 V power supply. The wide power supply range allows flexibility for battery powered applications. If a higher power supply is used in the system, a voltage regulator can be used to bring down the voltage to 2.6 V – 4.5 V range. Decoupling capacitors may be used to reduce noise and improve power supply integrity. AC coupling capacitors in 75 nF – 200 nF range must be placed on the MainLink (ML) and AUX lanes. In this particular application the AC coupling capacitors are shown on the connector side. The AC coupling capacitors may also be placed on the signal path on controller side. The AUX+ line must be pulled-down weakly through a resistor to ground and the AUX− line must be pulled-up weakly through a resistor to VCC.

9.2.2.3 Application Curves

Figure 25. Eye Pattern: 6.0 Gbps Port A, D1+ to D1+A, D1- to D1-A (Only One Channel Measured at a Time)

Figure 26. Eye Pattern: 6.0 Gbps, No Device Through Path (Only One Channel Measured at a Time)

9.2.3 HDMI Application

HDMI Application with TS3DV642 used to switch signals from a single graphic and memory controller to a two HDMI connectors.

Product Folder Links: *TS3DV642*
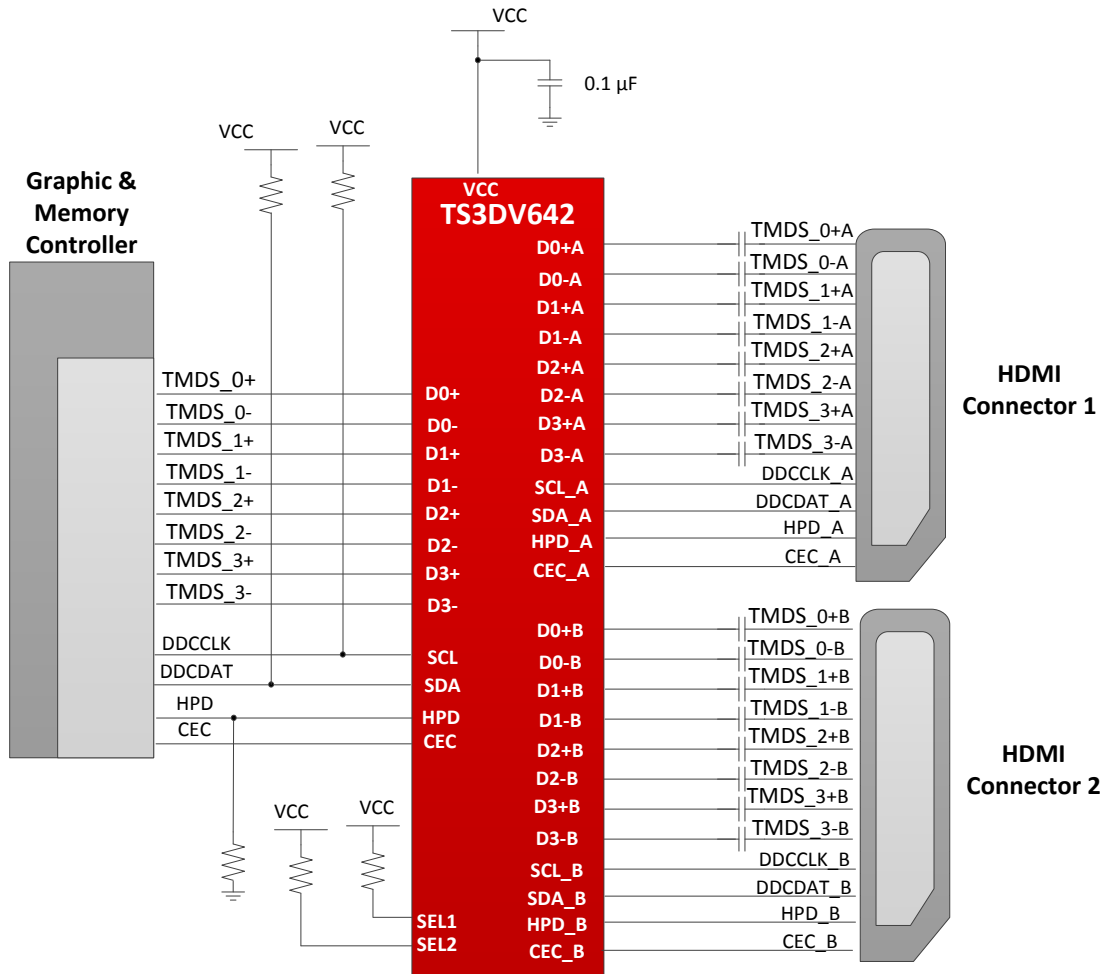
Figure 27. HDMI Application Schematic

9.2.3.1 Design Requirements

Table 4. Design Parameters for HDMI Application

Design parameter	Example value
V_{CC}	2.6 V to 4.5 V
VCC decoupling capacitor	0.1 µF
DDC Pull-up resistors	2 kΩ to 5 V
Pull-up / Pull-down resistors for SEL1 / SEL2 pins	10 kΩ
HPD Pull-down resistor	100 kΩ

9.2.3.2 Detailed Design Procedure

The TS3DV642 is designed to operate with 2.6 V – 4.5 V power supply. The wide power supply range allows flexibility for battery powered applications. If a higher power supply is used in the system, a voltage regulator can be used to bring down the voltage to 2.6 V – 4.5 V range. Decoupling capacitors may be used to reduce noise and improve power supply integrity. Pull-up resistors to 5 V must be placed on the source side DDC clock and data lines according to the HDMI standard. A weak pull-down resistor must be placed on the source side HPD line.

9.2.3.3 Application Curves
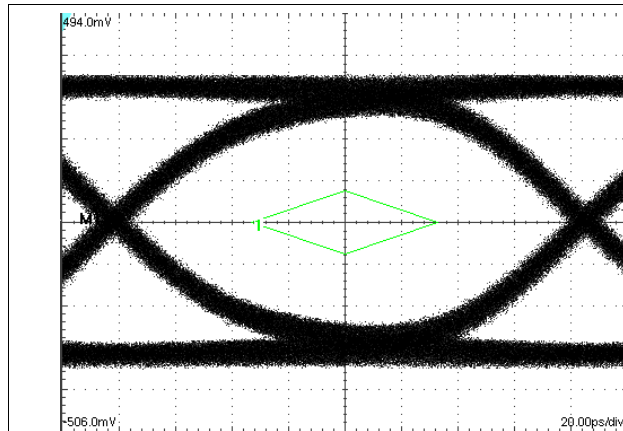
Figure 28. Eye Pattern: 6.0 Gbps Port A, D1+ to D1+A, D1- to D1-A (Only One Channel Measured at a Time)
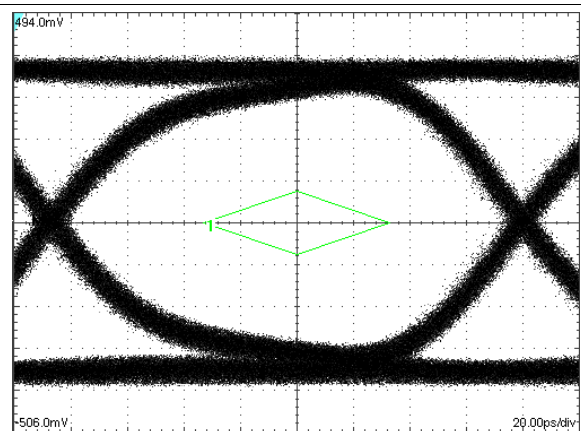
Figure 29. Eye Pattern: 6.0 Gbps, No Device Through Path (Only One Channel Measured at a Time)

10 Power Supply Recommendations

V_{CC} should be in the range of 2.6 V to 4.5 V. Voltage levels above those listed in the Absolute Ratings table should not be used. Decoupling capacitors may be used to reduce noise and improve power supply integrity. There are no power sequence requirements for the TS3DV642.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, the following commonly used printed-circuit board layout guidelines are recommended:

- Decoupling capacitors should be used between power supply pin and ground pin to ensure low impedance to reduce noise To achieve a low impedance over a wide frequency range use capacitors with a high self-resonance frequency.
- ESD and EMI protection devices (if used) should be placed as close as possible to the connector.
- Short trace lengths should be used to avoid excessive loading.
- To minimize the effects of crosstalk on adjacent traces, keep the traces at least two times the trace width apart.
- Separate high-speed signals from low-speed signals and digital from analog signals
- Avoid right-angle bends in a trace and try to route them at least with two 45° corners.
- The high-speed differential signal traces should be routed parallel to each other as much as possible. The traces are recommended to be symmetrical.
- A solid ground plane should be placed next to the high-speed signal layer. This also provides an excellent low-inductance path for the return current flow.

11.2 Layout Example

TS3DV642 application with a single controller interfacing with two HDMI connectors.

Layout Example (continued)
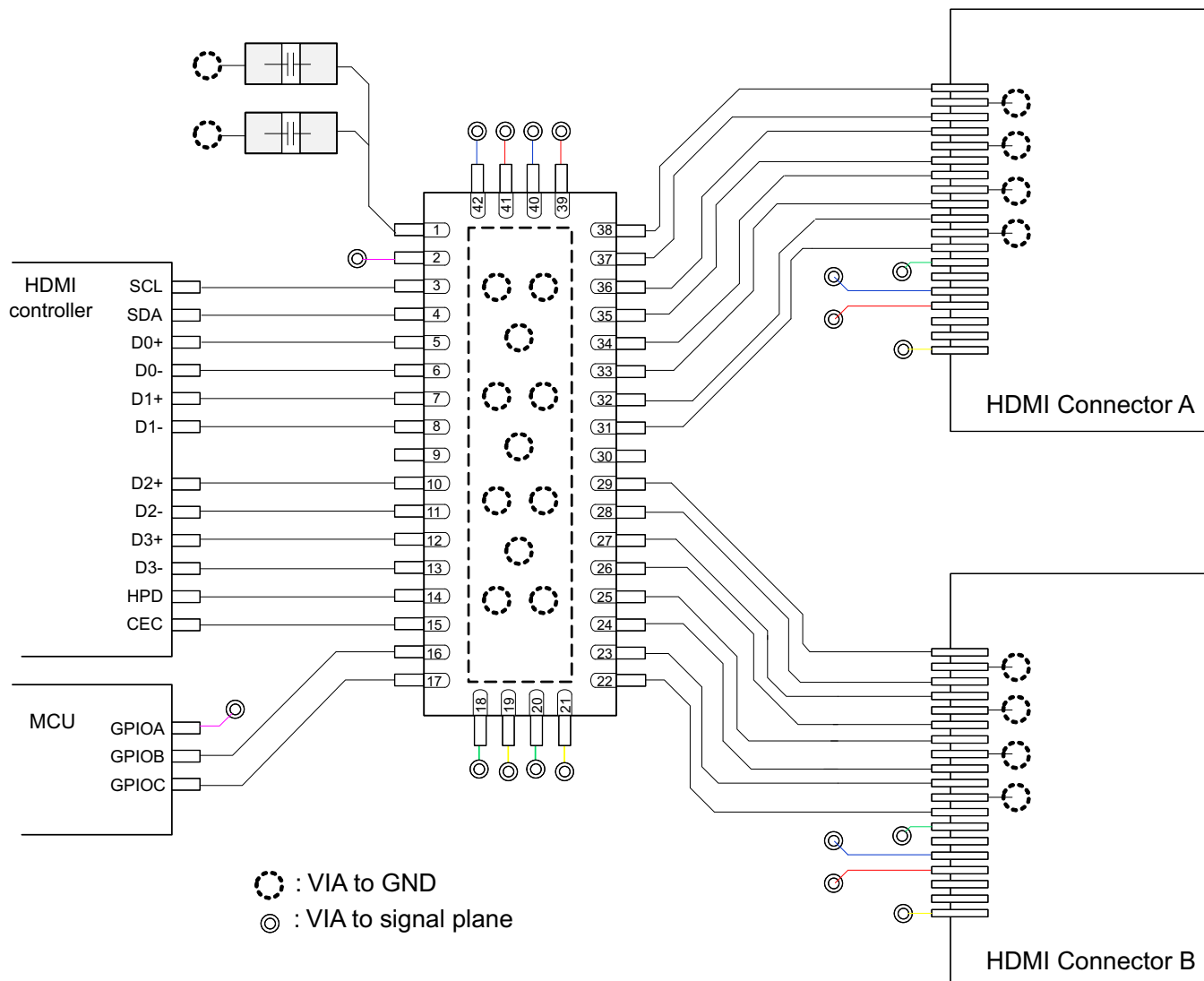
Figure 30. Layout Example

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12 Device and Documentation Support

12.1 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TS3DV642*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DV642A0RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		SD642A0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV642A0RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV642A0RUAR	WQFN	RUA	42	3000	367.0	367.0	38.0

RUA (R–PWQFN–N42)   PLASTIC QUAD FLATPACK NO–LEAD

Pin 1 Index Area

$\frac{9,10}{8,90}$

A

B

$\frac{3,60}{3,40}$

38   39   42   1   22   21   18   17

$\frac{0,80}{0,70}$

0,20 Nominal
Lead Frame

Seating Plane

$\frac{0,05}{0,00}$

0,08 C

C

0,50

1,50

THERMAL PAD
SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

$42X \frac{0,50}{0,30}$

$42X \frac{0,30}{0,20}$

⊕	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		

Bottom View

4208351/C 06/11
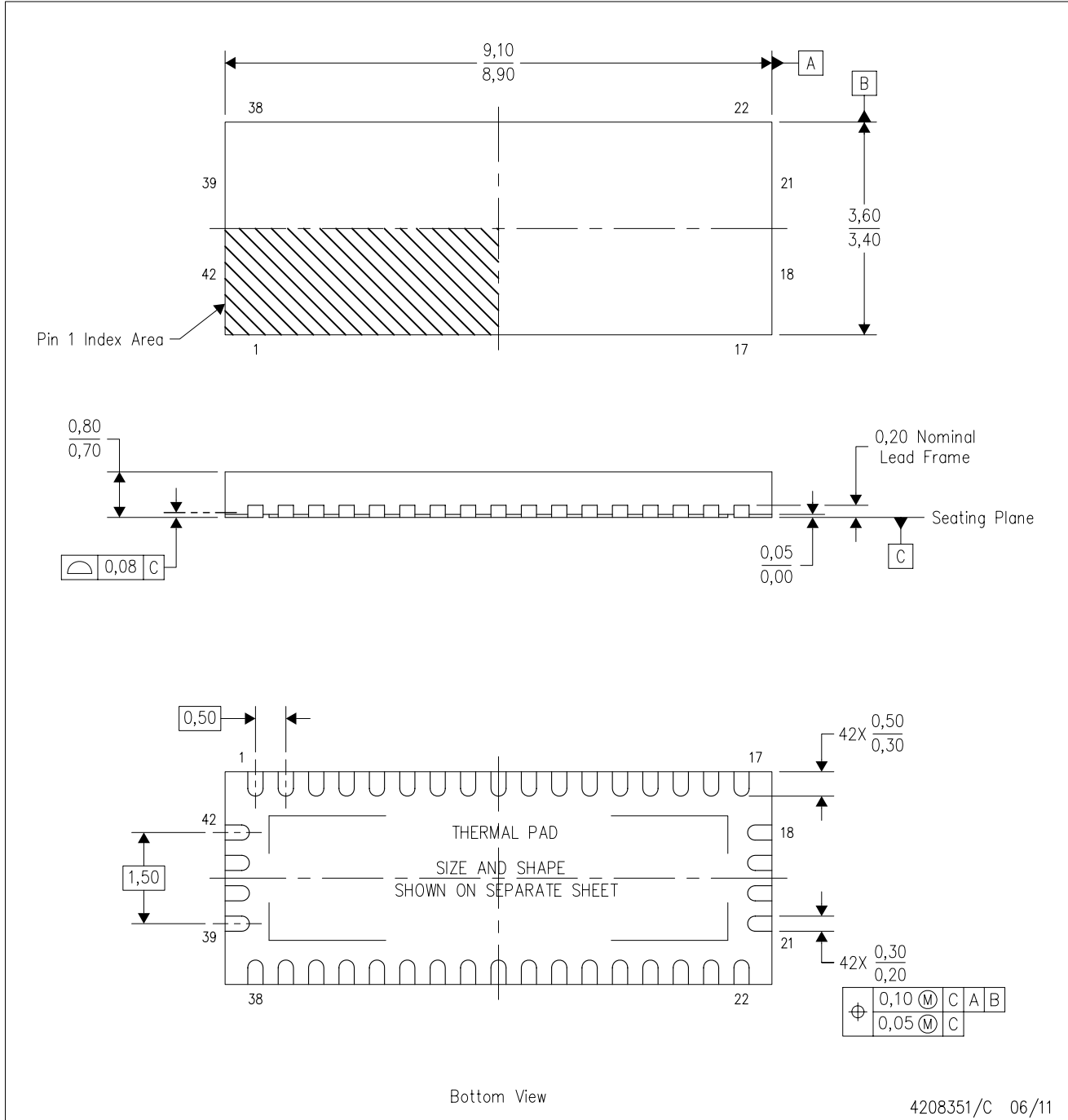
NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M–1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No–Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

RUA (R−PWQFN−N42)　　　　　　　PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Bottom View
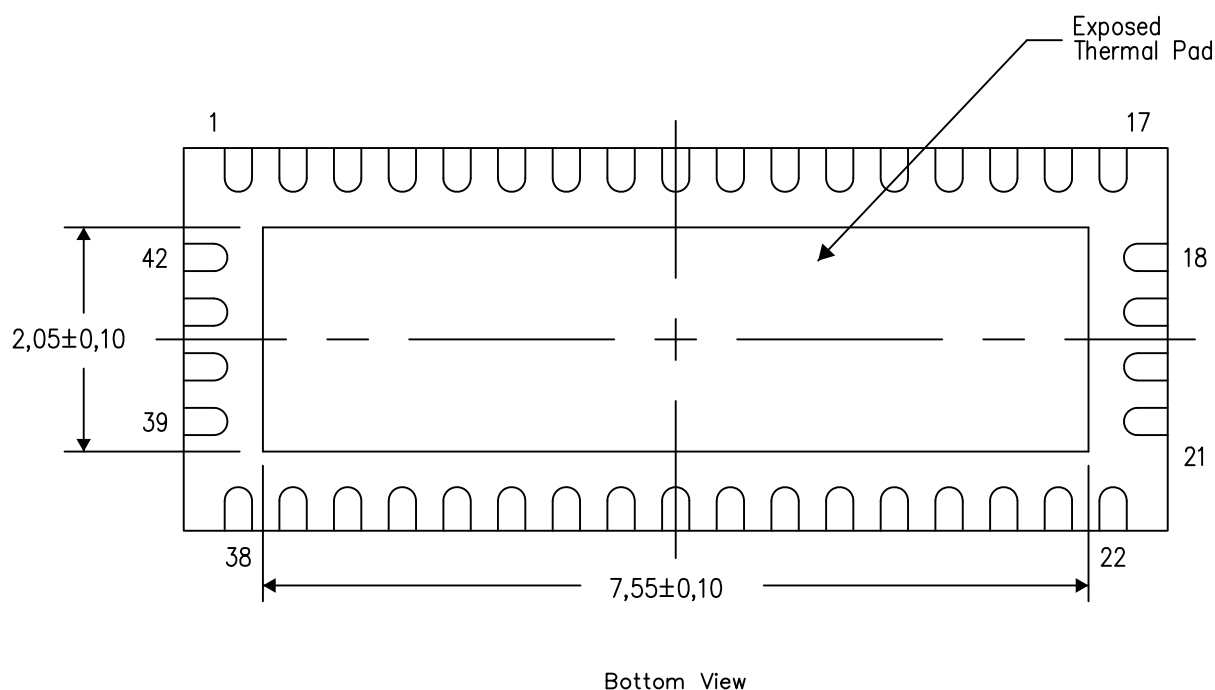
Exposed Thermal Pad Dimensions

4208352/E 01/13

NOTE:　All linear dimensions are in millimeters

RUA (R−PWQFN−N42)   PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Example Stencil Design
0,125 Thick Stencil
(Note E)

Note D

38x0,5

2,6 4,3

8,1

9,8

0,8

0,25 0,25

38x0,5

2,65 4,25

12x0,8

0,25

12x1,0

8,15

9,75

(62% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

R0,15

0,08

0,85

Example
Solder Mask Opening
(Note F)

0,07
All Around

0,30

Pad Geometry
(Note C)

14xØ0,3

7,55

1,0

0,5

2,05

0,75

1,5

4210129/D 01/13
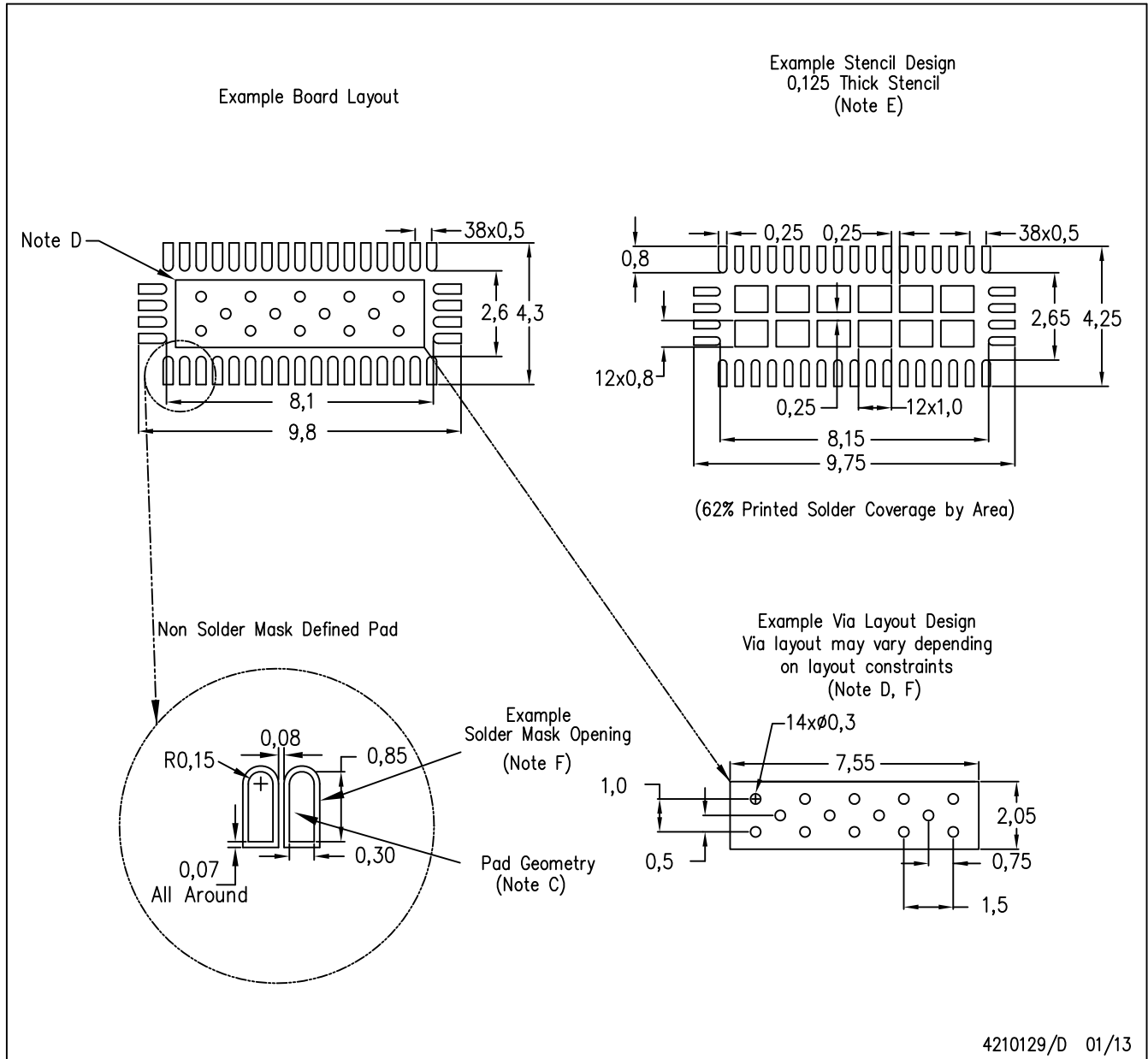
NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat−Pack
              Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout. These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE