

SN74AVCH16T245 16-Bit Dual-Supply Bus Transceiver with Configurable Level-Shifting / Voltage Translation and Tri-State Outputs

1 Features

- V_{CC} Isolation Feature – If Either V_{CC} Input is at GND, Both Ports are in the High-Impedance State
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Overvoltage-Tolerant Inputs and Outputs Allow Mixed Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2 V to 3.6 V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- I/Os are 4.6 V Tolerant
- Bus Hold on Data Inputs Eliminates the Need for External Pullup and Pulldown Resistors
- Maximum Data Rates
 - 380 Mbps (1.8 V to 3.3 V Level-Shifting)
 - 200 Mbps (<1.8 V to 3.3 V Level-Shifting)
 - 200 Mbps (Level-Shifting to 2.5 V or 1.8 V)
 - 150 Mbps (Level-Shifting to 1.5 V)
 - 100 Mbps (Level-Shifting to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 8000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

3 Description

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVCH16T245 device is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. The device is operational with V_{CCA}/V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVCH16T245	TSSOP (48)	12.50 mm × 6.10 mm
	TVSOP (48)	9.70 mm × 4.40 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

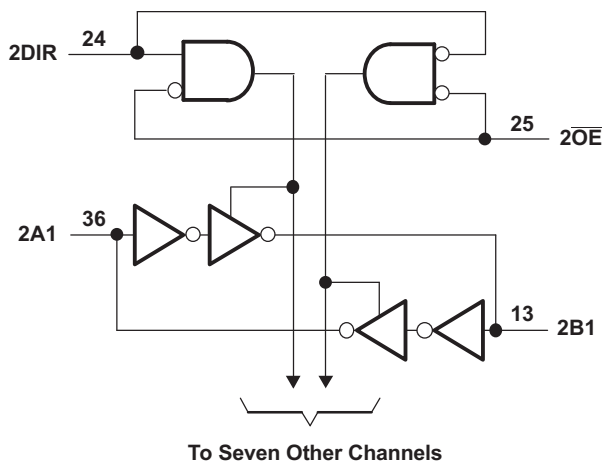
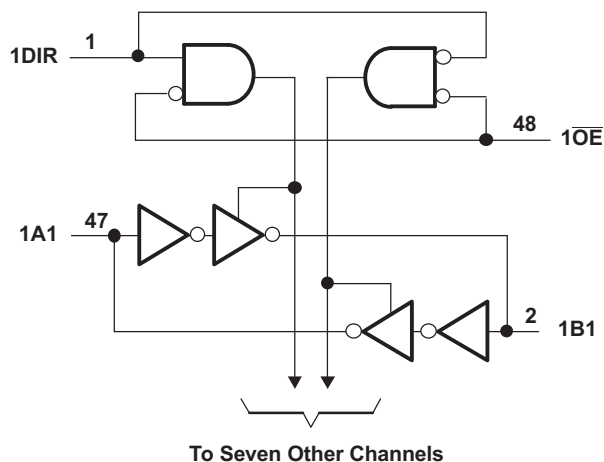


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2015) to Revision D	Page
• Updated Pin Functions table.	4

Changes from Revision B (May 2006) to Revision C	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

5 Description (continued)

The SN74AVCH16T245 control pins (1DIR, 2DIR, $\overline{1OE}$, and $\overline{2OE}$) are supplied by V_{CCA} .

The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. This device is fully specified for partial-power-down applications using I_{off} .

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

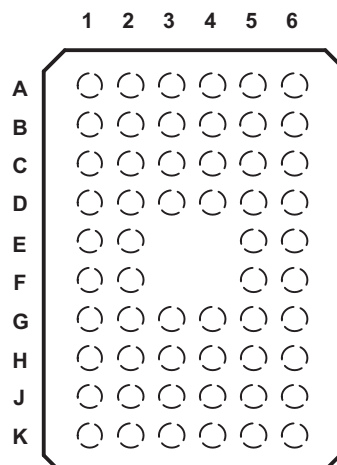
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

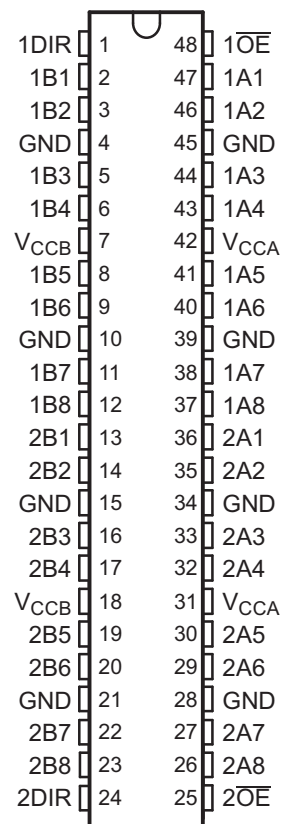
The SN74AVCH16T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the outputs so the buses are effectively isolated.

6 Pin Configuration and Functions

GQL or ZQL Package
56-Pin BGA MICROSTAR JUNIOR
Top View



DGG or DGV Package
48-Pin TSSOP or TVSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TSSOP TVSOP	BGA MICROSTAR		
1DIR, 2DIR	1, 24	A1, K1	I	Direction-control signal
1B1 to 1B8	2, 3, 5, 6, 8, 9, 11, 12	B2, B1, C2, C1, D2, D1, E2, E1	I/O	Input/Output. Referenced to V_{CCB}
2B1 to 2B8	13, 14, 16, 17, 19, 20, 22, 23	F1, F2, G1, G2, H1, H2, J1, J2	I/O	Input/Output. Referenced to V_{CCB}
GND	4, 10, 15, 21, 45, 39, 34, 28	B3, D3, G3, J3, J4, G4, D4, B4	—	Ground
V_{CCB}	7, 18	C3, H3	—	B-port supply voltage. $1.2\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$
$\overline{1OE}$, $\overline{2OE}$	48, 25	A6, K6	—	Tri-State output-mode enables. Pull \overline{OE} high to place all outputs in Tri-State mode. Referenced to V_{CCA}
1A1 to 1A8	47, 46, 44, 43, 41, 40, 38, 37	B5, B6, C5, C6, D5, D6, E5, E6	I/O	Input/Output. Referenced to V_{CCA}
2A1 to 2A8	36, 35, 33, 32, 30, 29, 27, 26	F6, F5, G6, G5, H6, H5, J6, J5	I/O	Input/Output. Referenced to V_{CCA}
V_{CCA}	42, 31	C4, H4	—	A-port supply voltage. $1.2\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$
N.C.	—	A2, A3, A4, A5, K2, K3, K4, K5	—	No internal connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted⁽¹⁾)

		MIN	MAX	UNIT	
V_{CCA} V_{CCB}	Supply voltage	-0.5	4.6	V	
V_I	Input voltage ⁽²⁾	I/O ports (A port)	-0.5	4.6	V
		I/O ports (B port)	-0.5	4.6	
		Control inputs	-0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A port	-0.5	4.6	V
		B port	-0.5	4.6	
V_O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$	-50	mA	
I_{OK}	Output clamp current	$V_O < 0$	-50	mA	
I_O	Continuous output current		±50	mA	
	Continuous current through each V_{CCA} , V_{CCB} , and GND		±100	mA	
T_J	Junction temperature	-40	150	°C	
T_{stg}	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage (V_I) and output negative-voltage (V_O) ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

7.2 ESD Ratings

		VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
		Machine model (A115-A)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

		V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage			1.2	3.6	V
V_{CCB}	Supply voltage			1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs ⁽⁴⁾	1.2 V to 1.95 V	$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V	1.6		
			2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	Data inputs ⁽⁴⁾	1.2 V to 1.95 V	$V_{CCI} \times 0.35$		V
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA}) ⁽⁵⁾	1.2 V to 1.95 V	$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V	1.6		
			2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA}) ⁽⁵⁾	1.2 V to 1.95 V	$V_{CCA} \times 0.35$		V
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
V_I	Input voltage			0	3.6	V
V_O	Output voltage	Active state		0	V_{CCO}	V
		Tri-State		0	3.6	
I_{OH}	High-level output current		1.2 V	-3		mA
			1.4 V to 1.6 V	-6		
			1.65 V to 1.95 V	-8		
			2.3 V to 2.7 V	-9		
			3 V to 3.6 V	-12		
I_{OL}	Low-level output current		1.2 V	3		mA
			1.4 V to 1.6 V	6		
			1.65 V to 1.95 V	8		
			2.3 V to 2.7 V	9		
			3 V to 3.6 V	12		
$\Delta t/\Delta v$	Input transition rise or fall rate				5	ns/V
T_A	Operating free-air temperature			-40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7$ V, V_{IL} max = $V_{CCI} \times 0.3$ V.

(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7$ V, V_{IL} max = $V_{CCA} \times 0.3$ V.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AVCH16T245			UNIT	
	TSSOP (DGG)	TVSOP (DGV)	ZQL/GQL (BGA MICROSTAR JUNIOR)		
	48 PINS	48 PINS	56 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.5	69.9	64.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.2	23.9	16.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.1	36.6	30.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	1.7	0.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.6	36.2	64.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS		V _{CCA}	V _{CCB}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V _{OH}		V _I = V _{IH}	1.2 V to 3.6 V	1.2 V to 3.6 V				V _{CCO} - 0.2		V
			1.2 V	1.2 V	0.95					
			1.4 V	1.4 V		1.05				
			1.65 V	1.65 V		1.2				
			2.3 V	2.3 V		1.75				
			3 V	3 V		2.3				
V _{OL}		V _I = V _{IL}	1.2 V to 3.6 V	1.2 V to 3.6 V				0.2		V
			1.2 V	1.2 V	0.15					
			1.4 V	1.4 V		0.35				
			1.65 V	1.65 V		0.45				
			2.3 V	2.3 V		0.55				
			3 V	3 V		0.7				
I _I	Control inputs	V _I = V _{CCA} or GND	1.2 V to 3.6 V	1.2 V to 3.6 V	±0.025	±0.25		±1	µA	
I _{BHL} ⁽³⁾		V _I = 0.42 V	1.2 V	1.2 V	25				µA	
		V _I = 0.49 V	1.4 V	1.4 V			15			
		V _I = 0.58 V	1.65 V	1.65 V			25			
		V _I = 0.7 V	2.3 V	2.3 V			45			
		V _I = 0.8 V	3.3 V	3.3 V			100			
I _{BHH} ⁽⁴⁾		V _I = 0.78 V	1.2 V	1.2 V	-25				µA	
		V _I = 0.91 V	1.4 V	1.4 V			-15			
		V _I = 1.07 V	1.65 V	1.65 V			-25			
		V _I = 1.6 V	2.3 V	2.3 V			-45			
		V _I = 2 V	3.3 V	3.3 V			-100			
I _{BHLO} ⁽⁵⁾		V _I = 0 to V _{CC}	1.2 V	1.2 V	50				µA	
			1.6 V	1.6 V			125			
			1.95 V	1.95 V			200			
			2.7 V	2.7 V			300			
			3.6 V	3.6 V			500			
I _{BHHO} ⁽⁶⁾		V _I = 0 to V _{CC}	1.2 V	1.2 V	-50				µA	
			1.6 V	1.6 V			-125			
			1.95 V	1.95 V			-200			
			2.7 V	2.7 V			-300			
			3.6 V	3.6 V			-500			
I _{off}	A port	V _I or V _O = 0 to 3.6 V	0 V	0 to 3.6 V	±0.1	±2.5		±5	µA	
	B port		0 to 3.6 V	0 V	±0.1	±2.5		±5		
I _{OZ} ⁽⁷⁾	A or B port	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	$\overline{OE} = V_{IH}$	3.6 V	3.6 V	±0.5	±2.5		±5	µA
	B port		$\overline{OE} = \text{don't care}$	0 V	3.6 V				±5	
	A port			3.6 V	0 V				±5	
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				25	µA	
			0 V	3.6 V				-5		
			3.6 V	0 V				25		

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

(5) An external driver must source at least I_{BHLO} to switch this node from low to high.

(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

(7) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Electrical Characteristics (continued)

 over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			T _A = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
I _{CCB}	V _I = V _{CC1} or GND, I _O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				25		μA
		0 V	3.6 V				25		
		3.6 V	0 V				-5		
I _{CCA} + I _{CCB}	V _I = V _{CC1} or GND, I _O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V				45		μA
C _i	Control inputs V _I = 3.3 V or GND	3.3 V	3.3 V		3.5				pF
C _{io}	A or B port V _O = 3.3 V or GND	3.3 V	3.3 V		7				pF

7.6 Switching Characteristics: V_{CCA} = 1.2 V

 over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2 V	V _{CCB} = 1.5 V	V _{CCB} = 1.8 V	V _{CCB} = 2.5 V	V _{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t _{PLH}	A	B	4.1	3.3	3	2.8	3.2	ns
t _{PHL}			4.1	3.3	3	2.8	3.2	
t _{PLH}	B	A	4.4	4	3.8	3.6	3.5	ns
t _{PHL}			4.4	4	3.8	3.6	3.5	
t _{PZH}	$\overline{\text{OE}}$	A	6.4	6.4	6.4	6.4	6.4	ns
t _{PZL}			6.4	6.4	6.4	6.4	6.4	
t _{PZH}	$\overline{\text{OE}}$	B	6	4.6	4	3.4	3.2	ns
t _{PZL}			6	4.6	4	3.4	3.2	
t _{PHZ}	$\overline{\text{OE}}$	A	6.6	6.6	6.6	6.6	6.8	ns
t _{PLZ}			6.6	6.6	6.6	6.6	6.8	
t _{PHZ}	$\overline{\text{OE}}$	B	6	4.9	4.9	4.2	5.3	ns
t _{PLZ}			6	4.9	4.9	4.2	5.3	

7.7 Switching Characteristics: $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	ns
t_{PHL}			3.6	0.5	6.2	0.5	5.2	0.5	4.1	0.5	3.7	
t_{PLH}	B	A	3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	ns
t_{PHL}			3.3	0.5	6.2	0.5	5.9	0.5	5.6	0.5	5.5	
t_{PZH}	\overline{OE}	A	4.3	1	10.1	1	10.1	1	10.1	1	10.1	ns
t_{PZL}			4.3	1	10.1	1	10.1	1	10.1	1	10.1	
t_{PZH}	\overline{OE}	B	5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	ns
t_{PZL}			5.6	1	10.1	0.5	8.1	0.5	5.9	0.5	5.2	
t_{PHZ}	\overline{OE}	A	4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	ns
t_{PLZ}			4.5	1.5	9.1	1.5	9.1	1.5	9.1	1.5	9.1	
t_{PHZ}	\overline{OE}	B	5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	ns
t_{PLZ}			5.5	1.5	8.7	1.5	7.5	1	6.5	1	6.3	

7.8 Switching Characteristics: $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	ns
t_{PHL}			3.4	0.5	5.9	0.5	4.8	0.5	3.7	0.5	3.3	
t_{PLH}	B	A	3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	ns
t_{PHL}			3	0.5	5.2	0.5	4.8	0.5	4.5	0.5	4.4	
t_{PZH}	\overline{OE}	A	3.4	1	7.8	1	7.8	1	7.8	1	7.8	ns
t_{PZL}			3.4	1	7.8	1	7.8	1	7.8	1	7.8	
t_{PZH}	\overline{OE}	B	5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	ns
t_{PZL}			5.4	1	9.2	0.5	7.4	0.5	5.3	0.5	4.5	
t_{PHZ}	\overline{OE}	A	4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	ns
t_{PLZ}			4.2	1.5	7.7	1.5	7.7	1.5	7.7	1.5	7.7	
t_{PHZ}	\overline{OE}	B	5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	ns
t_{PLZ}			5.2	1.5	8.4	1.5	7.1	1	5.9	1	5.7	

7.9 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

 over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	ns
t_{PHL}			3.2	0.5	5.6	0.5	4.5	0.5	3.3	0.5	2.8	
t_{PLH}	B	A	2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	ns
t_{PHL}			2.6	0.5	4.1	0.5	3.7	0.5	3.3	0.5	3.2	
t_{PZH}	\overline{OE}	A	2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
t_{PZL}			2.5	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	
t_{PZH}	\overline{OE}	B	5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	ns
t_{PZL}			5.2	0.5	9.4	0.5	7.3	0.5	5.1	0.5	4.5	
t_{PHZ}	\overline{OE}	A	3	1	6.1	1	6.1	1	6.1	1	6.1	ns
t_{PLZ}			3	1	6.1	1	6.1	1	6.1	1	6.1	
t_{PHZ}	\overline{OE}	B	5	1	7.9	1	6.6	1	6.1	1	5.2	ns
t_{PLZ}			5	1	7.9	1	6.6	1	6.1	1	5.2	

7.10 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

 over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	ns
t_{PHL}			3.2	0.5	5.5	0.5	4.4	0.5	3.2	0.5	2.7	
t_{PLH}	B	A	2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	ns
t_{PHL}			2.8	0.5	3.7	0.5	3.3	0.5	2.8	0.5	2.7	
t_{PZH}	\overline{OE}	A	2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	ns
t_{PZL}			2.2	0.5	4.3	0.5	4.2	0.5	4.1	0.5	4	
t_{PZH}	\overline{OE}	B	5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	ns
t_{PZL}			5.1	0.5	9.3	0.5	7.2	0.5	4.9	0.5	4	
t_{PHZ}	\overline{OE}	A	3.4	0.5	5	0.5	5	0.5	5	0.5	5	ns
t_{PLZ}			3.4	0.5	5	0.5	5	0.5	5	0.5	5	
t_{PHZ}	\overline{OE}	B	4.9	1	7.7	1	6.5	1	5.2	0.5	5	ns
t_{PLZ}			4.9	1	7.7	1	6.5	1	5.2	0.5	5	

7.11 Operating Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.2\text{ V}$	$V_{CCA} = V_{CCB} = 1.5\text{ V}$	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	$V_{CCA} = V_{CCB} = 2.5\text{ V}$	$V_{CCA} = V_{CCB} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
$C_{pdA}^{(1)}$	A to B	Outputs enabled	$C_L = 0,$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$	1	1	1	1	2	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		13	13	14	15	16	
		Outputs disabled		1	1	1	1	1	
$C_{pdB}^{(1)}$	A to B	Outputs enabled		13	13	14	15	16	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	1	2	
		Outputs disabled		1	1	1	1	1	

(1) Power dissipation capacitance per transceiver. Refer to the TI application report, *CMOS Power Consumption and Cpd Calculation*, [SCAA035](#)

7.12 Typical Characteristics ($T_A = 25^\circ\text{C}$)

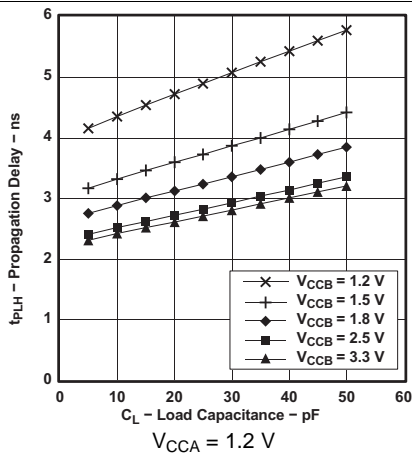


Figure 1. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

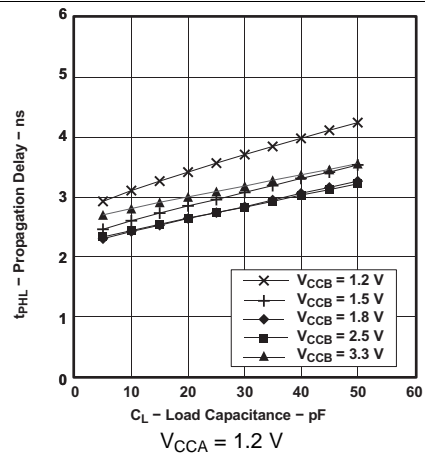


Figure 2. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

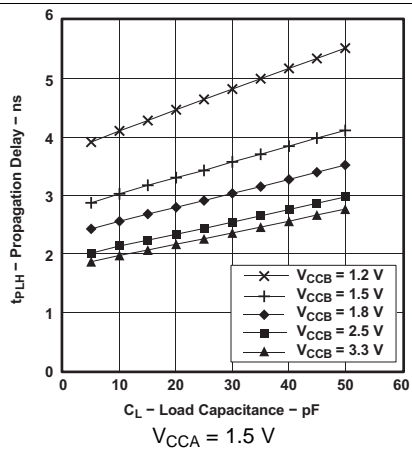


Figure 3. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

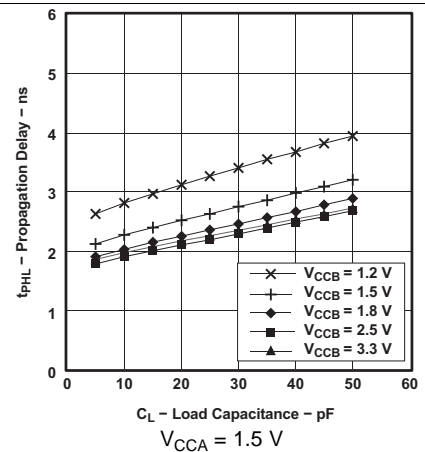


Figure 4. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

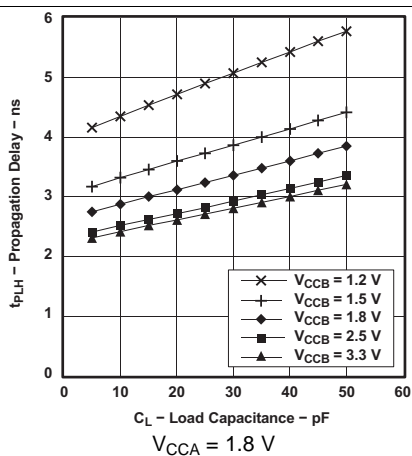


Figure 5. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

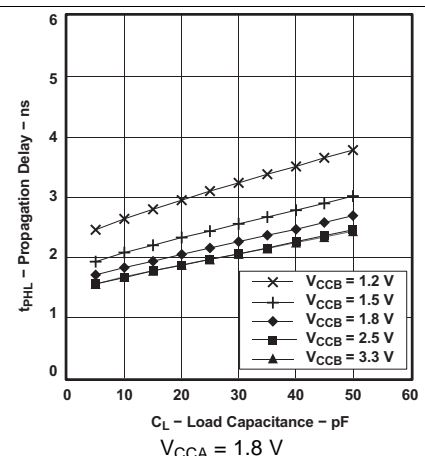


Figure 6. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

Typical Characteristics ($T_A = 25^\circ\text{C}$) (continued)

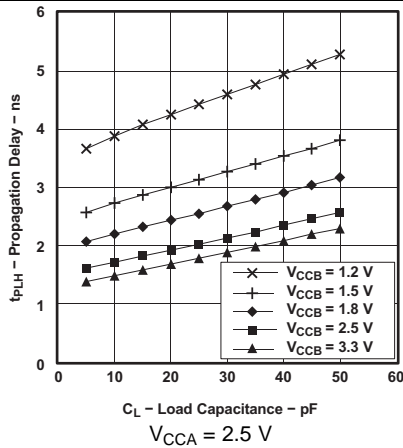


Figure 7. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

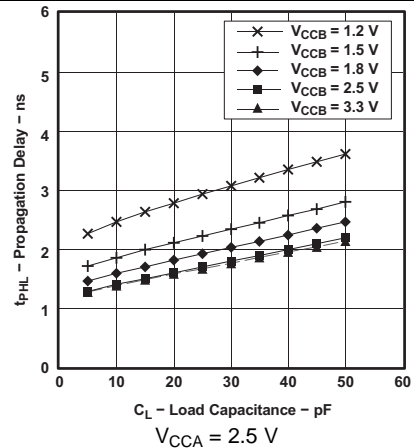


Figure 8. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

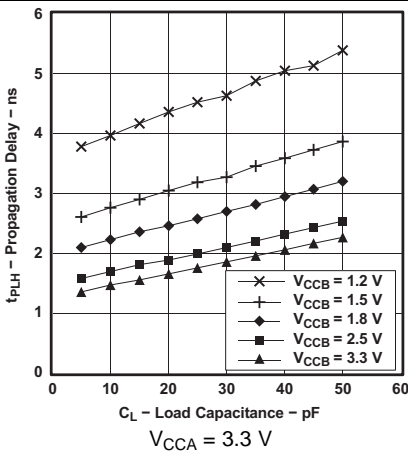


Figure 9. Typical Propagation Delay t_{PLH} (A to B) vs Load Capacitance

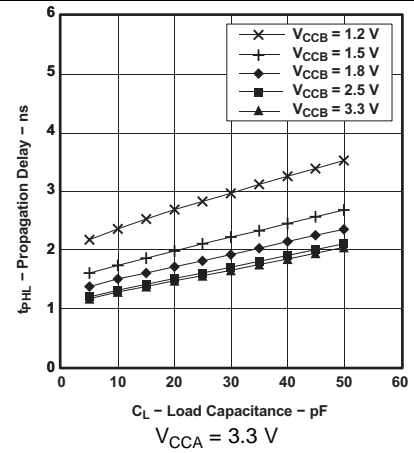
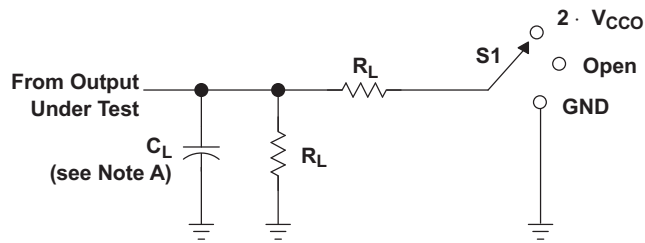


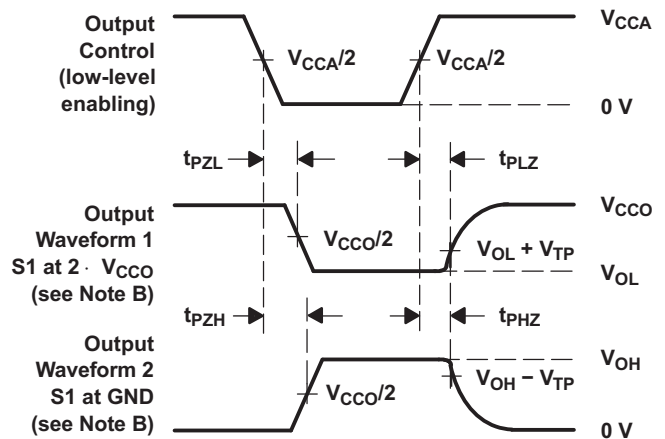
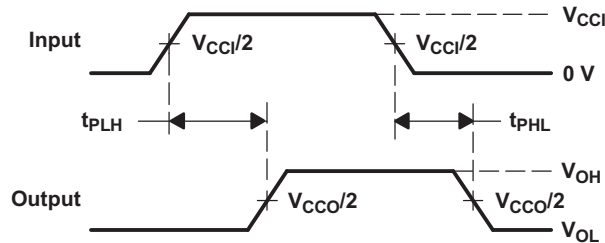
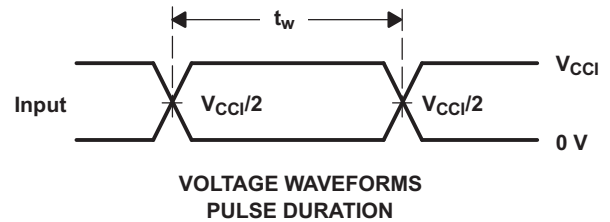
Figure 10. Typical Propagation Delay t_{PHL} (A to B) vs Load Capacitance

8 Parameter Measurement Information


LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CCO}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CCI} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.

Figure 11. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

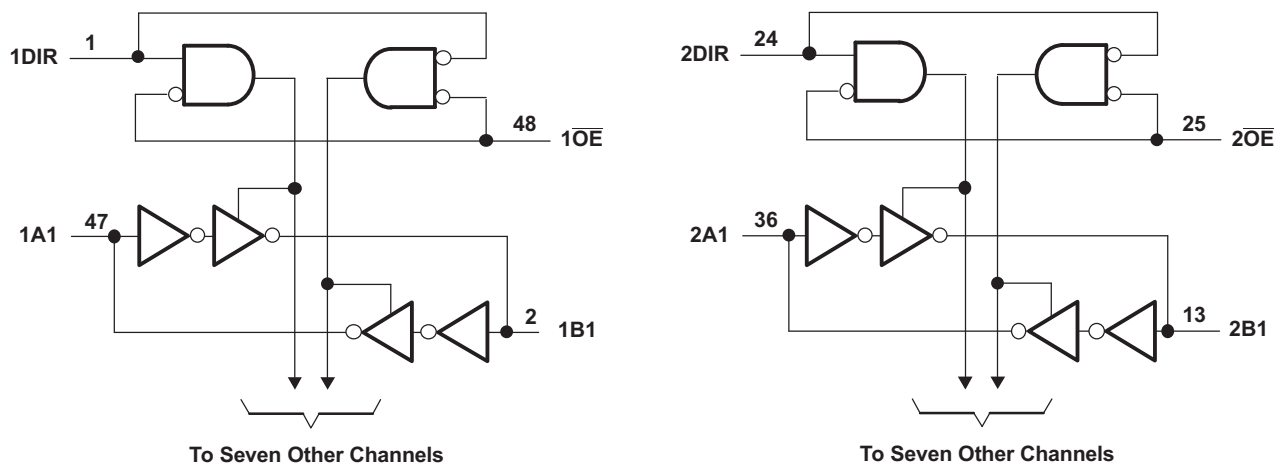
The SN74AVCH16T245 is a 16-bit, dual-supply noninverting bidirectional voltage level translation. Pins A and control pins (DIR and \overline{OE}) are supported by V_{CCA} and pins B are supported by V_{CCB} . The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when \overline{OE} is set to low. When \overline{OE} is set to high, both A and B are in the high-impedance state.

SN74AVCH16T245 features Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using off output current (I_{off}).

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are put in a high-impedance state.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2 V to 3.6 V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.2 V to 3.6 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

9.3.2 Partial-Power-Down Mode Operation

The I_{off} circuitry will prevent backflow current by disabling I/O output circuits when device is in partial power-down mode. This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.3.3 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports will be in a high-impedance state (I_{OZ} shown in [Electrical Characteristics](#)). This prevents false logic levels from being presented to either bus.

9.4 Device Functional Modes

The SN74AVCH16T245 is a voltage level translator that can operate from 1.2 V to 3.6 V (V_{CCA}) and 1.2 V to 3.6 V (V_{CCB}). The signal translation between 1.2 V and 3.6 V requires direction control and output enable control. When \overline{OE} is low and DIR is high, data transmission is from A to B. When \overline{OE} is low and DIR is low, data transmission is from B to A. When \overline{OE} is high, both output ports will be high-impedance.

**Table 1. Function Table
(Each Transceiver)**

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Table 2. Typical Total Static Power Consumption ($I_{CCA} + I_{CCB}$)

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	< 0.5	< 0.5	< 0.5	< 0.5	< 0.5	μA
1.2 V	< 0.5	< 1	< 1	< 1	< 1	1	
1.5 V	< 0.5	< 1	< 1	< 1	< 1	1	
1.8 V	< 0.5	< 1	< 1	< 1	< 1	< 1	
2.5 V	< 0.5	1	< 1	< 1	< 1	< 1	
3.3 V	< 0.5	1	< 1	< 1	< 1	< 1	

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AVCH16T245 device can be used in level-shifting applications for interfacing devices and addressing mixed voltage incompatibility. The SN74AVCH16T245 device is ideal for data transmission where direction is different for each channel.

10.2 Typical Application

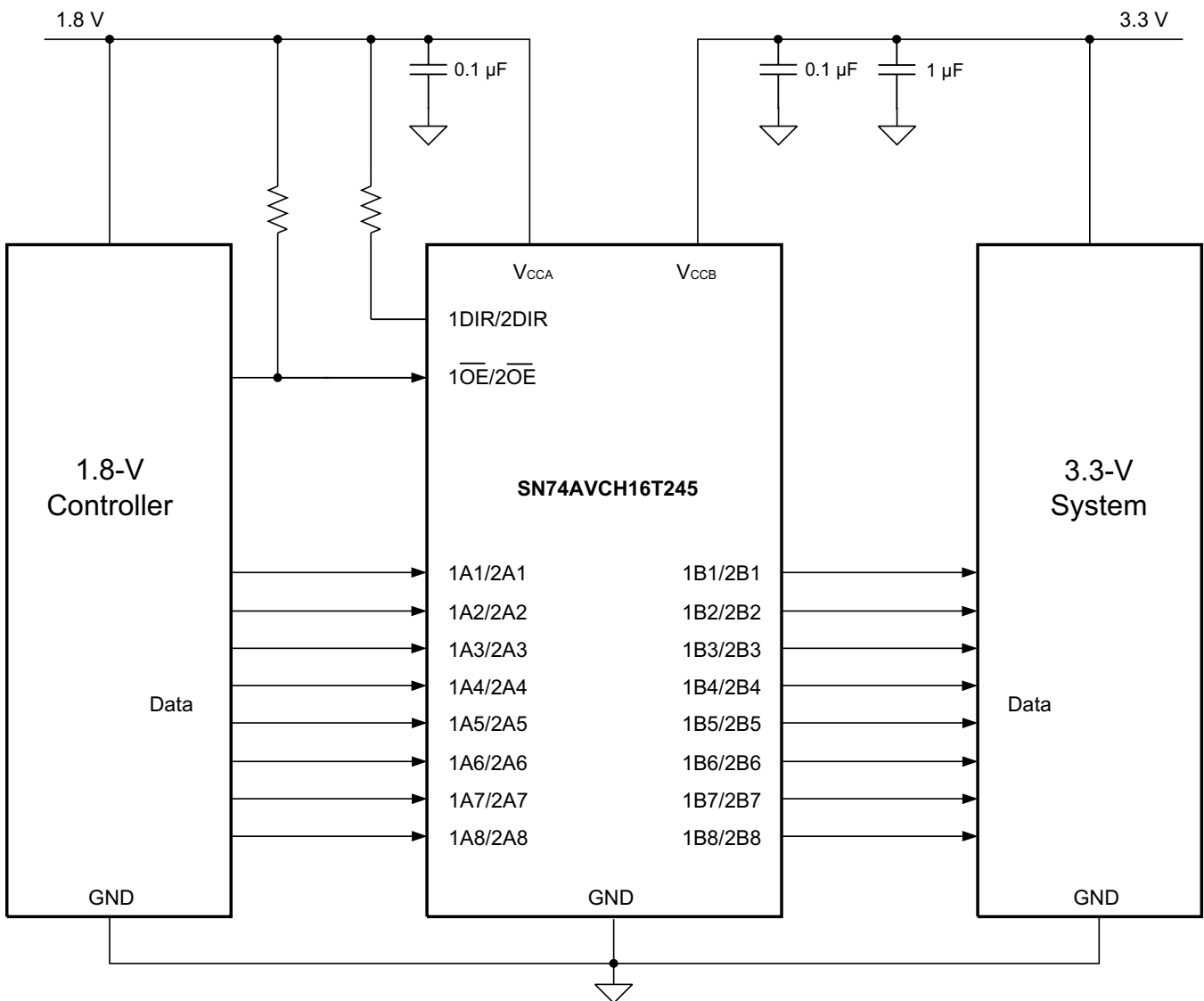


Figure 12. Typical Application Schematic

Typical Application (continued)

10.2.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs are must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Tie any unused input and output ports directly to ground.

For this design example, use the parameters listed in [Table 3](#).

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

10.2.2.1 Input Voltage Ranges

Use the supply voltage of the device that is driving the SN74AVCH16T245 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.

10.2.2.2 Output Voltage Range

Use the supply voltage of the device that the SN74AVCH16T245 device is driving to determine the output voltage range.

10.2.3 Application Curve

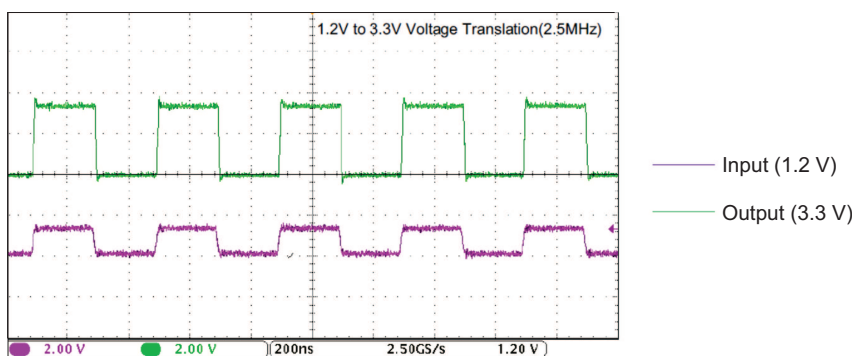


Figure 13. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74AVCH16T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB} . V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} , respectively, allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable \overline{OE} input circuit is supplied by V_{CCA} and when the \overline{OE} input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the \overline{OE} input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

12.2 Layout Example

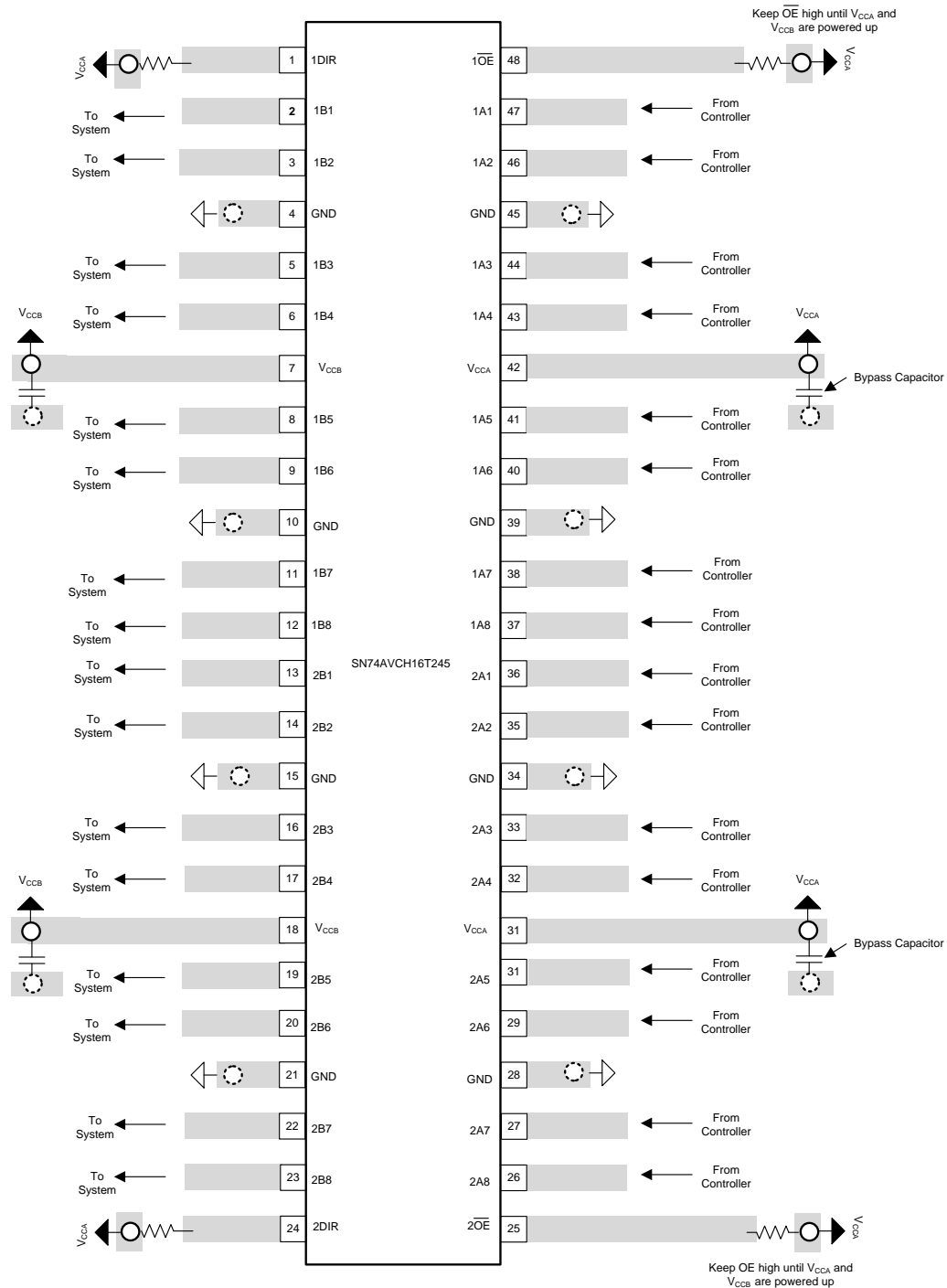
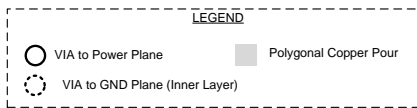


Figure 14. Recommended Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *CMOS Power Consumption and Cpd Calculation*, [SCAA035](#)
- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AVCH16T245GR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH16T245
SN74AVCH16T245GR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH16T245
SN74AVCH16T245GRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH16T245
SN74AVCH16T245GRG4.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVCH16T245
SN74AVCH16T245VR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WJ245
SN74AVCH16T245VR.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WJ245
SN74AVCH16T245VRG4	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WJ245
SN74AVCH16T245VRG4.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WJ245

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVCH16T245GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AVCH16T245GRG4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AVCH16T245VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74AVCH16T245VRG4	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVCH16T245GR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74AVCH16T245GRG4	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74AVCH16T245VR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74AVCH16T245VRG4	TVSOP	DGV	48	2000	353.0	353.0	32.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

EXAMPLE BOARD LAYOUT

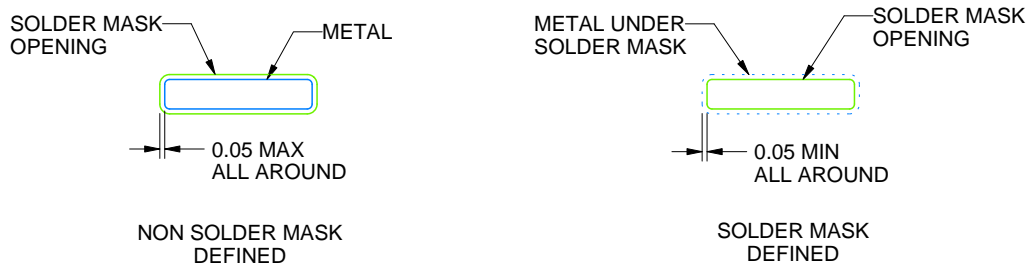
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
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 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Last updated 10/2025