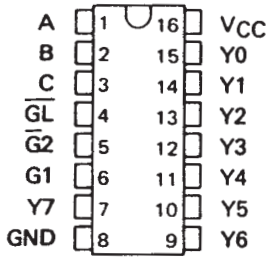
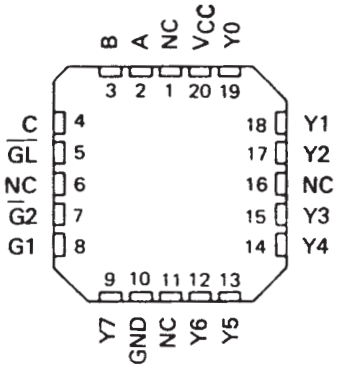
- **Combines Decoder and 3-Bit Address Latch**
- **Incorporates 2 Enable Inputs to Simplify Cascading**
- **Low Power Dissipation . . . 65 mW Typ**

**SN54LS137 . . . J OR W PACKAGE**
**SN74LS137 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54LS137 . . .FK PACKAGE**
**(TOP VIEW)**

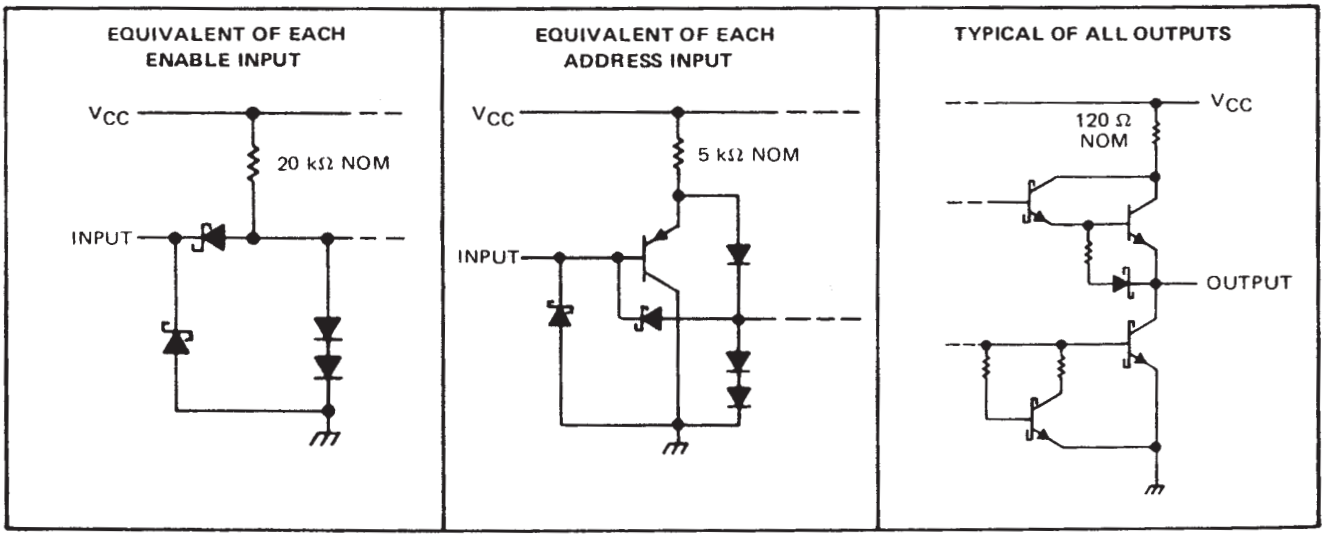



NC - No internal connection

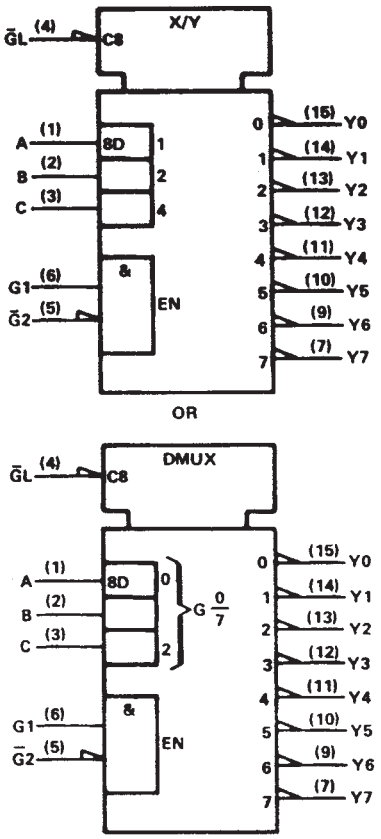
## description

The 'LS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'LS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A,B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'LS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

## schematics of inputs and outputs



## logic symbols†



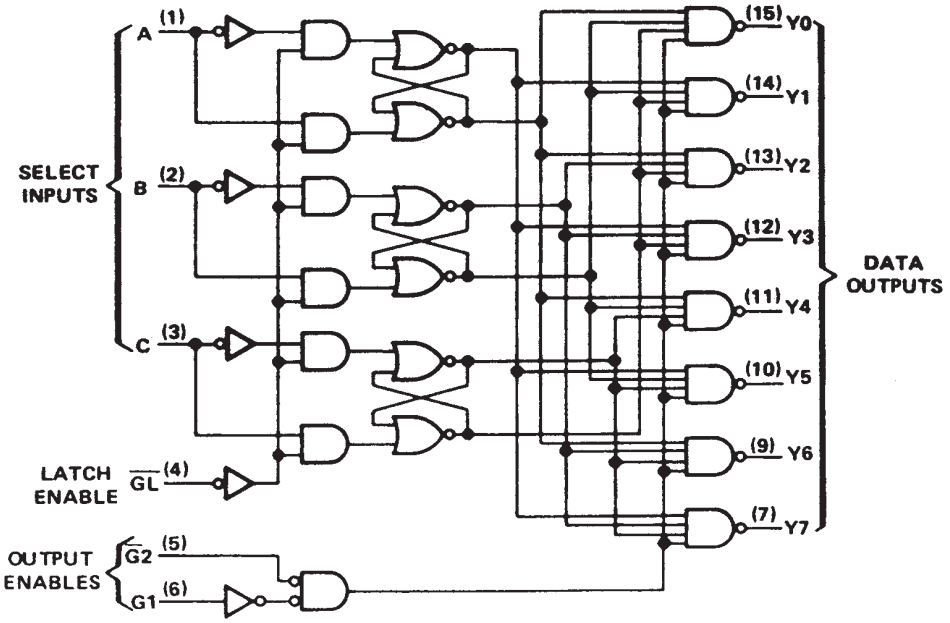

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

**FUNCTION TABLE**

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ENABLE | | | SELECT | | | | | | | | | | |
| $\overline{G1}$ | G1 | $\overline{G2}$ | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| L | H | L | L | L | L | L | H | H | H | H | H | H | H |
| L | H | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | L | H | H | L | H | H | H | H | H |
| L | H | L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | L | H | H | H | H | H | H | H | H | H | H | L |
| H | H | L | X | X | X | Output corresponding to stored address, L; all others, H | | | | | | | |

H = high level, L = low level, X = irrelevant

## logic diagram (positive logic)




Pin numbers shown are for D, J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (See Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS137 . . . . . −55°C to 125°C
SN74LS137 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | SN54LS137 | | | SN74LS137 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | –400 | | | –400 | μA |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Width of enabling pulse at $\overline{G}L$, $t_w$ | 15 | | | 15 | | | ns |
| Setup time at A, B, and C inputs, $t_{su}$ | 10 | | | 10 | | | ns |
| Hold time at A, B, and C inputs, $t_h$ | 10 | | | 10 | | | ns |
| Operating free-air temperature, $T_A$ | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54LS137 | | | SN74LS137 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = –18 mA | | | | –1.5 | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = –400 μA | | 2.5 | 3.5 | | 2.7 | 3.5 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max | $V_{IH}$ = 2 V, | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | Enable | | | –0.4 | | | –0.4 | mA |
| | | | | A, B, C | | | –0.2 | | | –0.2 | |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | | –20 | | –100 | –20 | | –100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, | See Note 2 | | | 11 | 18 | | 11 | 18 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: $I_{CC}$ is tested with all inputs grounded and all outputs open.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C, see note 3

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | LEVELS OF DELAY | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | A, B, C | Y | 2 | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | | 11 | 17 | ns |
| $t_{PHL}$ | | | 4 | | | 25 | 38 | |
| $t_{PLH}$ | A, B, C | Y | 3 | | | 16 | 24 | ns |
| $t_{PHL}$ | | | 3 | | | 19 | 29 | |
| $t_{PLH}$ | Enable $\overline{G}2$ | Y | 2 | | | 13 | 21 | ns |
| $t_{PHL}$ | | | 2 | | | 16 | 27 | |
| $t_{PLH}$ | Enable G1 | Y | 3 | | | 14 | 21 | ns |
| $t_{PHL}$ | | | 3 | | | 18 | 27 | |
| $t_{PLH}$ | Enable $\overline{G}L$ | Y | 3 | | | 18 | 27 | ns |
| $t_{PHL}$ | | | 4 | | | 25 | 38 | |

¶ $t_{PLH}$ = propagation delay time, low-to-high-level output.
$t_{PHL}$ = propagation delay time, high-to-low-level output.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN54LS137J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54LS137J | Samples |
| SNJ54LS137J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS137J | Samples |
| SNJ54LS137J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54LS137J | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

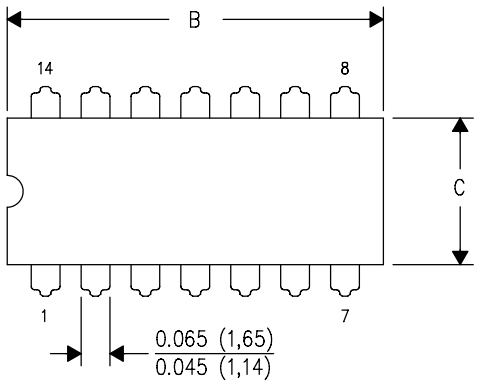
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

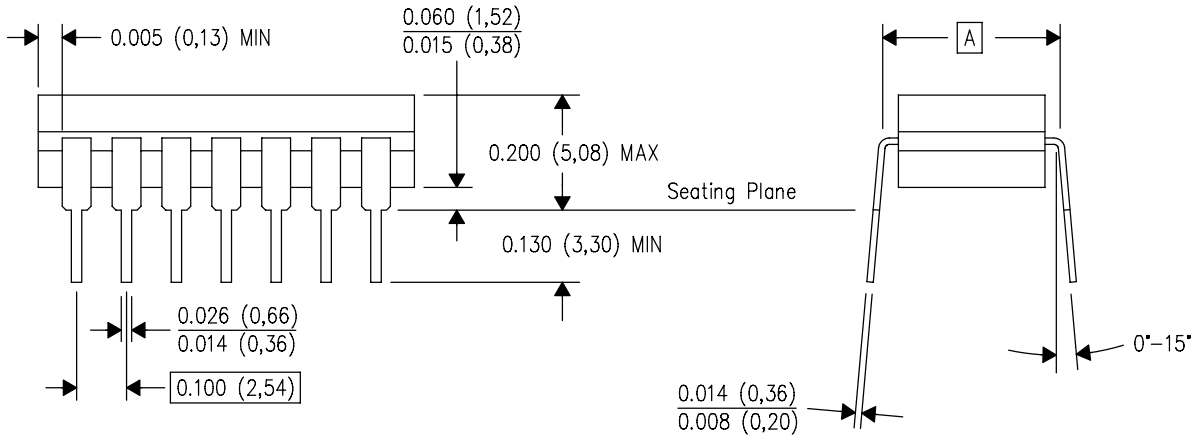
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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