

SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

SDLS195 – MARCH 1985 – REVISED MARCH 1988

'LS673

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

'LS674

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-level (\overline{CS}) input disables both the shift-register clock and the storage register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

SN54LS674, SN74LS674

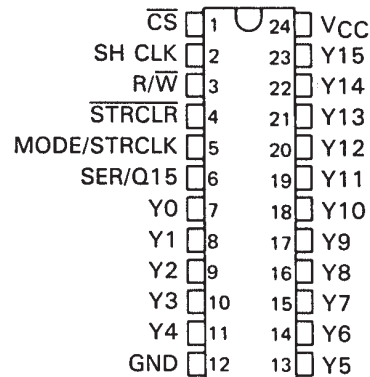
The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering a serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

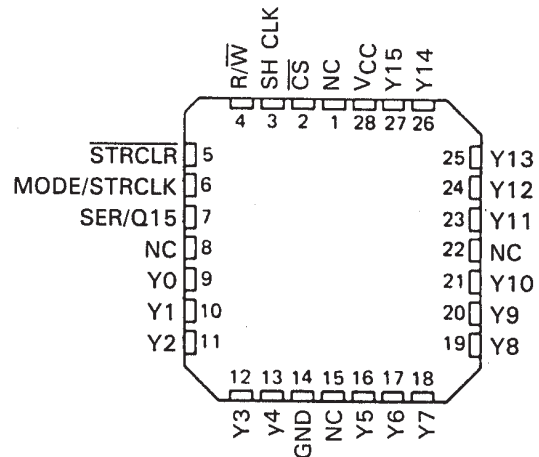
- 1) Hold (do nothing)
- 2) Write (serially via input/output)
- 3) Read (serially)
- 4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

SN54LS673 . . . J OR W PACKAGE SN74LS673 . . . DW OR N PACKAGE (TOP VIEW)



SN54LS673 . . . FK PACKAGE (TOP VIEW)

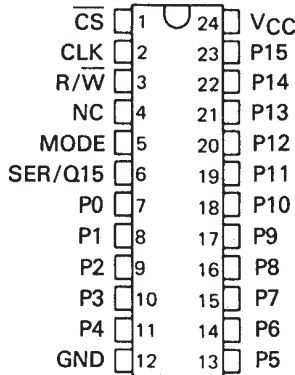


NC—No internal connection

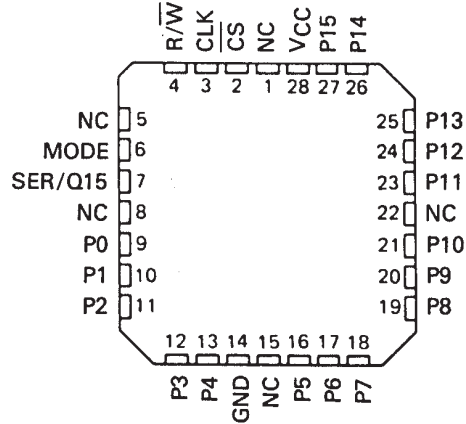
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SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS674 . . . FK PACKAGE
(TOP VIEW)



'LS673
FUNCTION TABLE

| INPUTS | | | | | SER/ Q15 | SHIFT REGISTER FUNCTIONS | | | | STORAGE REGISTER FUNCTIONS | |
|-----------------|-----|--------|---------------------|-----------------|-------------|--------------------------|----------------------------|----------------------------|------------------|----------------------------|------|
| \overline{CS} | R/W | SH CLK | \overline{STRCLR} | MODE/ STRCLK | | SHIFT | READ FROM SERIAL OUTPUT | WRITE INTO SERIAL INPUT | PARALLEL LOAD | CLEAR | LOAD |
| H | X | X | X | X | Z | NO | NO | NO | NO | | NO |
| X | X | X | L | X | | | | | | YES | |
| L | L | ↓ | X | X | Z | YES | NO | YES | NO | | |
| L | H | X | X | X | Q15 | | YES | NO | | | NO |
| L | H | ↓ | X | L | Q14n | YES | YES | NO | NO | | NO |
| L | H | ↓ | L | H | L | NO | YES | | YES | YES | NO |
| L | H | ↓ | H | H | Y15n | NO | YES | | YES | NO | NO |
| L | L | X | H | ↑ | Z | | NO | | NO | NO | YES |

'LS674 FUNCTION TABLE

| INPUTS | | | | SER/ Q15 | OPERATION |
|-----------------|-----|------|-----|-------------|-------------------------------|
| \overline{CS} | R/W | MODE | CLK | | |
| H | X | X | X | Z | Do nothing |
| L | L | X | ↓ | Z | Shift and write (serial load) |
| L | H | L | ↓ | Q14n | Shift and read |
| L | H | H | ↓ | P15 | Parallel load |

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

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logic symbols†

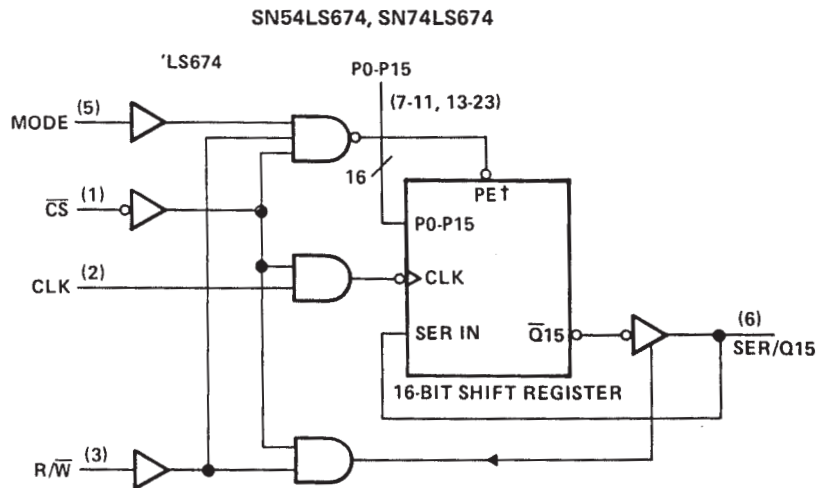
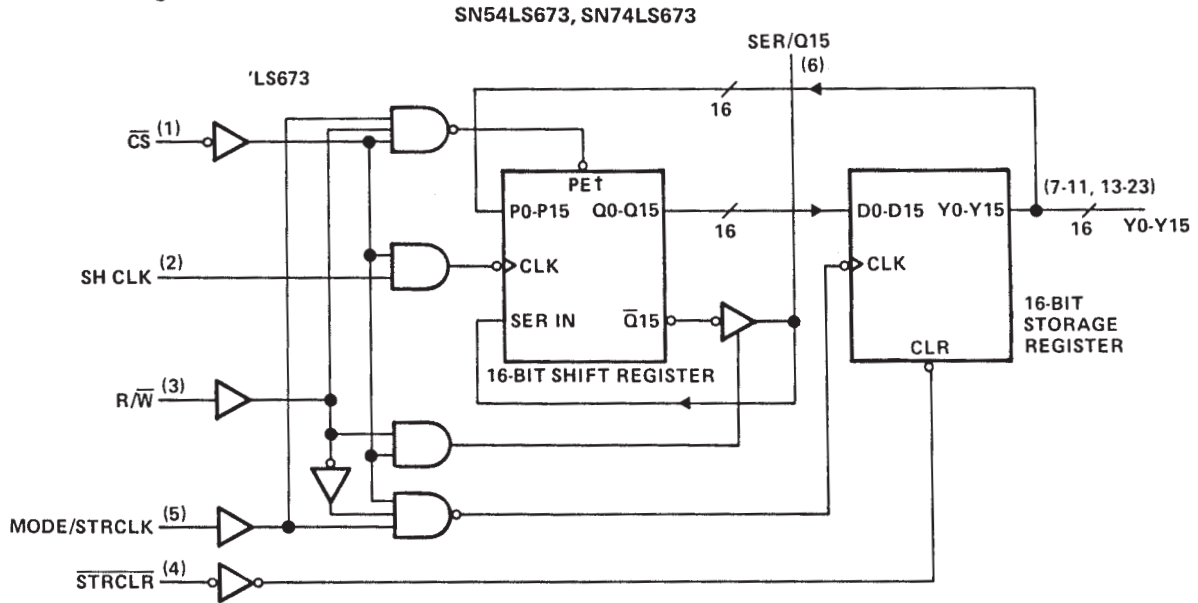


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

SN54LS673, SN54LS674, SN74LS673, SN74LS674 16-BIT SHIFT REGISTERS

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functional block diagrams

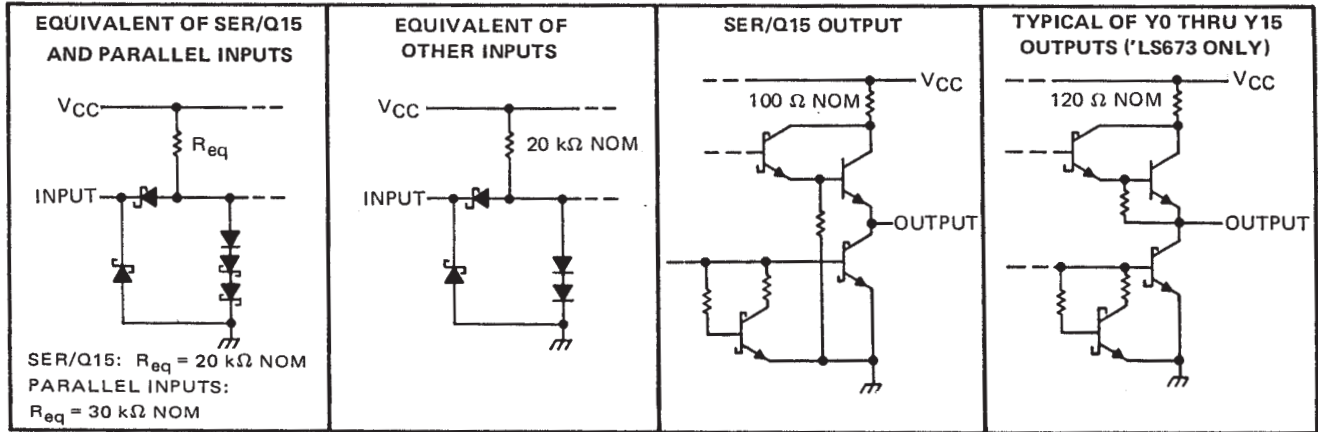


†When PE is active, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place. Pin numbers shown are for DW, J, N, and W packages.

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: SER/Q15 | 5.5 V |
| All others | 7 V |
| Off-state output voltage | 5.5 V |
| Operating free-air temperature range: SN54LS673, SN54LS674 | -55°C to 125°C |
| SN74LS673, SN74LS674 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

| | | SN54LS' | | | SN74LS' | | | UNIT |
|----------------|--------------------------------|--|--------|------|-------------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| I_{OH} | High-level output current | SER/Q15 | | -1 | Y0 thru Y15 | | -2.6 | mA |
| | | Y0 thru Y15 | | -0.4 | SER/Q15 | | -0.4 | |
| I_{OL} | Low-level output current | SER/Q15 | | 12 | Y0 thru Y15 | | 24 | mA |
| | | Y0 thru Y15 | | 4 | SER/Q15 | | 8 | |
| f_{clock} | Clock frequency | 0 | | 20 | 0 | | 20 | MHz |
| $t_{w(clock)}$ | Width of clock input pulse | 20 | | | 20 | | | ns |
| $t_{w(clear)}$ | Width of clear input pulse | 20 | | | 20 | | | ns |
| t_{su} | Setup time | SER/Q15 | | 20 | | | 20 | ns |
| | | P0 thru P15 | | 20 | | | 20 | |
| | | Mode | | 35 | | | 35 | |
| | | $R/\bar{W}, \bar{CS}$ | | 35 | | | 35 | |
| | | SH CLK ↓ to Mode/STR CLK ↑ See Note 2 | | 25 | | | 25 | |
| t_h | Hold time | SER/Q15 | | 0 | | | 0 | ns |
| | | P0 thru P15 | 'LS673 | 0 | | | 0 | |
| | | | 'LS674 | 5.0 | | | 5.0 | |
| Mode | | | | 0 | | | 0 | |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

NOTE 2: This setup time ensures the storage register will see stable data from the shift register.



SN54LS673, SN54LS674, SN74LS673, SN74LS674

16-BIT SHIFT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54LS' | | SN74LS' | | UNIT |
|------------------|--|--|---|-------------------------|---------|------|------|
| | | | MIN | TYP‡ | MAX | MIN | |
| V _{IH} | High-level input voltage | | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | | 0.7 | | 0.8 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = -18 mA | | -1.5 | | -1.5 | V |
| V _{OH} | High-level output voltage | SER/Q15 | V _{CC} = MIN, V _{IH} = 2 V, | | 2.4 | 3.1 | V |
| | | Y0 thru Y15¶ | V _{IL} = V _{ILmax} , I _{OH} = MAX | | 2.5 | 3.4 | |
| V _{OL} | Low-level output voltage | SER/Q15 | V _{CC} = MIN, V _{IH} = 2 V, | I _{OL} = 12 mA | 0.25 | 0.4 | V |
| | | | | I _{OL} = 24 mA | | 0.35 | |
| | | Y0 thru Y15¶ | V _{IL} = V _{ILmax} | I _{OL} = 4 mA | 0.25 | 0.4 | |
| | | | | I _{OL} = 8 mA | | 0.35 | |
| I _{OZH} | Off-state output current, high-level voltage applied | SER/Q15 | V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 2.7 V | 40 | | 40 | μA |
| I _{OZL} | Off-state output current, low-level voltage applied | SER/Q15 | V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = V _{ILmax} , V _O = 0.4 V | -0.4 | | -0.4 | mA |
| I _I | Input current at maximum input voltage | SER/Q15 | V _{CC} = MAX | V _I = 5.5 V | | 0.1 | mA |
| | | Others | | V _I = 7 V | | 0.1 | |
| I _{IH} | High-level input current | SER/Q15 | V _{CC} = MAX, V _I = 2.7 V | | | 40 | μA |
| | | Others | | | | 20 | |
| I _{IL} | Low-level input current | | V _{CC} = MAX, V _I = 0.4 V | | | -0.4 | mA |
| I _{OS} | Short-circuit output current§ | SER/Q15 | V _{CC} = MAX | | -30 | -130 | mA |
| | | Y0 thru Y15¶ | | | -20 | -100 | |
| I _{CC} | Supply current | 'LS673 | V _{CC} = MAX | | 50 | 80 | mA |
| | | 'LS674 | | | 25 | 40 | |

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

¶ 'LS673 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

| PARAMETER | 'LS673 | | 'LS674 | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------|-------------|---------|---------|--|-----|-----|-----|------|
| | FROM | TO | FROM | TO | | | | | |
| f _{max} | SH CLK | SER/Q15 | CLK | SER/Q15 | R _L = 667 Ω, C _L = 45 pF | 20 | 28 | | MHz |
| t _{PHL} | STRCLR | Y0 thru Y15 | | | R _L = 2 kΩ, C _L = 15 pF | | 25 | 40 | ns |
| t _{PLH} | MODE/ STRCLK | Y0 thru Y15 | | | | | 28 | 45 | |
| t _{PHL} | | | | | R _L = 667 Ω, C _L = 45 pF | | 30 | 45 | ns |
| t _{PLH} | SH CLK | SER/Q15 | CLK | SER/Q15 | | | 21 | 33 | |
| t _{PZH} | CS, R/W | SER/Q15 | CS, R/W | SER/Q15 | R _L = 667 Ω, C _L = 45 pF | | 30 | 45 | ns |
| t _{PZL} | | | | | | | 30 | 45 | |
| t _{PHZ} | CS, R/W | SER/Q15 | CS, R/W | SER/Q15 | R _L = 667 Ω, C _L = 5 pF | | 25 | 40 | ns |
| t _{PLZ} | | | | | | | 25 | 40 | |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|--------------------------------------|----------------------|--------------|--|-------------------------|
| 5962-88602013A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 88602013A SNJ54LS 673FK | Samples |
| 5962-8860201JA | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8860201JA SNJ54LS673J | Samples |
| 5962-8860201JA | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8860201JA SNJ54LS673J | Samples |
| 5962-8860201LA | ACTIVE | CDIP | JT | 24 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8860201LA SNJ54LS673JT | Samples |
| 5962-8860201LA | ACTIVE | CDIP | JT | 24 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8860201LA SNJ54LS673JT | Samples |
| 5962-88607013A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 88607013A SNJ54LS 674FK | Samples |
| 5962-88607013A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 88607013A SNJ54LS 674FK | Samples |
| 5962-8860701JA | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8860701JA SNJ54LS674J | Samples |
| 5962-8860701JA | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8860701JA SNJ54LS674J | Samples |
| SN54LS673J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS673J | Samples |
| SN54LS673J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS673J | Samples |
| SN54LS674J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS674J | Samples |
| SN54LS674J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS674J | Samples |
| SN74LS673DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS673 | Samples |
| SN74LS673DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS673 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| SN74LS674DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS674 | Samples |
| SN74LS674DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS674 | Samples |
| SN74LS674DWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS674 | Samples |
| SN74LS674DWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS674 | Samples |
| SNJ54LS673FK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-88602013A SNJ54LS 673FK | Samples |
| SNJ54LS673FK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-88602013A SNJ54LS 673FK | Samples |
| SNJ54LS673J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8860201JA SNJ54LS673J | Samples |
| SNJ54LS673J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8860201JA SNJ54LS673J | Samples |
| SNJ54LS673JT | ACTIVE | CDIP | JT | 24 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8860201LA SNJ54LS673JT | Samples |
| SNJ54LS673JT | ACTIVE | CDIP | JT | 24 | 1 | TBD | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8860201LA SNJ54LS673JT | Samples |
| SNJ54LS674FK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-88607013A SNJ54LS 674FK | Samples |
| SNJ54LS674FK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-88607013A SNJ54LS 674FK | Samples |
| SNJ54LS674J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8860701JA SNJ54LS674J | Samples |
| SNJ54LS674J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8860701JA SNJ54LS674J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS673, SN54LS674, SN74LS673, SN74LS674 :

● Catalog: [SN74LS673](#), [SN74LS674](#)

● Military: [SN54LS673](#), [SN54LS674](#)

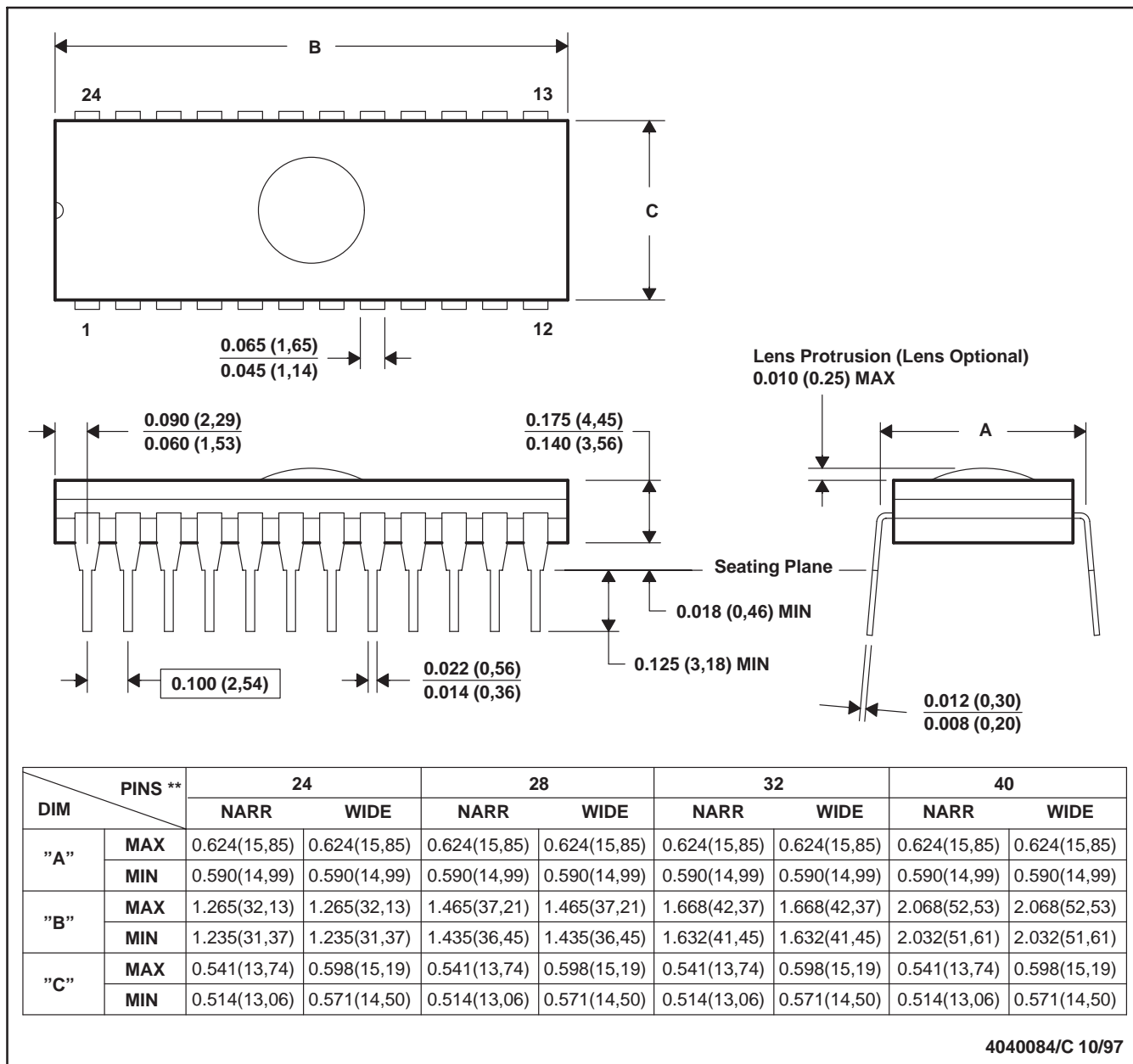
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

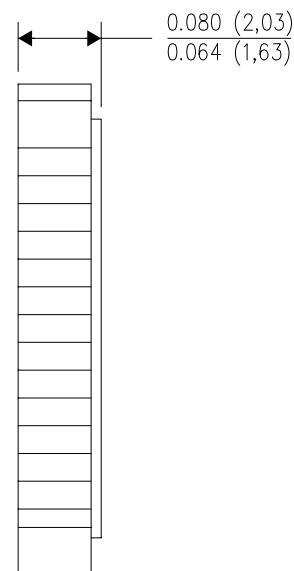
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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