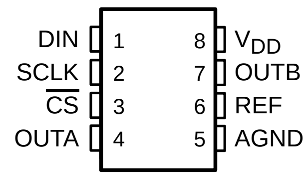
features

- Dual 10-Bit Voltage Output DAC
- Programmable Settling Time
  - 3 µs in Fast Mode
  - 10 µs in Slow Mode
- Compatible With TMS320 and SPI™ Serial Ports
- Differential Nonlinearity <0.1 LSB Typ
- Monotonic Over Temperature
- Direct Replacement for TLC5617A

applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

D PACKAGE
(TOP VIEW)



description

The TLV5617A is a dual 10-bit voltage output DAC with a flexible 3-wire serial interface. The serial interface is compatible with TMS320, SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control bits and 10 data bits.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class-AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation.

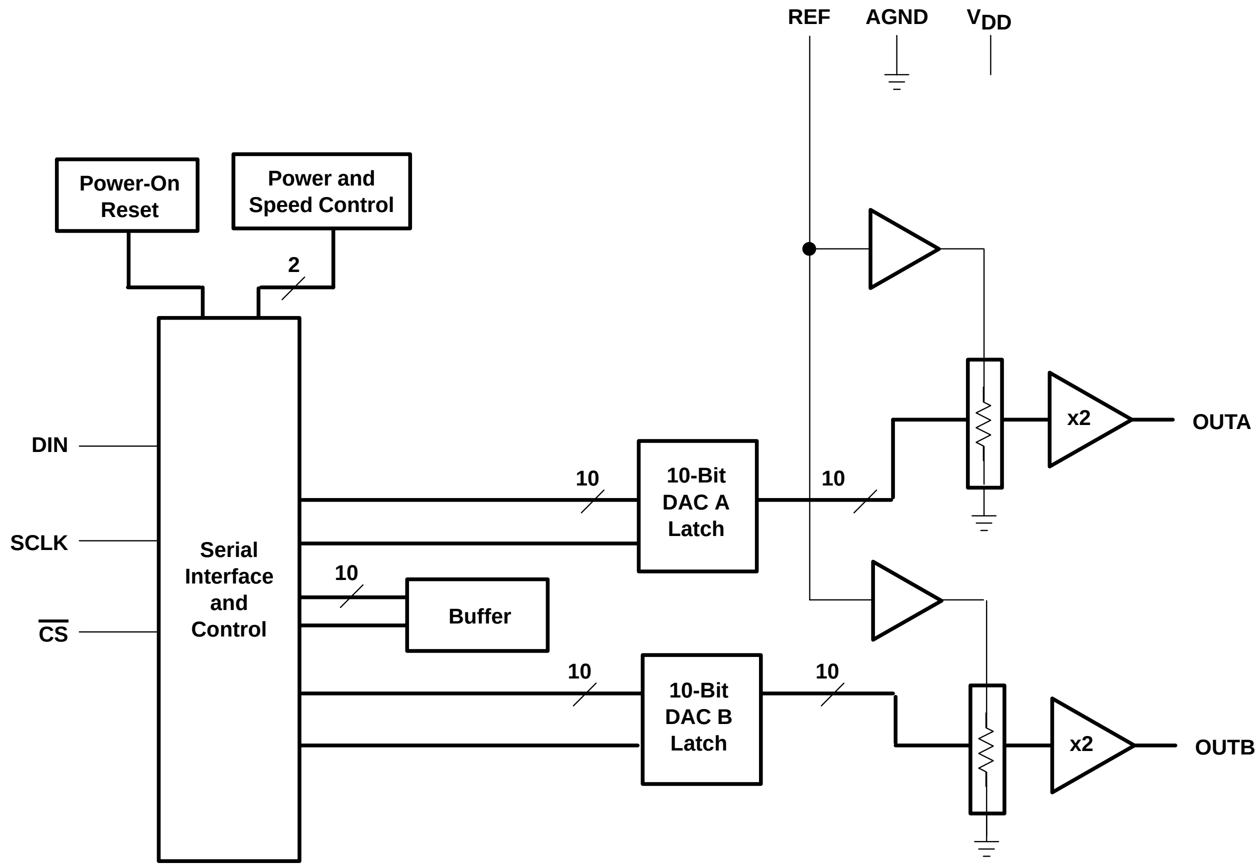
Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC package in standard commercial and industrial temperature ranges.

AVAILABLE OPTIONS

T_A	PACKAGE SOIC (D)
0°C to 70°C	TLV5617ACD
–40°C to 85°C	TLV5617AID

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O/P	DESCRIPTION
AGND	5	P	Ground
$\overline{\text{CS}}$	3	I	Chip select. Digital input active low, used to enable/disable inputs.
DIN	1	I	Digital serial data input
OUTA	4	O	DAC A analog voltage output
OUTB	7	O	DAC B analog voltage output
REF	6	I	Analog reference voltage input
SCLK	2	I	Digital serial clock input
V_{DD}	8	P	Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND) . . . . 7 V
Reference input voltage range . . . . – 0.3 V to V_{DD} + 0.3 V
Digital input voltage range . . . . – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5617AC . . . . 0°C to 70°C
TLV5617AI . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 5 V	4.5	5	5.5	V
	V_{DD} = 3 V	2.7	3	3.3	
Power on reset, POR		0.55		2	V
High-level digital input voltage, V_{IH}	V_{DD} = 2.7 V	2			V
	V_{DD} = 5.5 V	2.4			
Low-level digital input voltage, V_{IL}	V_{DD} = 2.7 V			0.6	V
	V_{DD} = 5.5 V			1	
Reference voltage, V_{ref} to REF terminal	V_{DD} = 5 V (see Note 1)	AGND	2.048	V_{DD}–1.5	V
	V_{DD} = 3 V (see Note 1)	AGND	1.024	V_{DD}–1.5	
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Clock frequency, f_{CLK}				20	MHz
Operating free-air temperature, T_A	TLV5617AC	0		70	°C
	TLV5617AI	–40		85	

NOTE 1: Due to the x2 output buffer, a reference input voltage ≥ (V_{DD}–0.4 V)/2 causes clipping of the transfer function.

electrical characteristics over recommended operating conditions (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	Fast		1.6	2.5	mA
			Slow		0.6	1	mA
	Power down supply current				1		μA
PSRR	Power supply rejection ratio	Zero scale, See Note 2			–65		dB
		Full scale, See Note 3			–65		dB

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:
$PSRR = 20 \log [(E_{ZS}(V_{DD}max) – E_{ZS}(V_{DD}min)/V_{DD}max]$
3. Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:
$PSRR = 20 \log [(E_G(V_{DD}max) – E_G(V_{DD}min)/V_{DD}max]$

static DAC specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution			10			bits
INL	Integral nonlinearity	See Note 4			±0.7	±1	LSB
DNL	Differential nonlinearity	See Note 5			±0.1	±0.5	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	See Note 6				±12	mV
E_{ZS} TC	Zero-scale-error temperature coefficient	See Note 7			3		ppm/°C
E_G	Gain error	See Note 8	V_{DD} = 2.7 V to 3.3 V			±0.6	% full scale V
			V_{DD} = 4.5 V to 5.5 V			±0.29	% full scale V
E_G T_C	Gain-error temperature coefficient	See Note 9			1		ppm/°C

NOTES: 4. The relative accuracy of integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale, excluding the effects of zero-code and full-scale errors.
5. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1-LSB amplitude change of any two adjacent codes.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: $E_{ZS}\ TC = [E_{ZS}(T_{max}) – E_{ZS}(T_{min})]/2V_{ref} \times 10^6/(T_{max} – T_{min})$.
8. Gain error is the deviation from the ideal output ($2V_{ref}$ – 1 LSB) with an output load of 10 kΩ.
9. Gain temperature coefficient is given by: $E_G\ T_C = [E_G(T_{max}) – E_g(T_{min})]/2V_{ref} \times 10^6/(T_{max} – T_{min})$.

output specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage range	R_L = 10 kΩ			V_{DD}–0.4	V
	Output load regulation accuracy	V_O = 4.096 V, 2.048 V, R_L = 2 kΩ to 10 kΩ		±0.1		% FS

reference input

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			0		V_{DD}–1.5	V
R_I	Input resistance				10		MΩ
C_I	Input capacitance				5		pF
	Reference input bandwidth	REF = 0.2 V_{pp} + 1.024 V dc	Fast		1.3		MHz
			Slow		525		kHz
	Reference feedthrough	REF = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 10)			–80		dB

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

electrical characteristics over recommended operating conditions (unless otherwise noted) (Continued)

digital inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			1	µA
I_{IL}	Low-level digital input current	$V_I = 0$ V	–1			µA
C_i	Input capacitance			8		pF

analog output dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	$R_L = 10$ kΩ,	$C_L = 100$ pF, See Note 11	Fast		1	3	µs
				Slow		3	10	
$t_{s(CC)}$	Output settling time, code to code	$R_L = 10$ kΩ,	$C_L = 100$ pF, See Note 12	Fast		1		µs
				Slow		2		
SR	Slew rate	$R_L = 10$ kΩ,	$C_L = 100$ pF, See Note 13	Fast		3		V/µs
				Slow		0.5		
	Glitch energy	DIN = 0 to 1,	FCLK = 100 kHz, $\overline{CS} = V_{DD}$			5		nV–s
SNR	Signal-to-noise ratio	$f_s = 102$ kSPS, $C_L = 100$ pF	$f_{out} = 1$ kHz, $R_L = 10$ kΩ,			68		dB
SINAD	Signal-to-noise + distortion					65		dB
THD	Total harmonic distortion					–62		dB
SFDR	Spurious free dynamic range					64		dB

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDC and 0xFDC to 0x020 respectively. Not tested, assured by design.

12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.

13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% of full-scale voltage.

digital input timing requirements

			MIN	NOM	MAX	UNIT
$t_{su(CS–CK)}$	Setup time, $\overline{CS}$ low before first negative SCLK edge	V_{DD} = 2.7 V to 3.3 V	10			ns
		V_{DD} = 4.5 V to 5.5 V	5			
$t_{su(C16-CS)}$	Setup time, 16th negative SCLK edge before $\overline{CS}$ rising edge		10			ns
t_{wH}	SCLK pulse width high		25			ns
t_{wL}	SCLK pulse width low		25			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	V_{DD} = 2.7 V to 3.3 V	10			ns
		V_{DD} = 4.5 V to 5.5 V	5			
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	V_{DD} = 2.7 V to 3.3 V	10			ns
		V_{DD} = 4.5 V to 5.5 V	5			

timing requirements

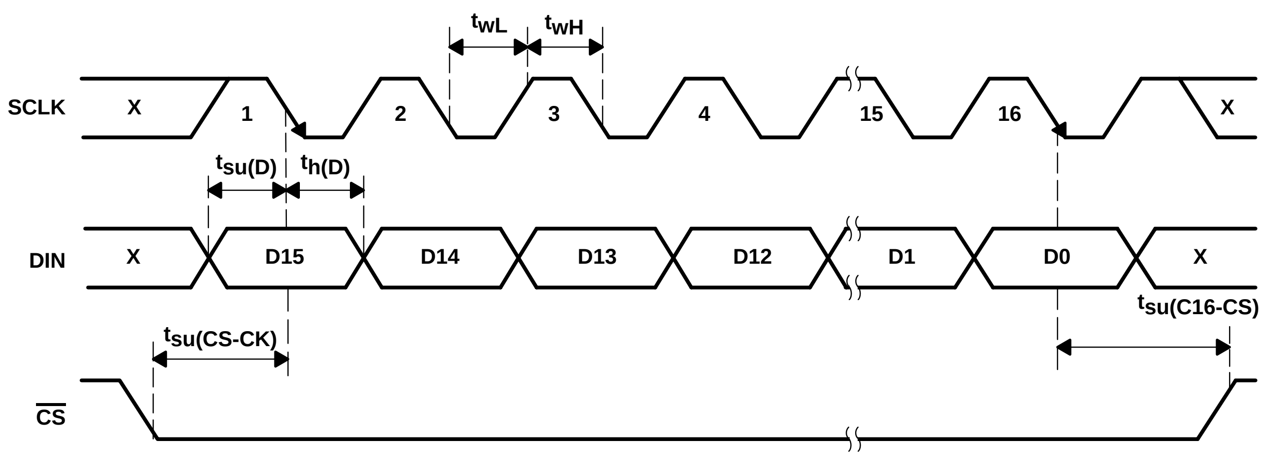


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

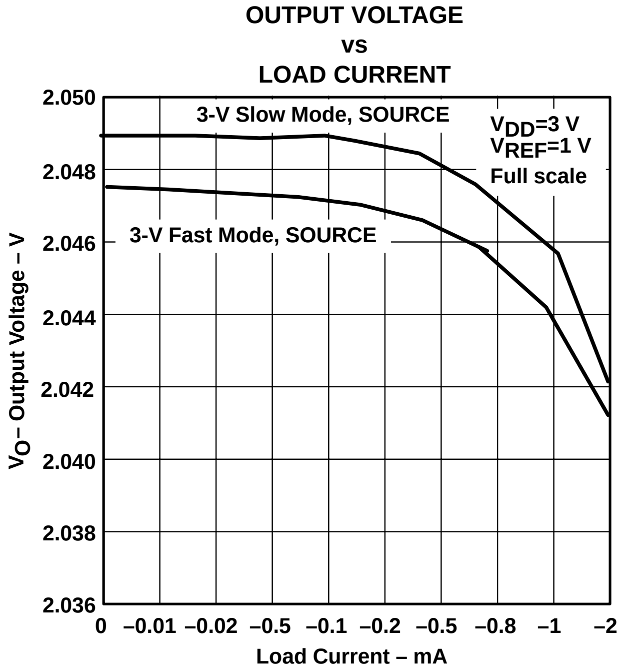


Figure 2

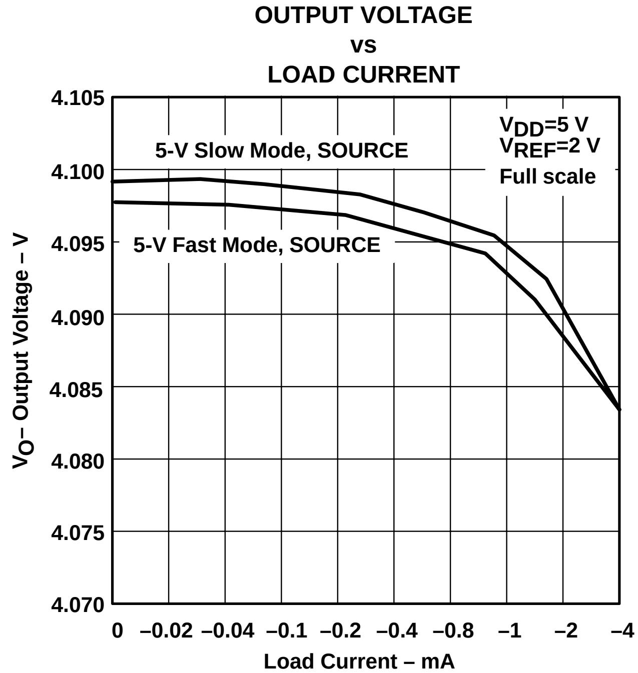


Figure 3

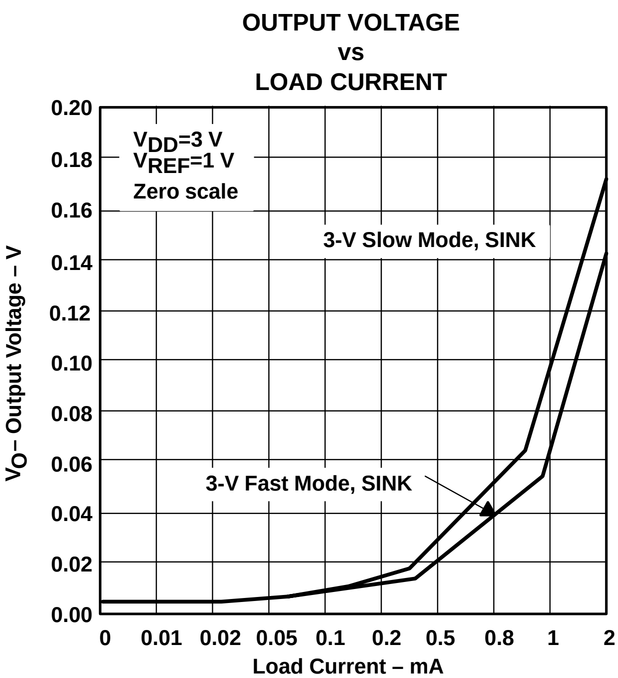


Figure 4

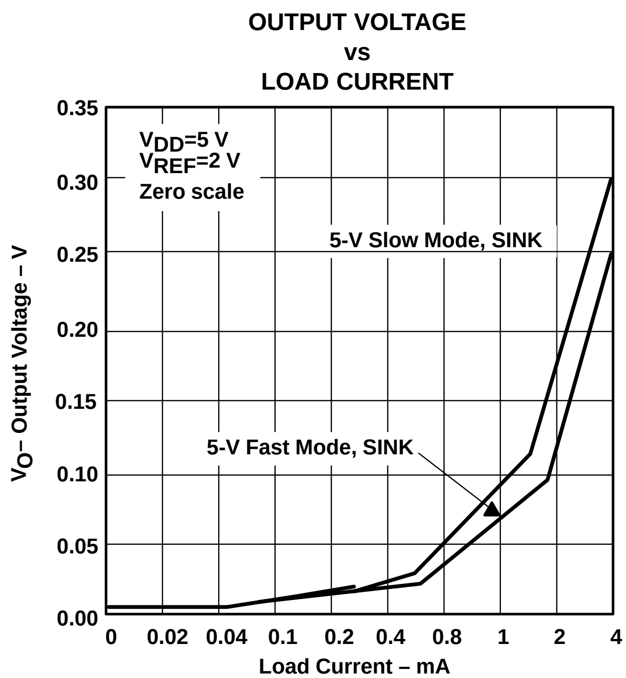


Figure 5

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

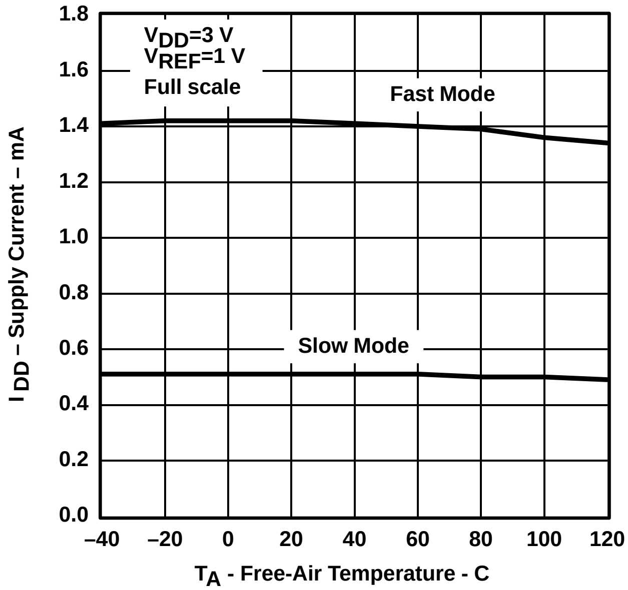


Figure 6

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

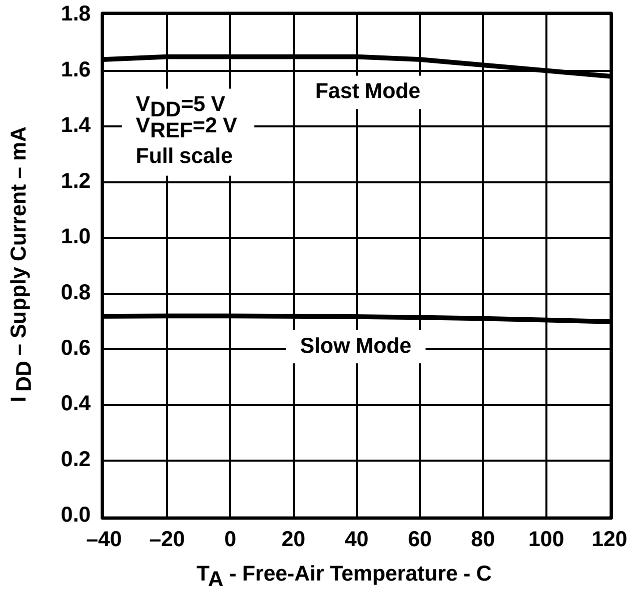


Figure 7

TOTAL HARMONIC DISTORTION vs FREQUENCY

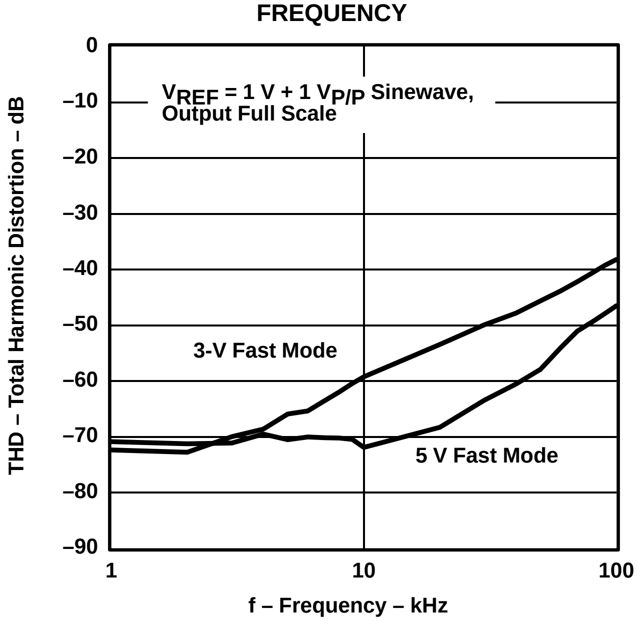


Figure 8

TOTAL HARMONIC DISTORTION vs FREQUENCY

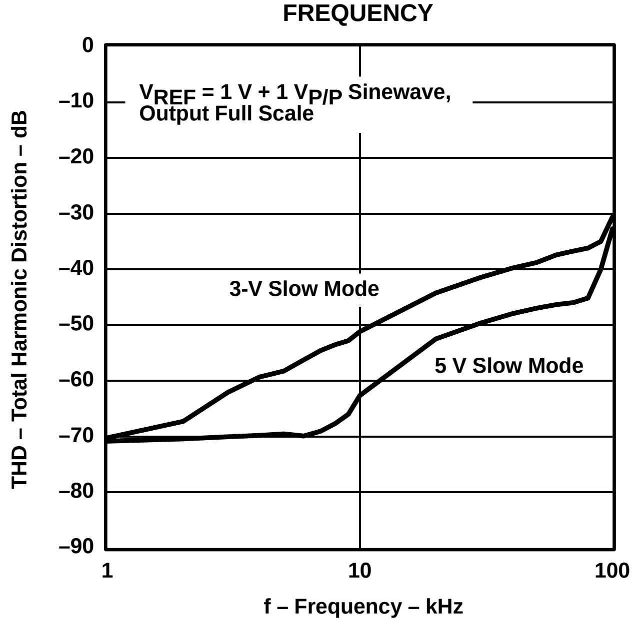


Figure 9

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY ERROR
vs
DIGITAL CODE

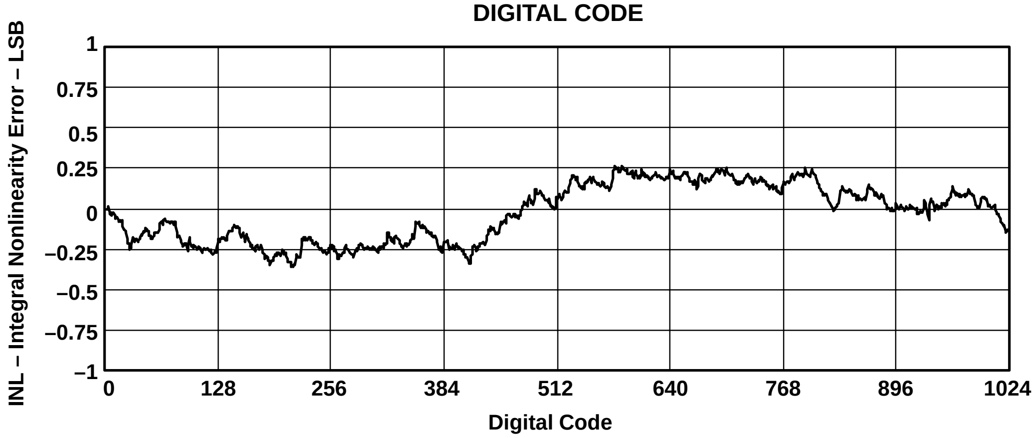


Figure 10

DIFFERENTIAL NONLINEARITY ERROR
vs
DIGITAL CODE

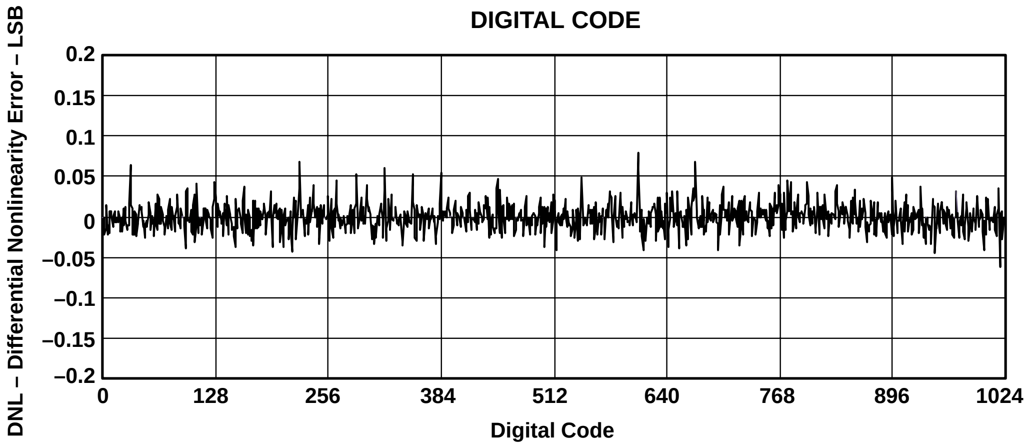


Figure 11

APPLICATION INFORMATION

general function

The TLV5617A is a dual 10-bit, single-supply DAC, based on a resistor-string architecture. It consists of a serial interface, speed and power-down control logic, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by the reference) is given by:

$$2\ \text{REF}\ \frac{\text{CODE}}{2^n}\ [\text{V}]$$

Where REF is the reference voltage and CODE is the digital input value within the range of 0_{10} to $2^n–1$, where n=10 (bits). The 16-bit data word, consisting of control bits and the new DAC value, is illustrated in the *data format* section. A power-on reset initially resets the internal latches to a defined state (all bits zero).

serial interface

A falling edge of $\overline{\text{CS}}$ starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or $\overline{\text{CS}}$ rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 12 shows examples of how to connect the TLV5617A to TMS320, SPI, and Microwire.

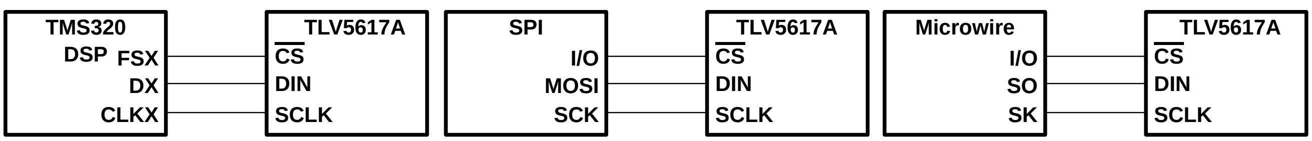


Figure 12. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the pin connected to $\overline{\text{CS}}$. If the word width is 8 bits (SPI and Microwire) two write operations must be performed to program the TLV5617A. After the write operation(s), the holding registers or the control register of the DAC update automatically on the rising $\overline{\text{CS}}$ edge, ending the write cycle to the DAC. Note: After transfer of the LSB during a data or control write cycle, one additional rising edge on SCLK is required to reset the internal state machine. This edge can occur when $\overline{\text{CS}}$ is high or low, but must occur before the next falling $\overline{\text{CS}}$ edge that begins the following write cycle. Refer to the timing diagram for more information.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 20\ \text{MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16\left(t_{whmin} + t_{wlmin}\right)} = 1.25\ \text{MHz}$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5617A should also be considered.

APPLICATION INFORMATION

data format

The 16-bit data word for the TLV5617A consists of two parts:

- Program bits (D15..D12)
- New data (D11..D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	SPD	PWR	R0	MSB				10 Data bits					LSB	0	0

SPD: Speed control bit 1 → fast mode 0 → slow mode
PWR: Power control bit 1 → power down 0 → normal operation
On power up, SPD and PWD are reset to 0 (slow mode and normal operation)

The following table lists all possible combinations of register-select bits:

register-select bits

R1	R0	REGISTER
0	0	Write data to DAC B and BUFFER
0	1	Write data to BUFFER
1	0	Write data to DAC A and update DAC B with BUFFER content
1	1	Reserved

The meaning of the 12 data bits depends on the register. If one of the DAC registers or the BUFFER is selected, then the 12 data bits determine the new DAC value:

examples of operation

- Set DAC A output, select fast mode:

  Write new DAC A value and update DAC A output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	New DAC A output value										0	0

The DAC A output is updated on the rising clock edge after D0 is sampled.

- Set DAC B output, select fast mode:

  Write new DAC B value to BUFFER and update DAC B output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	New BUFFER content and DAC B output value										0	0

The DAC A output is updated on the rising clock edge after D0 is sampled.

- Set DAC A value, set DAC B value, update both simultaneously, select slow mode:

  1. Write data for DAC B to BUFFER:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	New DAC B value										0	0

  2. Write new DAC A value and update DAC A and B simultaneously:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	New DAC A value										0	0

APPLICATION INFORMATION

examples of operation (continued)

Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

- Set powerdown mode:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Don't care

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 13.

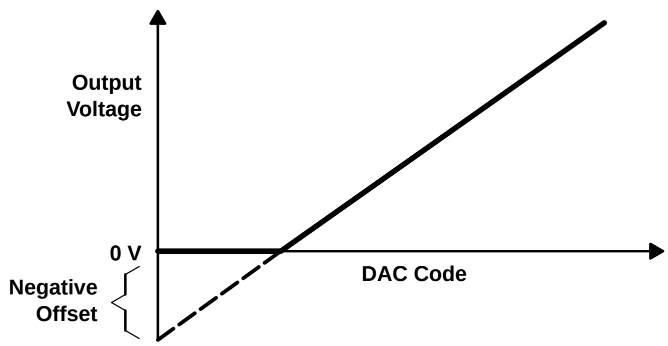


Figure 13. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

definitions of specifications and terminology (continued)

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

total harmonic distortion (THD)

THD is the ratio of the rms value of the first six harmonic components to the value of the fundamental signal. The value for THD is expressed in decibels.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5617ACD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5617	Samples
TLV5617ACDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5617	Samples
TLV5617ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5617	Samples
TLV5617AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5617	Samples
TLV5617AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5617	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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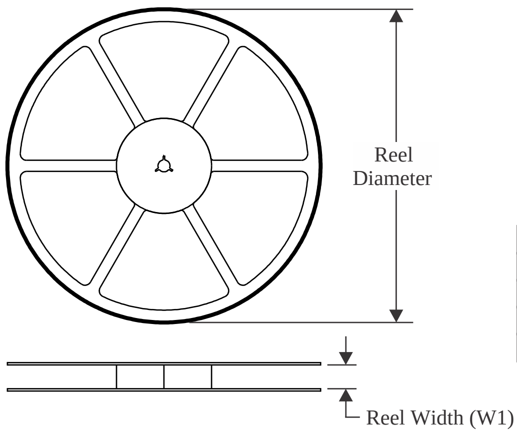
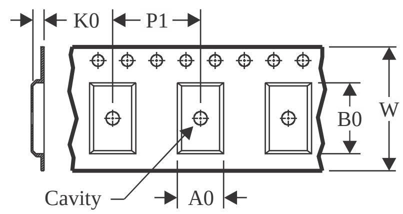
TAPE AND REEL INFORMATION

REEL DIMENSIONS

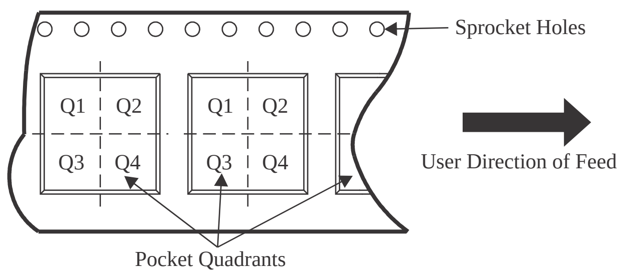


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

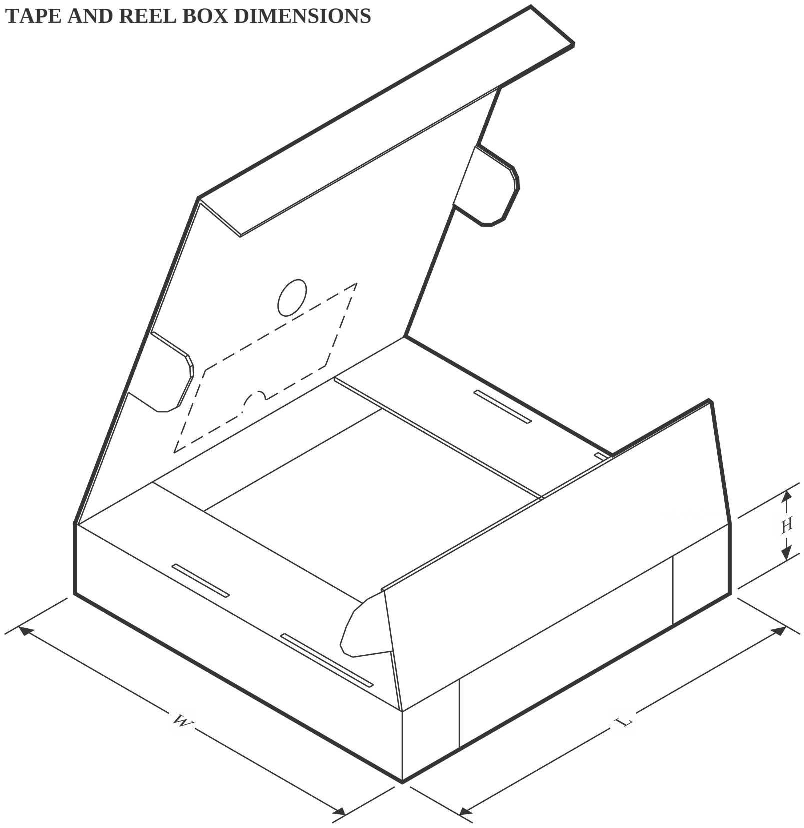
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5617AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

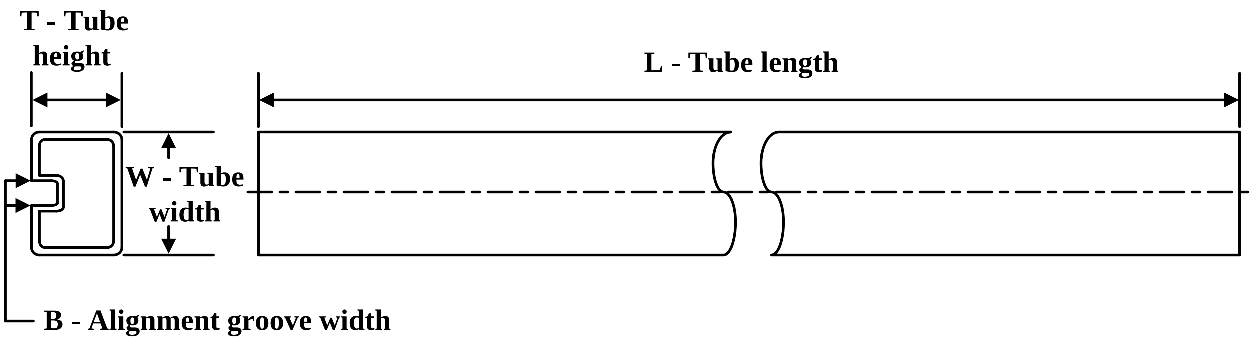
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

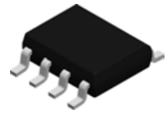
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5617AIDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

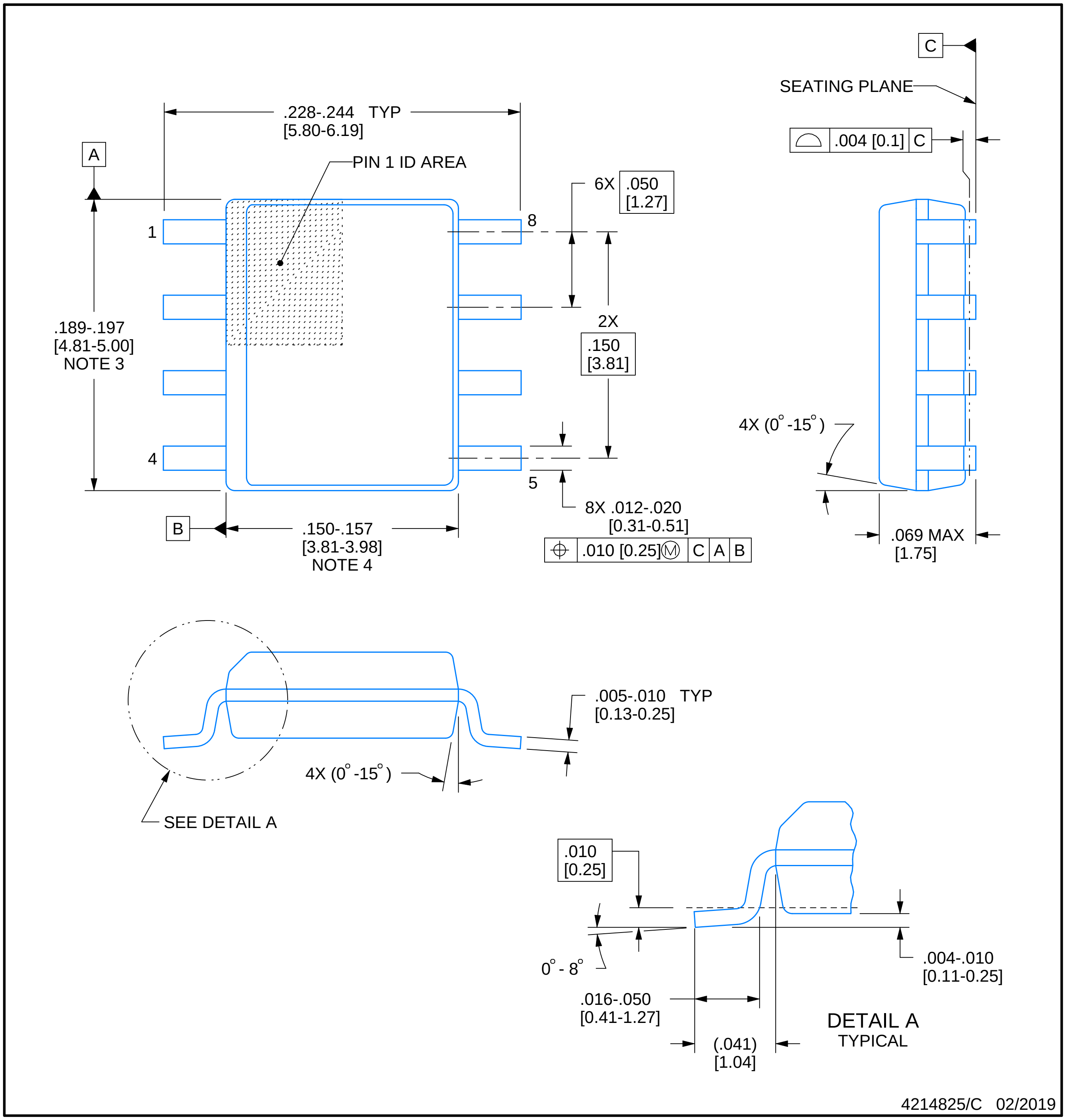
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5617ACD	D	SOIC	8	75	505.46	6.76	3810	4
TLV5617ACDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLV5617AID	D	SOIC	8	75	505.46	6.76	3810	4



D0008A

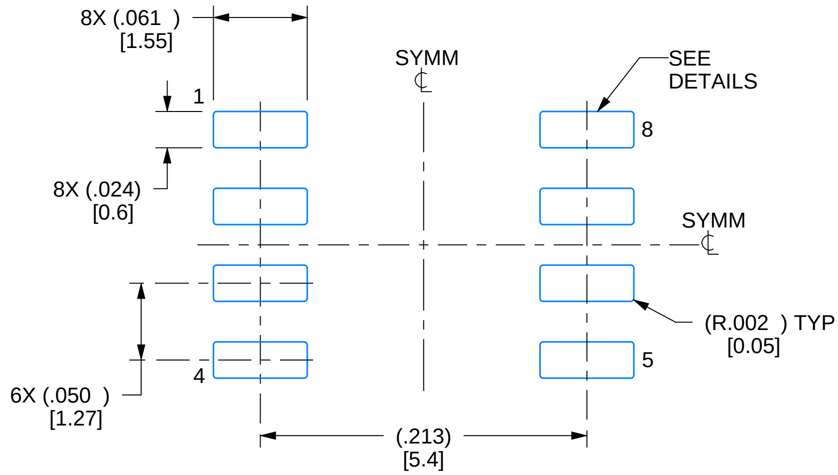
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

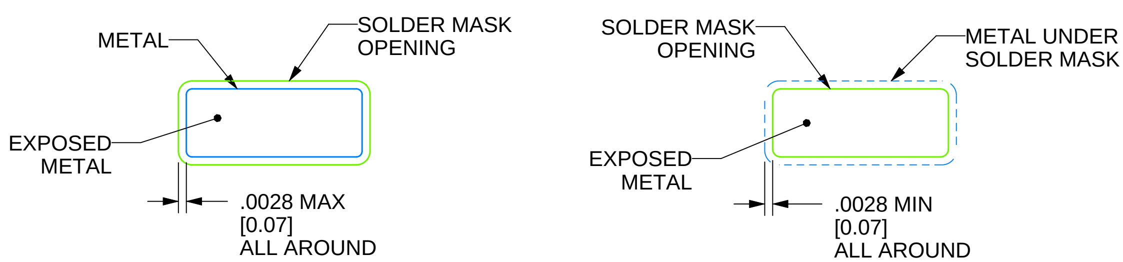


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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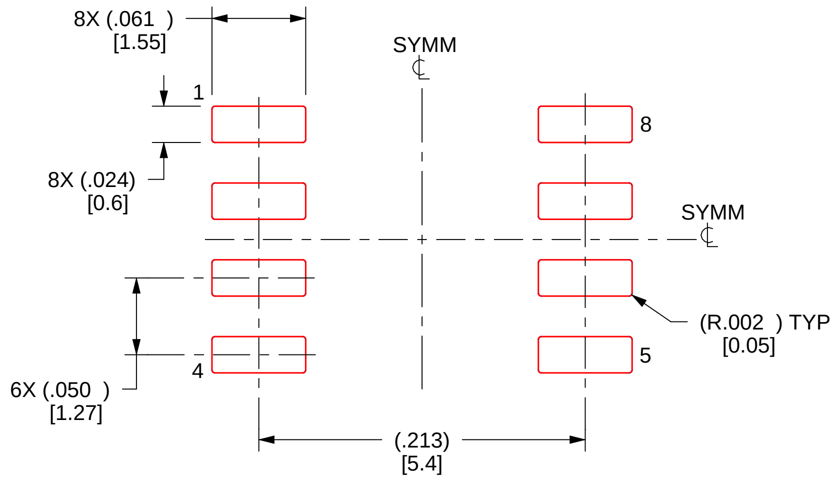
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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