DisplayPort to TMDS Translator

FEATURES

- **DisplayPort Physical Layer Input Port to TMDS Physical Layer Output Port**
- **Integrated TMDS Level Translator With Receiver Equalization**
- **Supports Data Rates up to 2.5 Gbps**
- **Integrated I^2C Logic Block for DVI / HDMI Connector Recognition**
- **Integrated Active I^2C Buffer**
- **Enhanced ESD: 12 kV on all Pins**
- **Enhanced Commercial Temperature Range: 0°C to 85°C**
- **36 Pin 6 × 6 QFN Package**

APPLICATIONS

- **Personal Computer Market**
  - **DP/TMDS Hardware Key (Dongle)**
  - **Desktop PC**
  - **Notebook PC**
  - **Docking Station**
  - **Standalone Video Card**

DESCRIPTION

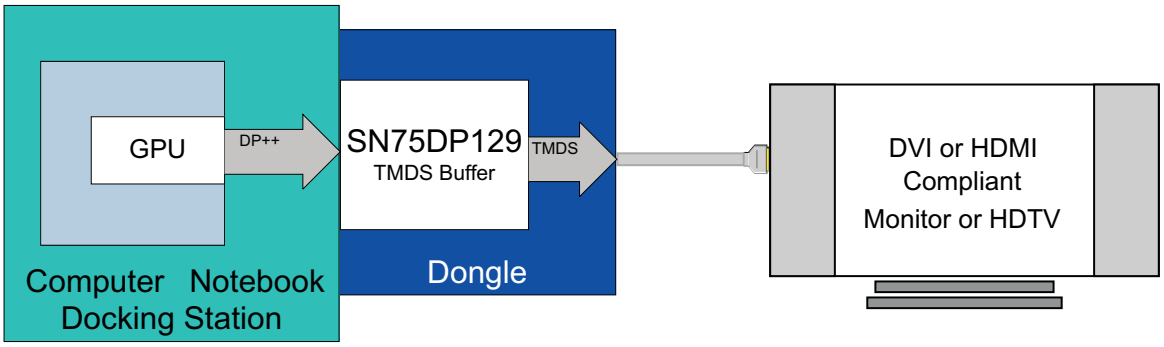
The SN75DP129 is a Dual-Mode DisplayPort input to Transition-Minimized Differential Signaling (TMDS) output. The TMDS output has a built-in level translator, compliant with Digital Visual Interface 1.0 (DVI) and High Definition Multimedia Interface 1.3 (HDMI) standards. The SN75DP129 is specified up to a maximum data rate of 2.5 Gbps, supporting resolutions greater then 1920 x 1200 or HDTV 12-bit color depth at 1080p (progressive scan).

An integrated Active I^2C buffer isolates the capacitive loading of the source system from that of the sink and interconnecting cable. This isolation improves overall signal integrity of the system and provides greater design margin within the source system for DVI / HDMI compliance testing.

A logic block was designed into the SN75DP129 to assist with TMDS connector identification. Through the use of the I^2C_EN pin, this logic block can be enabled to indicate the translated port is an HDMI port; therefore legally supporting HDMI content.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION



GPU—Graphics Processing Unit

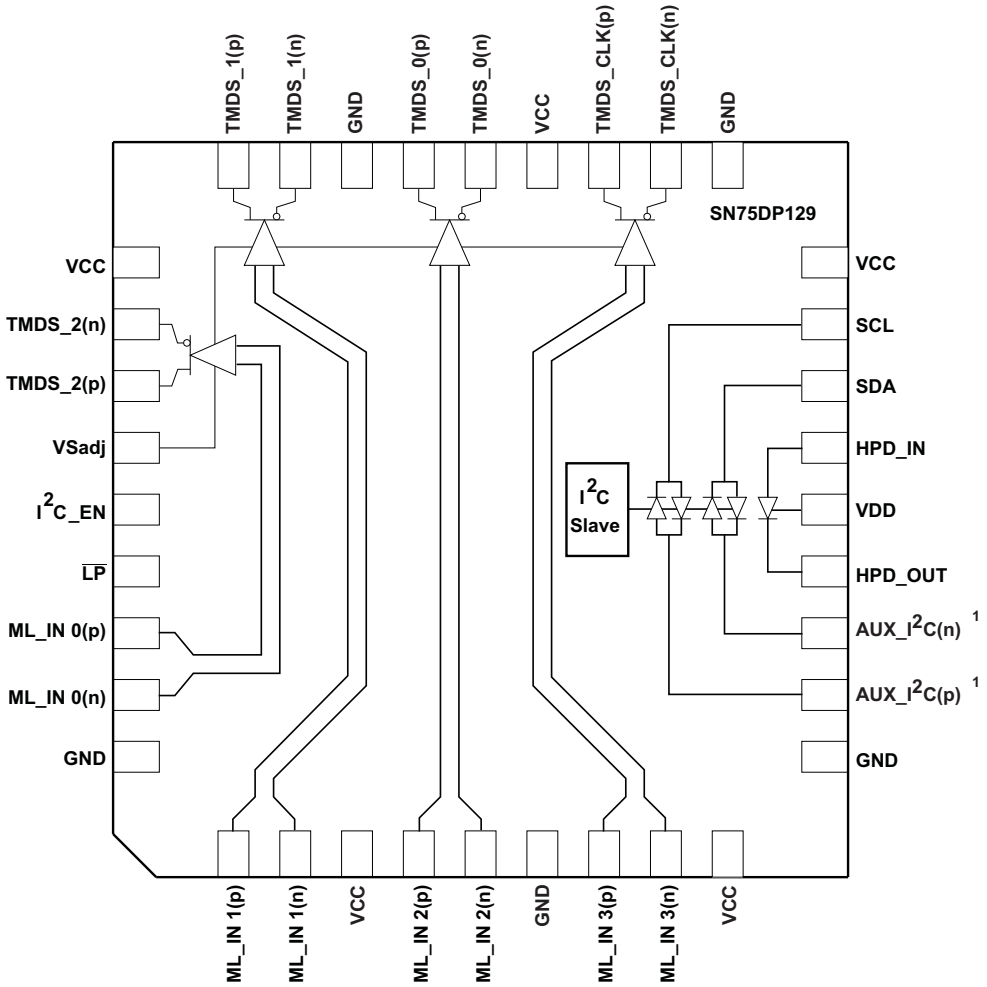
DP++—Dual-Mode DisplayPort

TMDS—Transition-Minimized Differential Signaling

DVI—Digital Visual Interface

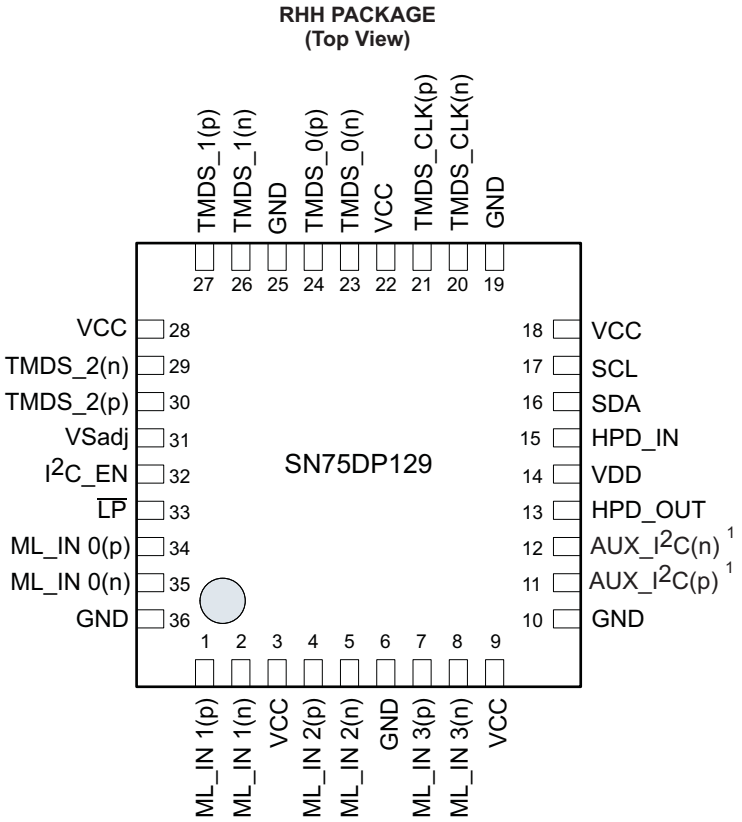
HDMI—High Definition Multimedia Interface

INTERNAL DATA CONNECTION DIAGRAM



(1) I^2C bus data (n-SDA) and clock (p-SCL) lines.

PIN CONFIGURATION



(1) I^2C bus data (n-SDA) and clock (p-SCL) lines.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION	TYPE
NAME	NO.(1)			
AUX_I^2C(2)	11(p), 12(n)	I/O	Source Side Bidirectional DisplayPort Auxiliary Data Line	DDC LINK (Source)
GND	6, 10, 19, 25, 36		Ground	Ground
HPD_IN	15	I	Hot Plug Detect (HPD) Input	Hot Plug Detect
HPD_OUT	13	O	Hot Plug Detect (HPD) Output	Hot Plug Detect
I^2C_EN	32	I	Internal I^2C register enable, used for HDMI / DVI connector differentiation	Control
$\overline{LP}$	33	I	Low Power Select Bar	Control
ML_IN 0	34(p), 35(n)	I	DisplayPort Main Link Channel 0 Differential Input	Main Link Input Pins
ML_IN 1	1(p), 2(n)	I	DisplayPort Main Link Channel 1 Differential Input	Main Link Input Pins
ML_IN 2	4(p), 5(n)	I	DisplayPort Main Link Channel 2 Differential Input	Main Link Input Pins
ML_IN 3	7(p), 8(n)	I	DisplayPort Main Link Channel 3 Differential Input	Main Link Input Pins
TMDS_2	30(p), 29(n)	O	TMDS Data 2 Differential Output	Main Link Output
TMDS_1	27(p), 26(n)	O	TMDS Data 1 Differential Output	Main Link Output
TMDS_0	24(p), 23(n)	O	TMDS Data 0 Differential Output	Main Link Output
TMDS_CLK	21(p), 20(n)	O	TMDS Data Clock Differential Output	Main Link Output
SCL	17	I/O	TMDS Port Bidirectional I^2C Clock Line	DDC Link (Sink)
SDA	16	I/O	TMDS Port Bidirectional I^2C Data Line	DDC Link (Sink)
VCC	3, 9, 18, 22, 28		3.3 V Supply	Voltage Supply

(1) (p) Positive; (n) Negative
(2) I^2C bus data (n-SDA) and clock (p-SCL) lines.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION	TYPE
NAME	NO.(1)			
VDD	14		HPD Supply	Voltage Supply
VSadj	31	I	TMDS-Compliant Voltage Swing Control	Reference

Input/Output Equivalent Circuits

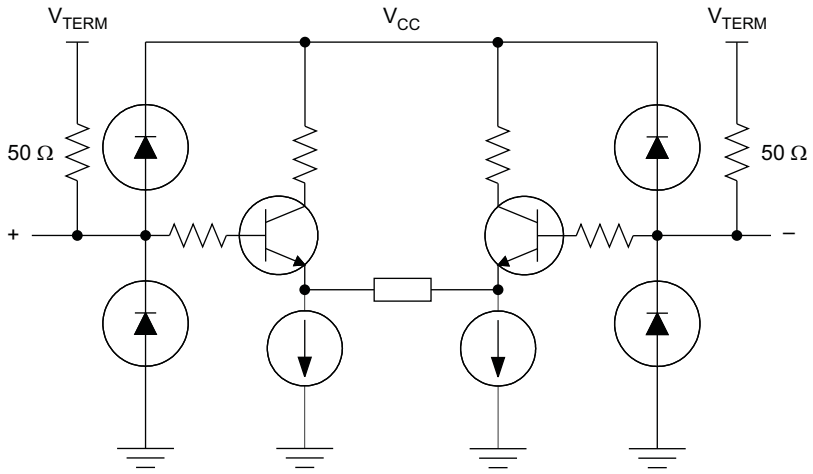


Figure 1. DisplayPort Input Stage

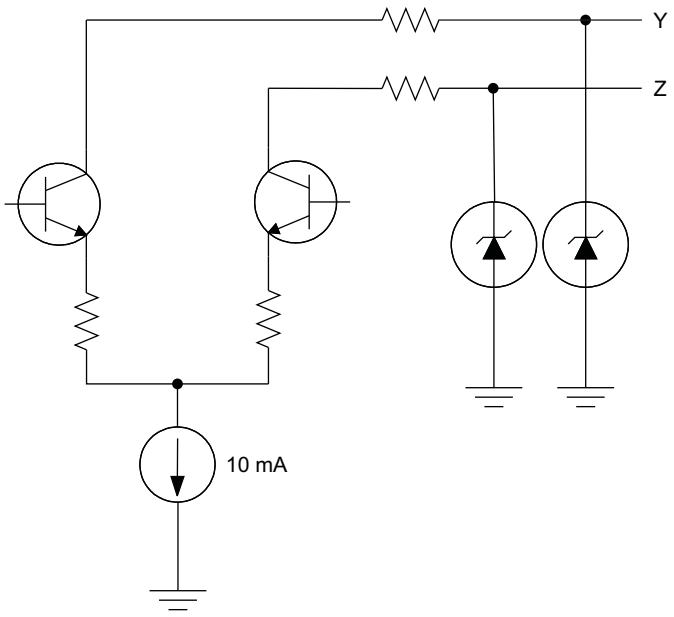


Figure 2. TMDS Output Stage

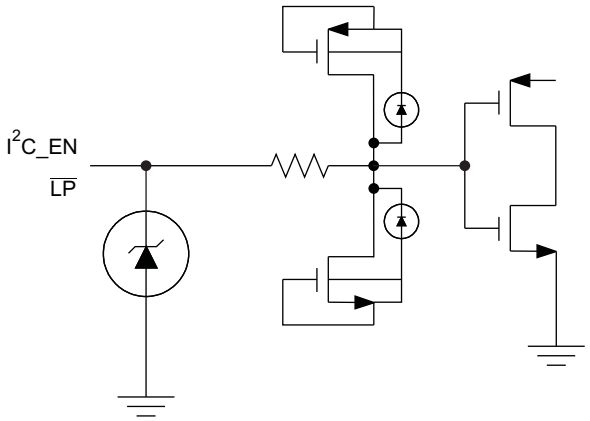


Figure 3. HPD and Control Input Stage

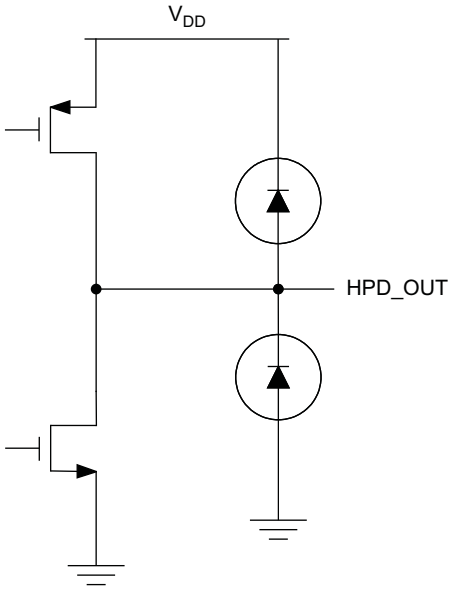


Figure 4. HPD Output Stage

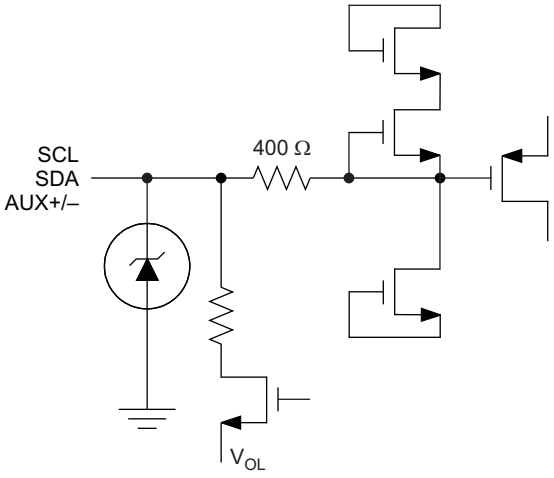


Figure 5. I²C Input and Output Stage

Table 1. Control Pin Lookup Table(1)

SIGNAL	LEVEL	STATE	DESCRIPTION
$\overline{LP}$	H	Normal Mode	Normal operational mode for device
	L	Low Power Mode	Device is forced into a Low Power state causing the outputs to go to a high impedance state. All other inputs are ignored.
I^2C_EN	H	HDMI	Internal I^2C register is active and readable, indicating the connector in use is HDMI-compliant.
	L	DVI	Internal I^2C register is disabled and unreadable, indicating the connector in use is DVI-compliant.
VS_{adj}	4.65 kΩ	Compliant Voltage Swing	Driver output voltage swing precision control to aid with system compliance.

(1) (H) Logic High; (L) Logic Low

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75DP129RHHR	DP129	36-pin QFN Reel (large)
SN75DP129RHHT	DP129	36-pin QFN Reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	VCC	–0.3 to 3.6	V
Supply voltage range	VDD	–0.3 to 3.6	V
Voltage range	Main link I/O (ML_IN x, DP_SINK x) differential voltage	1.5	V
	TMDS I/O	–0.3 to 4	V
	HPD I/O	–0.3 to 5.5	V
	Auxiliary I/O	–0.3 to 5.5	V
	Control I/O	–0.3 to 5.5	V
Electrostatic discharge	Human body model(3)	±12000	V
	Charged-device model(4)	±1000	V
	Machine model(5)	±200	V
Continuous power dissipation		See Dissipation Ratings Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
36-pin QFN (RHH)	Low-K	1398 mW	13.98 mW/°C	559 mW
	High-K	2941 mW	29.41 mW/°C	1176 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			9.44(1)		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			24.74		°C/W
P_D	Device power dissipation(2)	$\overline{LP}$ = 3.3 V, ML: V_{ID} = 500 mV, 2.5 Gbps PRBS; I^2C: V_{ID} = 3.3 V, 100 Kbps PRBS; HPD = 5 V		380	490	mW
P_{SD}	Device power dissipation under low power	$\overline{LP}$ = 0 V		5	20	µW

(1) The maximum rating is simulated under 3.6 V V_{CC} and V_{DD} unless otherwise noted.
(2) Power disipation is the sum of the power consumption from the V_{CC} and V_{DD} pins, plus the 132 mW of power from the AVCC (Receiver Termination Supply).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{DD}	Supply voltage	1.65		3.6	V
T_A	Operating free-air temperature	0		85	°C
MAIN LINK DIFFERENTIAL INPUT PINS					
V_{ID}	Peak-to-peak input differential voltage	0.15		1.40	V
d_R	Data rate			2.5	Gbps
TMDS DIFFERENTIAL OUTPUT PINS					
AV_{CC}	TMDS output termination voltage	3	3.3	3.6	V
d_R	Data rate			2.5	Gbps
R_t	Termination resistance	45	50	55	Ω
AUXILIARY AND I^2C PINS					
V_I	Input voltage	0		5.5	V
$d_{R(I2C)}$	I2C data rate			100	kHz
HPD AND CONTROL PINS					
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V

Device Power

The SN75DP129 is designed to operate from one or two supply voltages, depending on the implementation of the integrated Hot Plug Detect (HPD) level translator. The TMDS level translator is powered from a single 3.3-V supply. The HPD translator is powered using the VDD pin and its voltage can range from 1.8 V to 3.3 V. This voltage determines the HIGH-level output voltage of the HPD_OUT pin.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	LP = 3.6 V, V_{CC} = V_{DD}, ML: V_{ID} = 500 mV, 2.7 Gbps PRBS AUX: V_I = 3.3 V, 100 kHz PRBS HPD: HPD_IN = 5 V	50	75	112	mA
I_{DD}	Supply current			1	2	mA
ISD	Shutdown current	$\overline{LP}$ = 0 V		1	5	µA

Hot Plug and Cable Adapter Detect

The SN75DP129 has a built-in level shifter for the HPD outputs. The output voltage level of the HPD pin is defined by the voltage level of the VDD pin.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH3.3}$	High-level output voltage	I_{OH} = –100 µA, $V_{DD\times1}$ = 3.3 V	3		3.3	V
$V_{OH2.5}$		I_{OH} = –100 A, $V_{DD\times1}$ = 2.5 V	2.25		2.5	V
$V_{OH1.8}$		I_{OH} = –100 A, $V_{DD\times1}$ = 1.8 V	1.62		1.8	V
V_{OL}	Low-level output voltage	I_{OH} = 100 µA	0		0.4	V
I_H	High-level input current	V_{IH} = 2.0 V, V_{DD} = 3.6 V	–10		10	µA
I_L	Low-level input current	V_{IL} = 0.8 V, V_{DD} = 3.6 V	–10		10	µA

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(HPD)}$	Propagation delay	V_{DD} = 3.6 V	5		30	ns

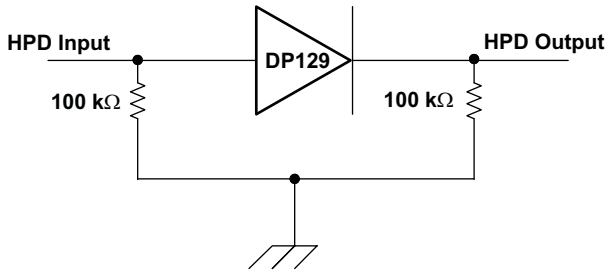


Figure 6. HPD Test Circuit

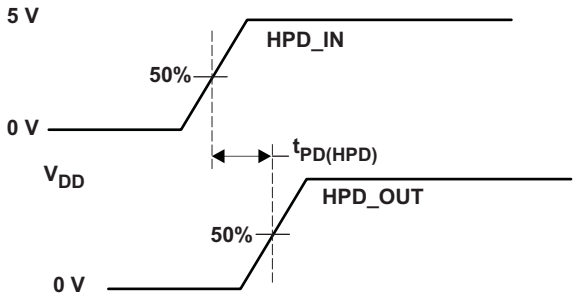


Figure 7. HPD Timing Diagram

AUX / I²C Pins

The SN75DP129 utilizes an active I^2C repeater. The repeater isolates the parasitic effects of the system to aid with system level compliance.

In addition to the I^2C repeater, the SN75DP129 supports the connector detection I^2C register. This register is enabled using the I2C_EN pin. When active, an internal memory register is readable using the AUX_I^2C pins. This I^2C register block functionality is described in the APPLICATION INFORMATION section.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	Low input current		V_{CC} = 3.6 V, V_I = 0 V	–10		10	µA
$I_{lkg(AUX)}$	Input leakage current	AUX_I^{2}C pins	V_{CC} = 3.6 V, V_I = 3.6 V	–10		10	µA
$C_{IO(AUX)}$	Input/output capacitance	AUX_I^{2}C pins	DC bias = 1.65 V, AC = 2.1 V_{p-p}, f = 100 kHz			15	pF
$V_{IH(AUX)}$	High-level input voltage	AUX_I^{2}C pins		1.6		5.5	V
$V_{IL(AUX)}$	Low-level input voltage	AUX_I^{2}C pins		–0.2		0.4	V
$V_{OL(AUX)}$	Low-level output voltage	AUX_I^{2}C pins	I_O = 4 mA	0.5		0.6	V
$I_{lkg(I2C)}$	Input leakage current	I^{2}C SDA/SCL pins	V_{CC} = 3.6 V, V_I = 4.95 V	–10		10	µA
$C_{IO(I2C)}$	Input/output capacitance	I^{2}C SDA/SCL pins	DC bias = 2.5 V, AC = 3.5 V_{p-p}, f = 100 kHz			15	pF
$V_{IH(I2C)}$	High-level input voltage	I^{2}C SDA/SCL pins		2.1		5.5	V
$V_{IL(I2C)}$	Low-level input voltage	I^{2}C SDA/SCL pins		–0.2		1.5	V
$V_{OL(I2C)}$	Low-level output voltage	I^{2}C SDA/SCL pins	I_O = 4 mA			0.2	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Propagation delay time, low to high	Source to Sink	204		459	ns
t_{PHL1}	Propagation delay time, high to low	Source to Sink	35		200	ns
t_{PLH2}	Propagation delay time, low to high	Sink to Source	80		251	ns
t_{PHL2}	Propagation delay time, high to low	Sink to Source	35		200	ns
t_{f1}	Output signal fall time	Sink Side	20		72	ns
t_{f2}	Output signal fall time	Source Side	20		72	ns
f_{SCL}	SCL clock frequency for internal register	Source Side			100	kHz
$t_{W(L)}$	Clock LOW period for I^{2}C register	Source Side	4.7			µs
$t_{W(H)}$	Clock HIGH period for internal register	Source Side	4.0			µs
t_{SU1}	Internal register setup time, SDA to SCL	Source Side	250			ns
$t_{h(1)}$	Internal register hold time, SCL to SDA	Source Side	0			µs
$t_{(buf)}$	Internal register bus free time between STOP and START	Source Side	4.7			µs
$t_{su(2)}$	Internal register setup time, SCL to START	Source Side	4.7			µs
$t_{h(2)}$	Internal register hold time, START to SCL	Source Side	4.0			µs
$t_{su(3)}$	Internal register hold time, SCL to STOP	Source Side	4.0			µs

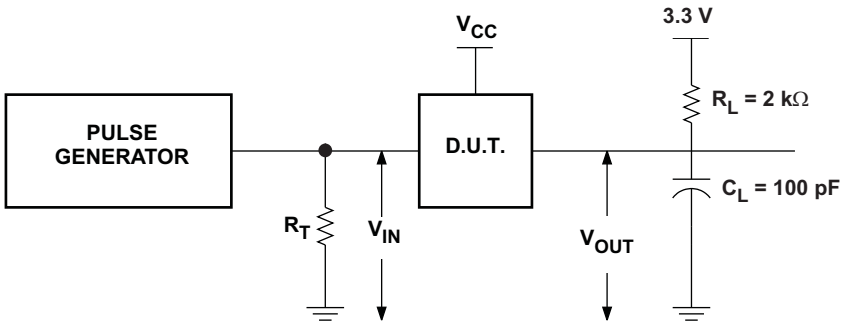


Figure 8. Source Side Test Circuit (AUX_I^{2}C)

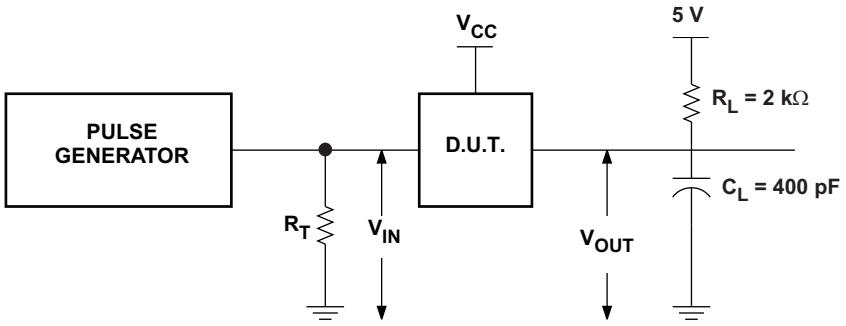


Figure 9. Sink Side Test Circuit (SCL, SDA)

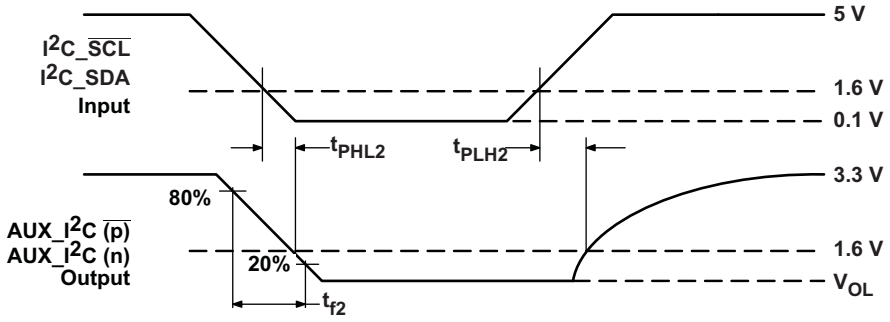


Figure 10. Source Side Output AC Measurements

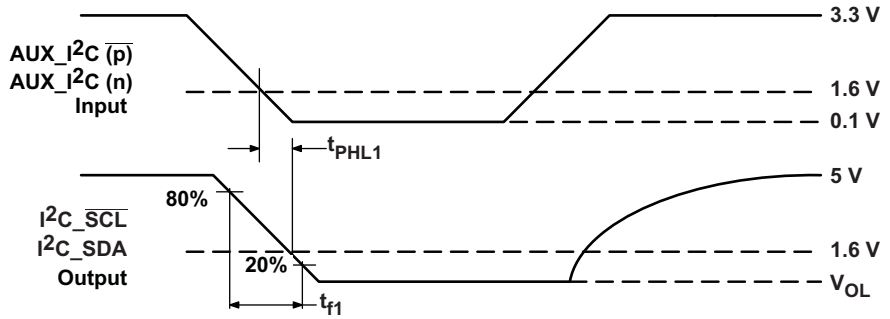


Figure 11. Sink Side Output AC Measurements

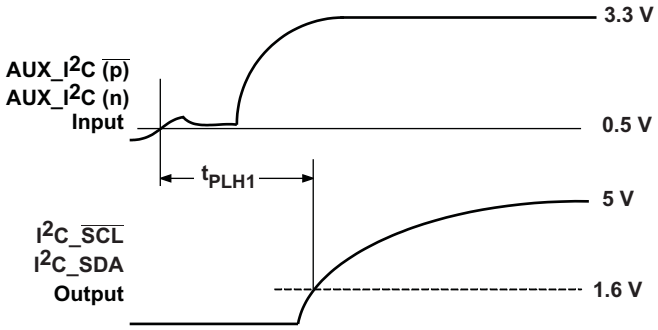


Figure 12. Sink Side Output AC Measurements (continued)

TMDS and Main Link Pins

The main link inputs are designed to be compliant with the DisplayPort 1.1 specification. The TMDS outputs of the SN75DP129 are designed to be compliant with the Digital Visual Interface 1.0 (DVI) and High Definition Multimedia Interface 1.3 (HDMI) specifications. The differential output voltage swing can be fine-tuned with the VSadj (TMDS-compliant Voltage Swing Control) resistor.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Single-ended HIGH level output voltage	AVCC = 3.3 V, R_T = 50 Ω	AVCC–10		AVCC+10	mV
V_{OL}	Single-ended LOW level output voltage		AVCC–600		AVCC–400	mV
V_{SWING}	Single-ended output voltage swing		400		600	mV
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–5		5	mV
$V_{OD(PP)}$	Peak-to-peak output differential voltage		800		1200	mV
$V_{(O)SBY}$	Single-ended standby output voltage	AVCC = 3.3 V, R_T = 50 Ω, LP = 0	AVCC–10		AVCC+10	mV
$I_{(O)OFF}$	Single-ended power down output current	0 V ≤ V_{CC} ≥ 1.5 V, AVCC = 3.3 V, R_T = 50 Ω	–10		10	µA
I_{OS}	Short circuit output current	V_{ID} = 500 mV	–15		15	mA
R_{INT}	Input termination impedance		45	50	55	Ω
V_{term}	Input termination voltage		1		2	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time	AVCC = 3.3 V, R_T = 50 Ω, f = 1 MHz	250	350	600	ps
t_{PHL}	Propagation delay time		250	350	600	ps
t_R	Rise time		60	90	140	ps
t_F	Fall time		60	90	140	ps
$t_{SK(P)}$	Pulse skew			8	15	ps
$t_{SK(D)}$	Intra-pair skew			20	40	ps
$t_{SK(O)}$	Inter-pair skew			20	65	ps
$t_{JITD(PP)}$	Peak-to-peak output residual data jitter	AVCC = 3.3 V, R_T = 50 Ω, dR = 2.5 Gbps		14	50	ps
$t_{JITC(PP)}$	Peak-to-peak output residual clock jitter	AVCC = 3.3 V, R_T = 50 Ω, f = 250 MHz		8	30	ps

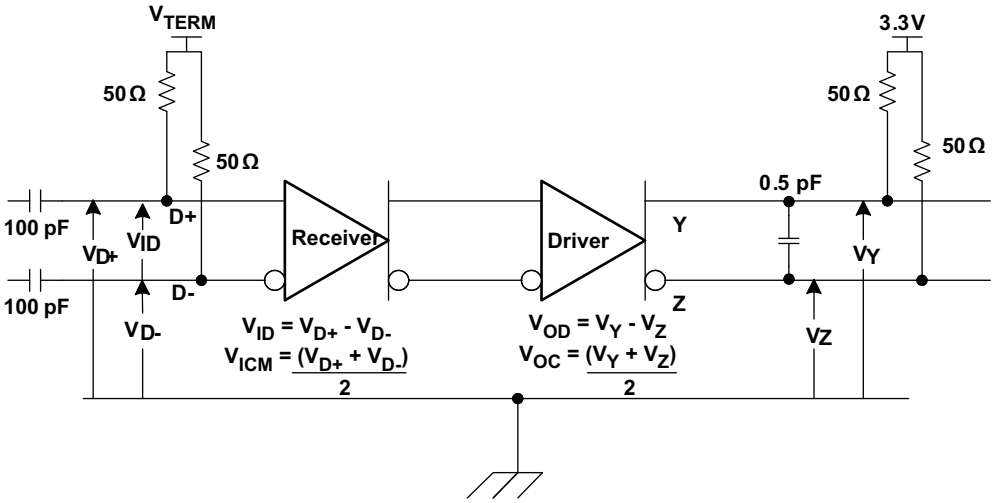


Figure 13. TMDS Main Link Test Circuit

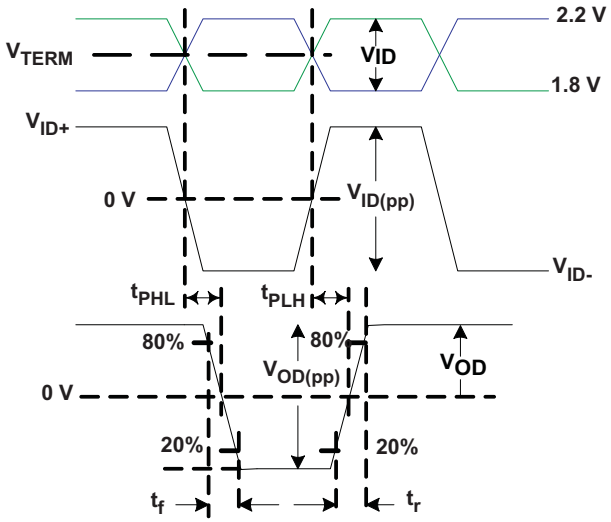


Figure 14. TMDS Main Link Timing Measurements

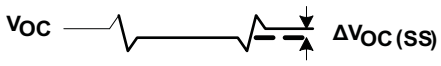
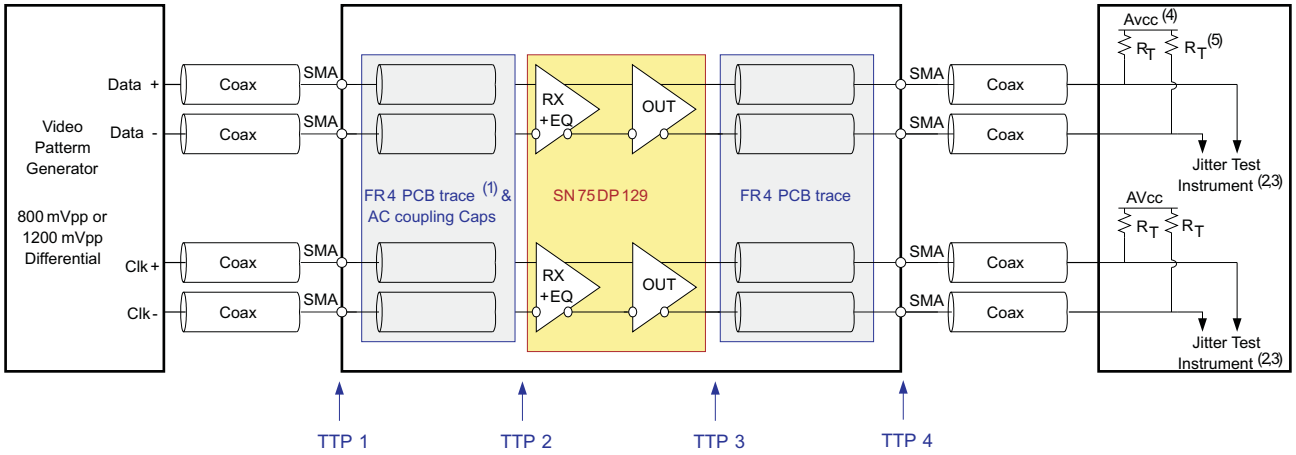


Figure 15. TMDS Main Link Common Mode Measurements



(1) The FR4 trance between TTP1 and TTP2 is designed to emulate 8 inches of FR4, a connector, and another 8 inches if FR4.

(2) All jitter is measured at a BER of 10^{-12}

(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1.

(4) AVCC = 3.3 V

(5) R_T = 50 Ω

Figure 16. TMDS Jitter Measurements

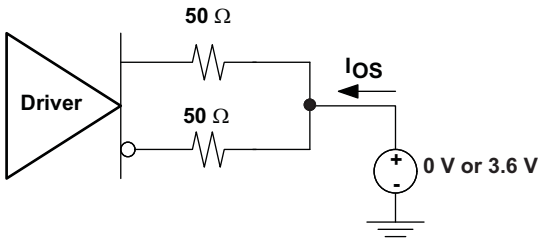


Figure 17. TMDS Main Link Short Circuit Output Circuit

TYPICAL CHARACTERISTICS

Power disipation is the sum of the power consumption from the VCC and VDD pins, plus the 132 mW of power from the AVCC (Receiver Termination Supply).

POWER DISSIPATION vs DATA RATE

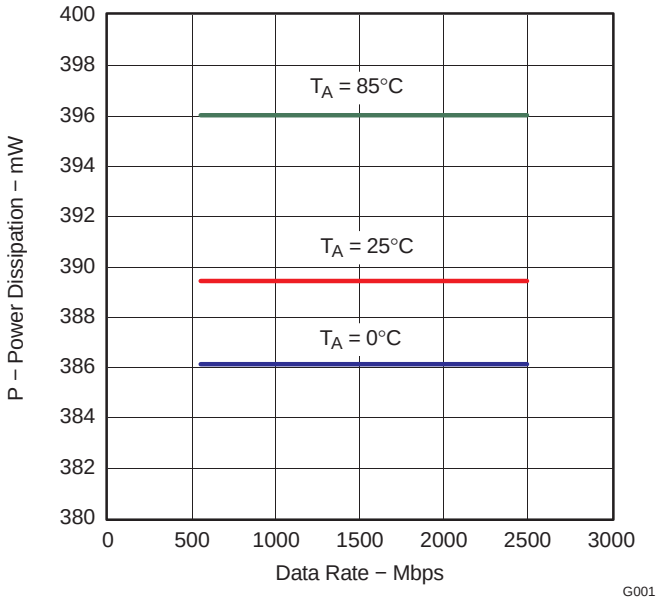


Figure 18.

PEAK-TO-PEAK RESIDUAL DATA JITTER (at 2.5 Gbps) vs SUPPLY VOLTAGE

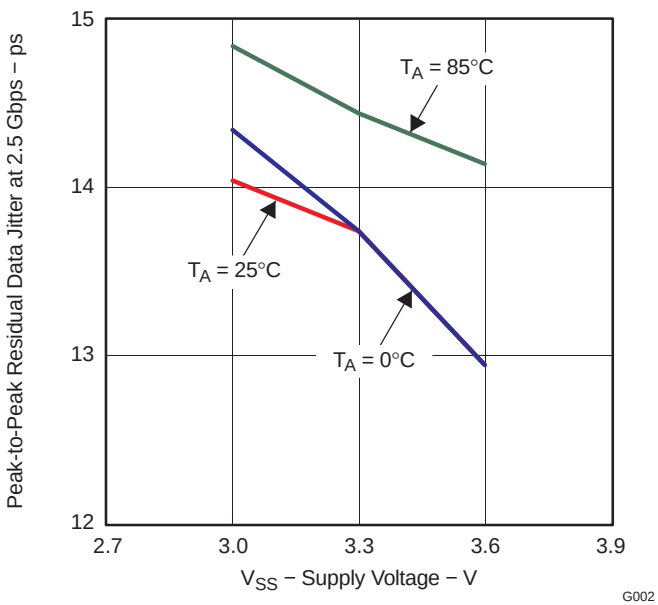


Figure 19.

PEAK-TO-PEAK RESIDUAL DATA JITTER vs DATA RATE

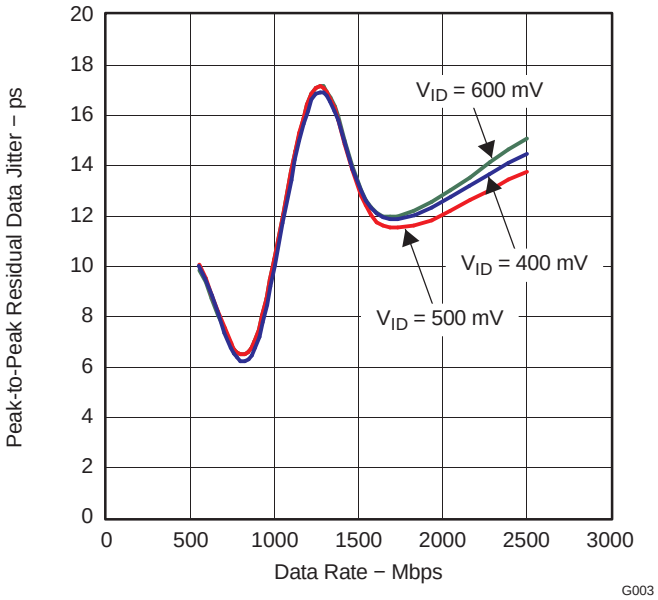


Figure 20.

GAIN vs FREQUENCY

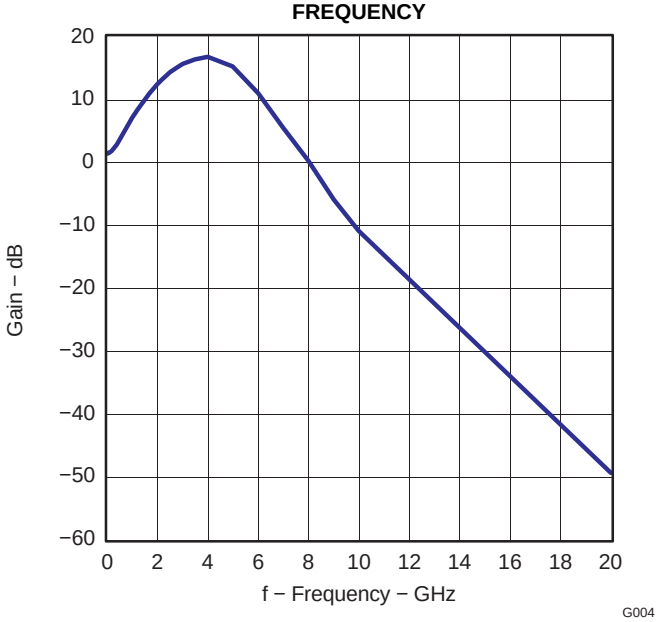


Figure 21.

TYPICAL CHARACTERISTICS (continued)

Power disipation is the sum of the power consumption from the VCC and VDD pins, plus the 132 mW of power from the AVCC (Receiver Termination Supply).

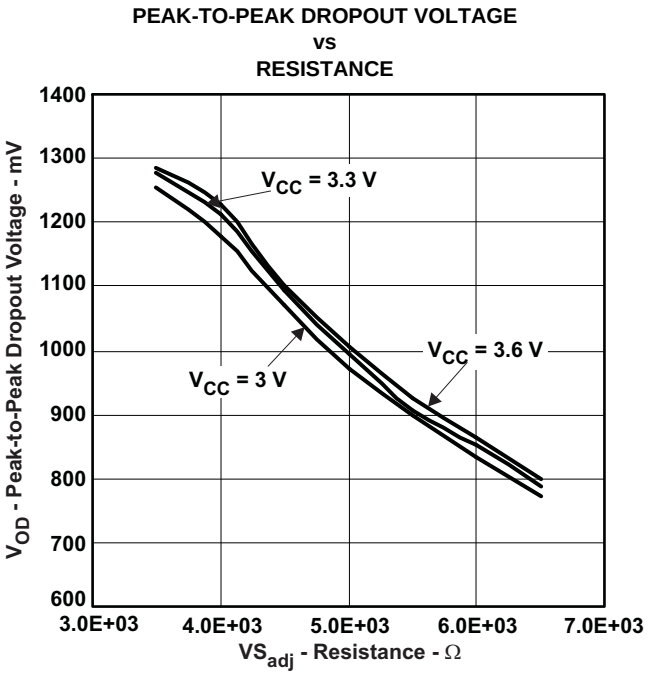


Figure 22.

APPLICATION INFORMATION

I²C INTERFACE NOTES

The I²C interface can access the internal memory of the SN75DP129. I²C is a two-wire serial interface developed by Philips Semiconductor (see I2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device. The SN75DP129 works as a slave and supports the standard mode transfer (100 kbps) as defined in the I²C-Bus Specification.

The basic I²C start and stop access cycles are shown in Figure 23.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

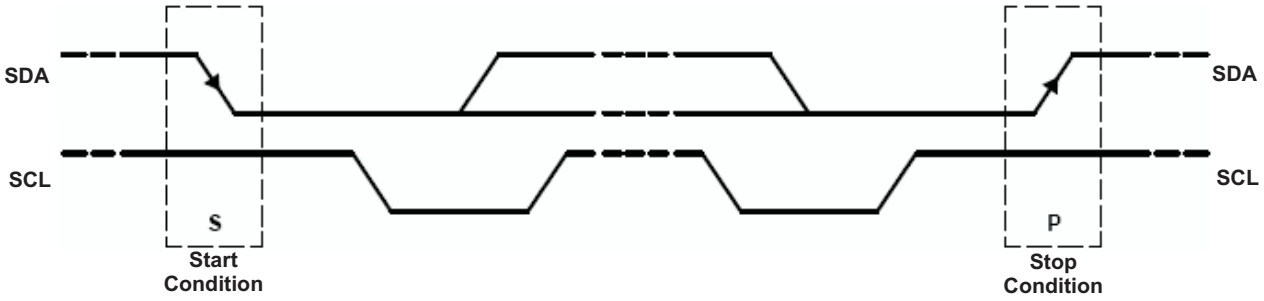


Figure 23. I²C Start and Stop Conditions

GENERAL I²C PROTOCOL

- The master initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line the SCL line is high, as shown in Figure 25. All I²C-compliant devices should recognize a *start condition*.
- The master generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 24). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 25) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to transmit data to the slave (R/W bit 0) or *receive* data from the slave (R/W bit 1). In either case, the *receiver* needs to acknowledge the data sent by the *transmitter*. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 26).
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 26). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* ,followed by a matching address.

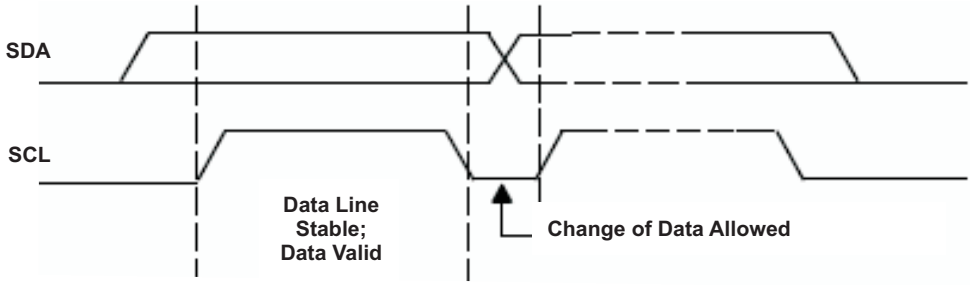


Figure 24. I²C Bit Transfer

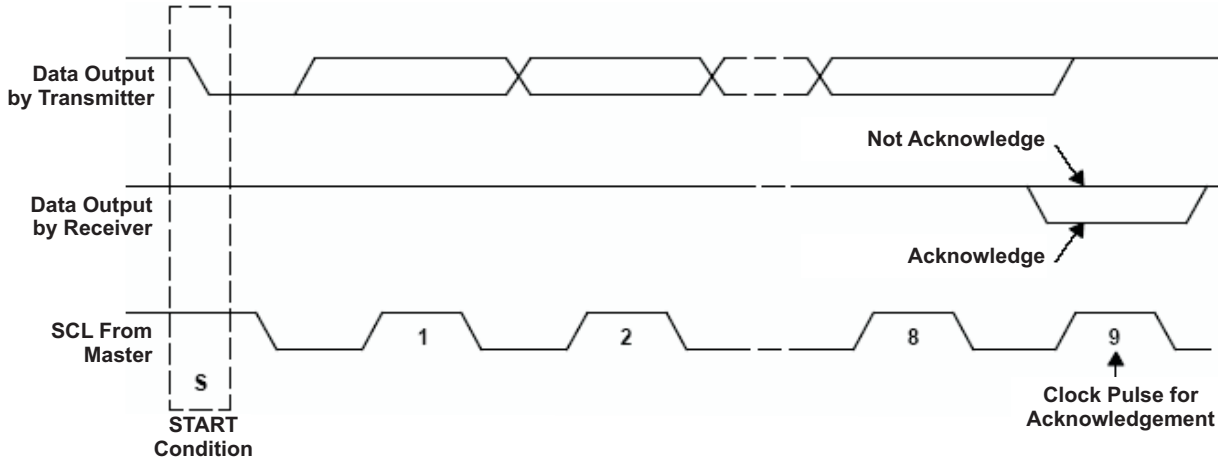


Figure 25. I²C Acknowledge

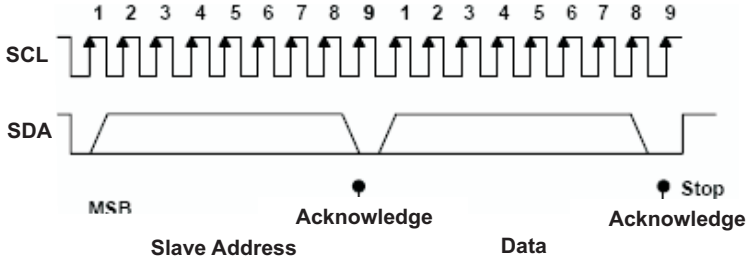


Figure 26. I²C Address and Data Cycles

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 27 and Figure 28. See the Reading from the SN75DP129, an example section for more information.

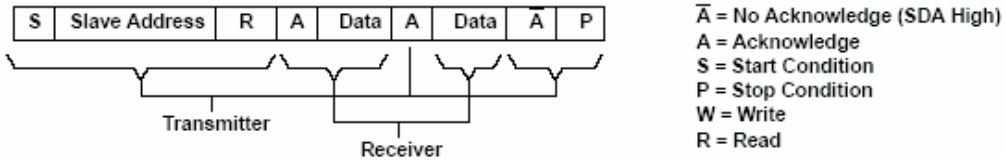


Figure 27. I²C Read Cycle

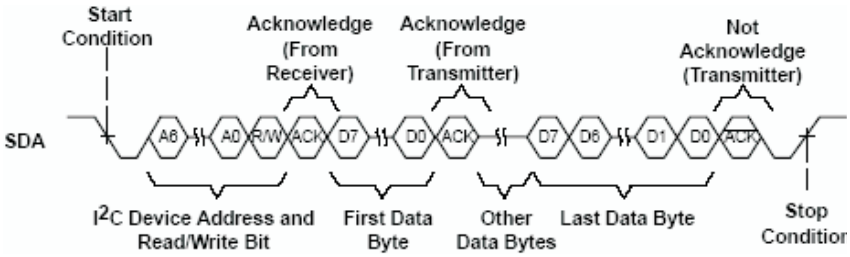


Figure 28. Multiple Byte Read Transfer

Slave Address

Both SDA and SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I^2C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The 7 bit address is factory preset to 1000000. Table 2 lists the calls that the SN75DP129 will respond to.

Table 2. SN75DP129 Slave Address

FIXED ADDRESS							READ/WRITE BIT
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (R/W)
1	0	0	0	0	0	0	1

Sink Port Selection Register and Source Plug-In Status Register Description (Sub-Address)

The SN75DP129 operates using a multiple byte transfer protocol similar to Figure 28. The internal memory of the SN75DP129 contains the phrase *DP-HDMI ADAPTOR<EOT>* converted to ASCII characters. The internal memory address registers and the corresponding values can be found in Table 3.

During a read cycle, the SN75DP129 sends the data (within its selected sub-address) in a single transfer to the master device requesting the information. See the Reading from the SN75DP129, an Example section of this data sheet for the proper procedure.

Table 3. SN75DP129 Sink Port and Source Plug-In Status Registers Selection

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	0x10
Data	44	50	2D	48	44	4D	49	20	41	44	41	50	54	4F	52	04	FF

READING FROM THE SN75DP129, AN EXAMPLE

The read operation consists of several steps. The I^2C master begins the communication with the transmission of the start sequence, followed by the slave address of the SN75DP129 and logic address of **00h**. The SN75DP129 acknowledges it's presence to the master and begins to transmit the memory registers contents . After each byte is transferred, the SN75DP129 waits for an acknowledge (ACK) or a not-acknowledge (NACK) from the master. If an ACK is received, the next byte of data is transmitted. If a NACK is received, the data transmission sequence is expected to end and the master should send the stop command.

The SN75DP129 continues to send data until the master fails to acknowledge each byte transmission. If an ACK is received after the transmission of byte **0x0F**, the SN75DP129 transmits byte **0x10** and continues to transmit byte **0x10** for all further ACK's until a NACK is received.

SN75DP129 Read Phase

Step 1(1)	**0**
I^2C Start (Master)	S

(1) The SN75DP129 also supports an accelerated read mode in which steps 1 through 6 can be skipped.

Step 2	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^2C General Address Write (Master)	1	0	0	0	0	0	0	0

Step 3	**9**
I^2C Acknowledge (Slave)	A

Step 4	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^2C Logic Address (Master)	1	0	0	0	0	0	0	0

Step 5	**9**
I^2C Acknowledge (Slave)	A

Step 6	**0**
I^2C Stop (Master)	P

Step 7	**0**
I^2C Start (Master)	S

Step 8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^2C General Address Read (Master)	1	0	0	0	0	0	0	1

Step 9	**9**
I^2C Acknowledge (Slave)	A

Step 10	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the Logic values Contained in the Sink Port Register

Step 11	**9**
I^2C Not-Acknowledge (Master)	X

Where X is an A (Acknowledge) or $\overline{A}$ (Not-Acknowledge)
An A causes the pointer to increment and step 10 is repeated.
An $\overline{A}$ causes the slave to stop transmitting and proceeds to step 12.

Step 12	**0**
I^2C Stop (Master)	P

Revision History

Changes from Original (January 2008) to Revision A **Page**

- Changed device power dissipation from 250 mW typ to 380 mW typ 8
- Changed device power dissipation from 400 mW max to 490 mW max 8
- Changed propagation delay time, high to low, sink to source from 140 ns max to 200 ns max 10
- Changed t_{PHL1} to t_{PLH1} in Figure 12 11
- Changed t_{PHL} propagation delay time from 800 ps max to 600 ps max 12
- Changed $t_{JITD(PP)}$ peak-to-peak output residual data jitter from 20 ps typ to 14 ps typ 12
- Changed $t_{JITC(PP)}$ peak-to-peak output residual clock jitter from 10 ps typ to 8 ps typ 12
- Added peak-to-peak dropout voltage vs resistance curves 16

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75DP129RHHR	Active	Production	VQFN (RHH) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP129
SN75DP129RHHT	Active	Production	VQFN (RHH) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP129

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

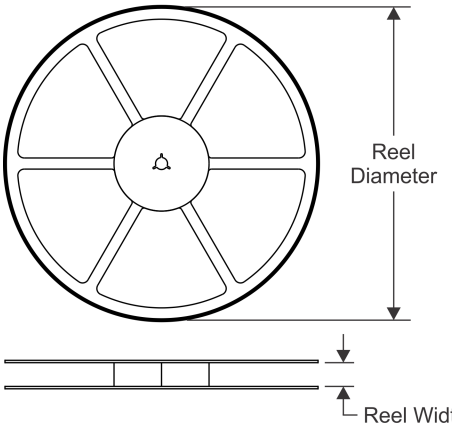
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

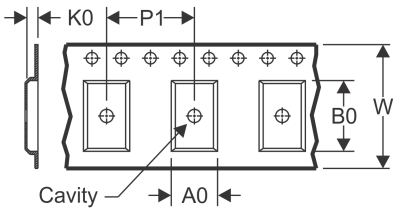
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

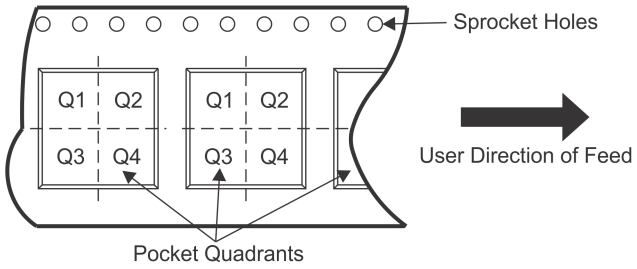


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

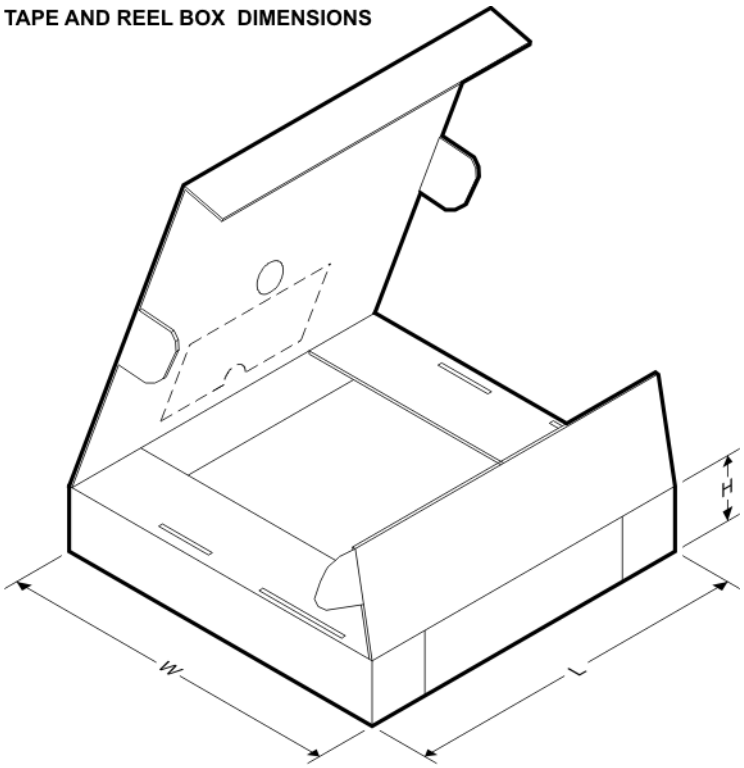
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP129RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
SN75DP129RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP129RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
SN75DP129RHHT	VQFN	RHH	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

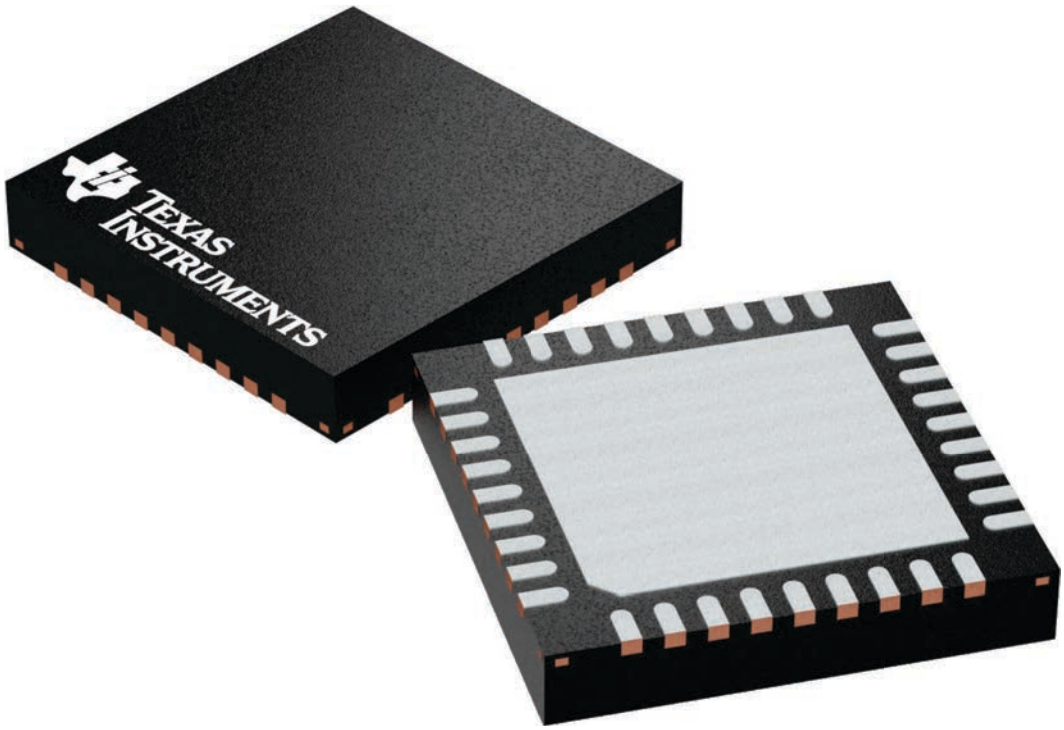
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



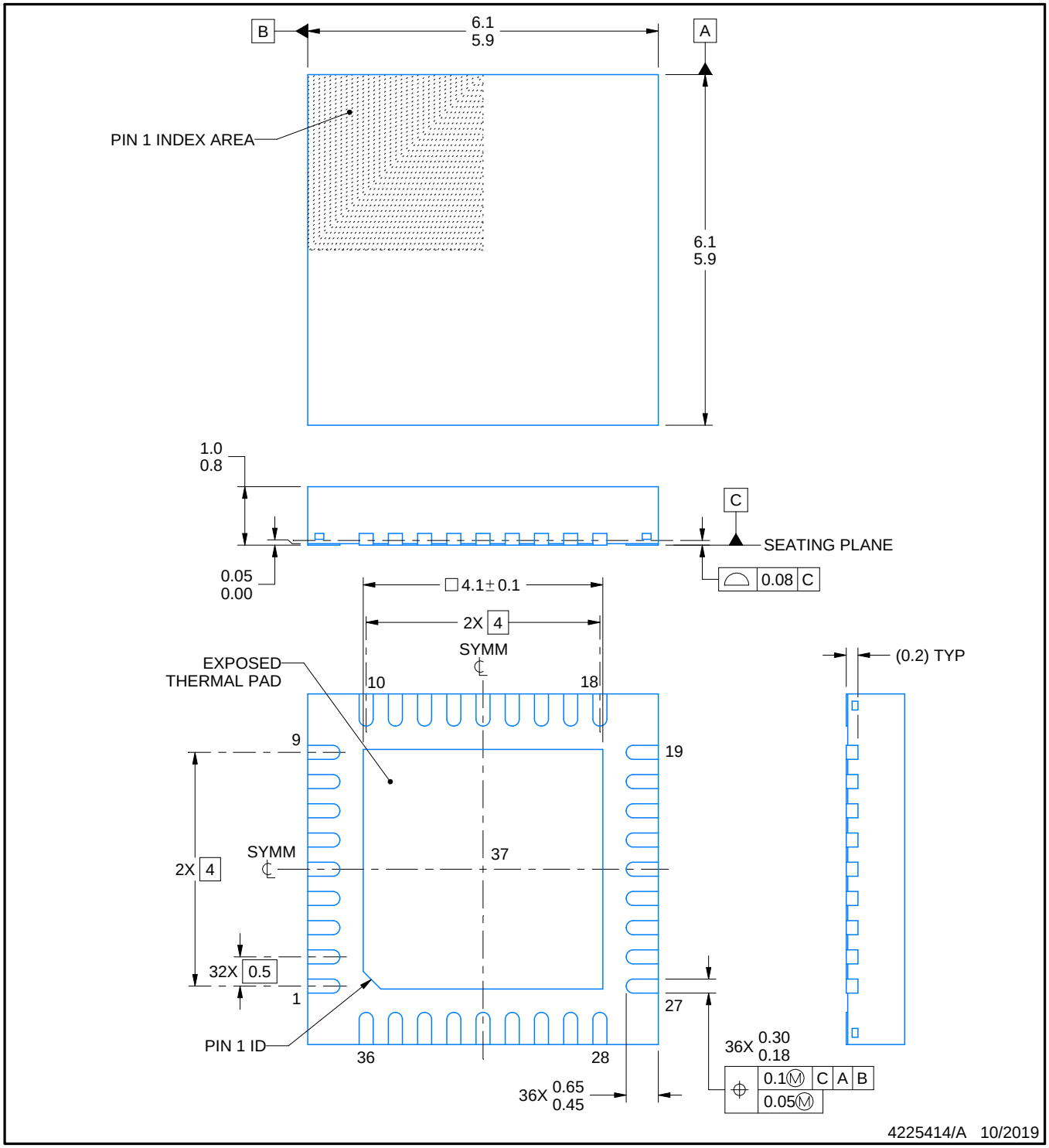
4225440/A

RHH0036B

PACKAGE OUTLINE

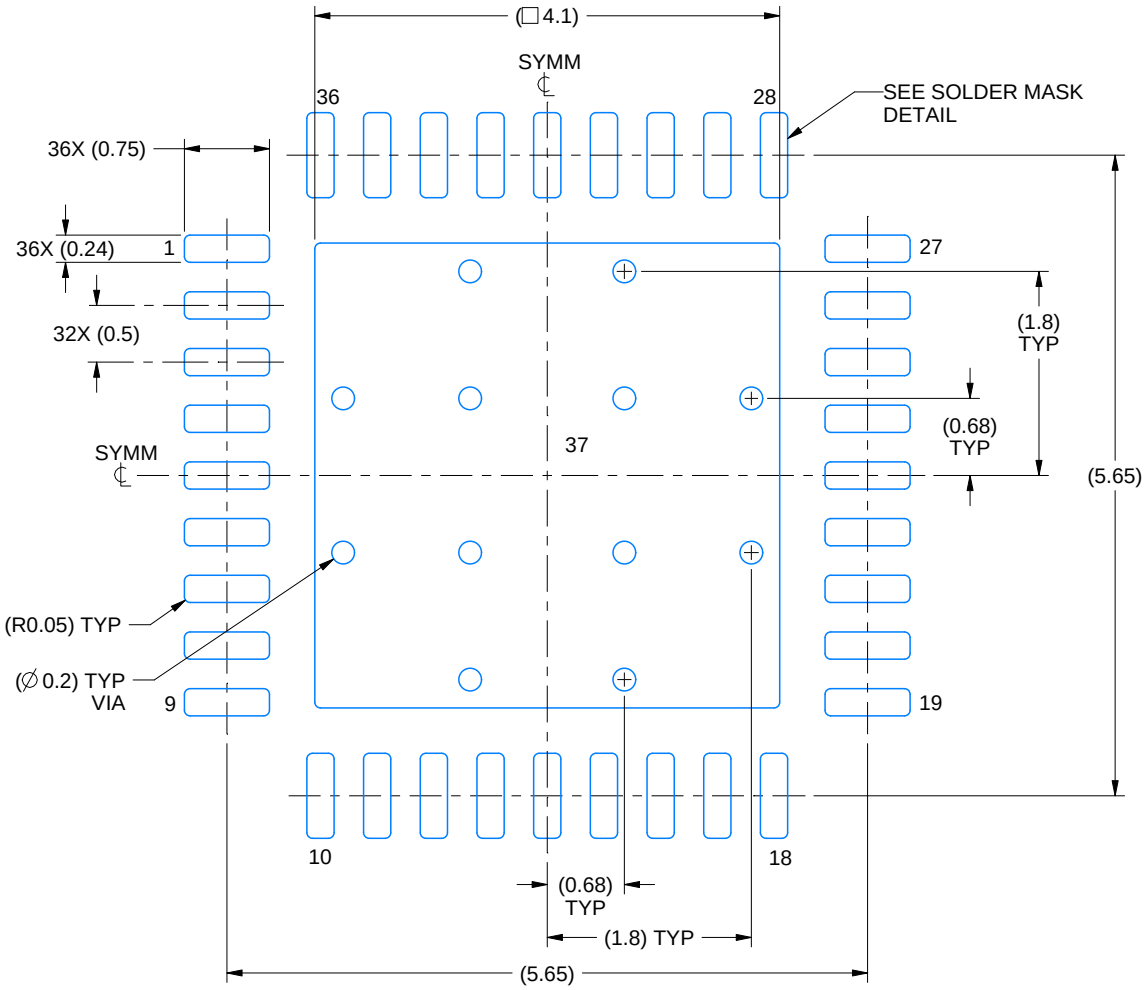
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

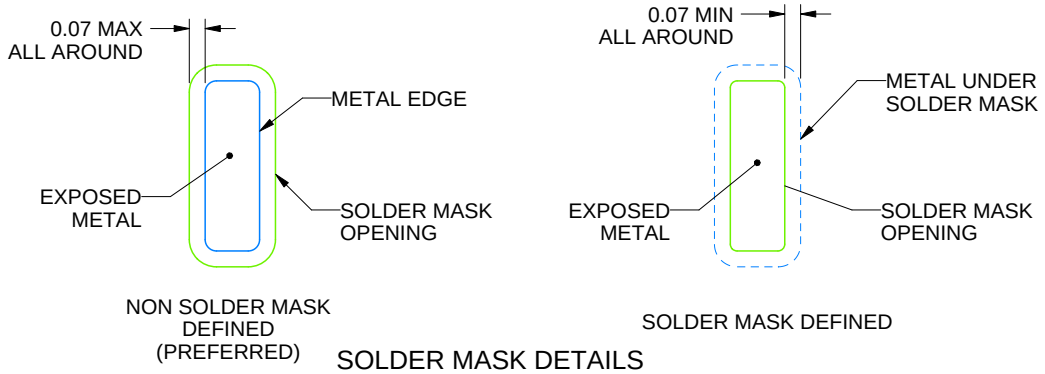


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

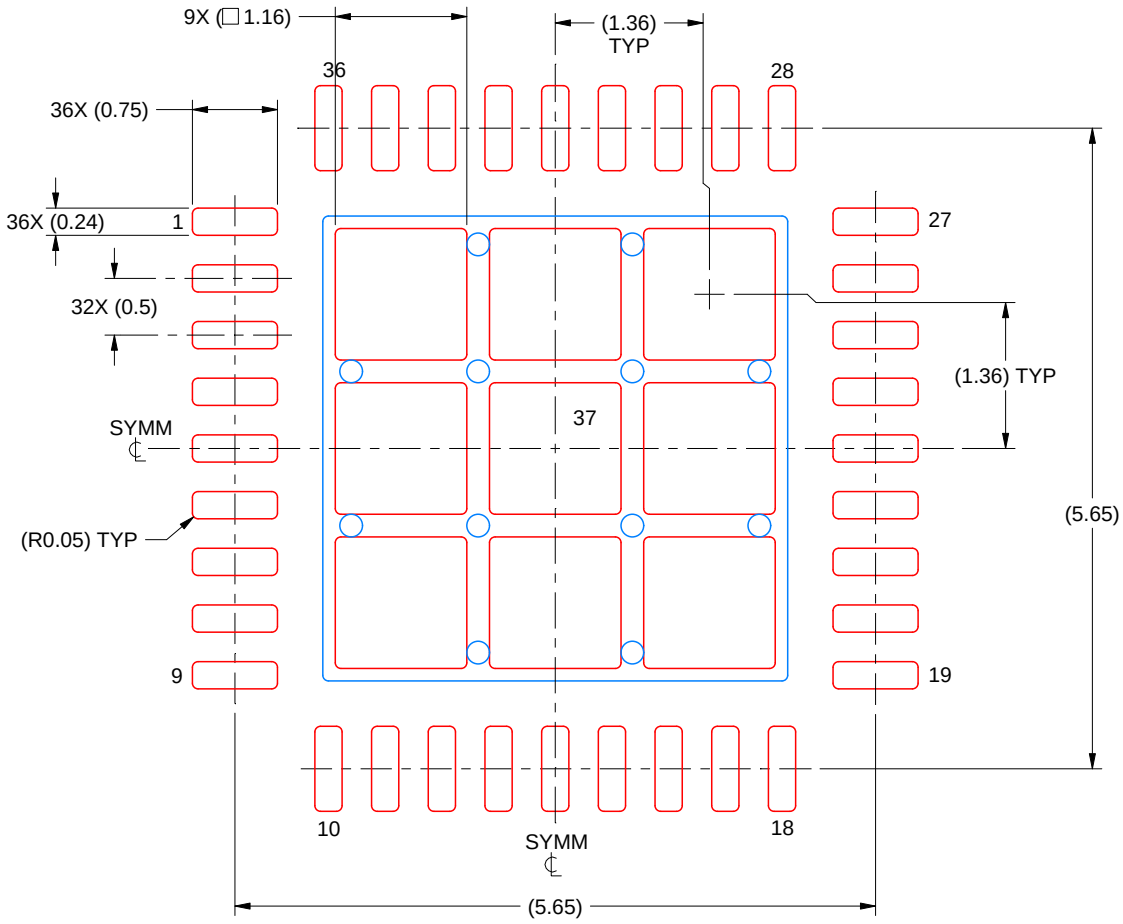


SOLDER MASK DETAILS

4225414/A 10/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225414/A 10/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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