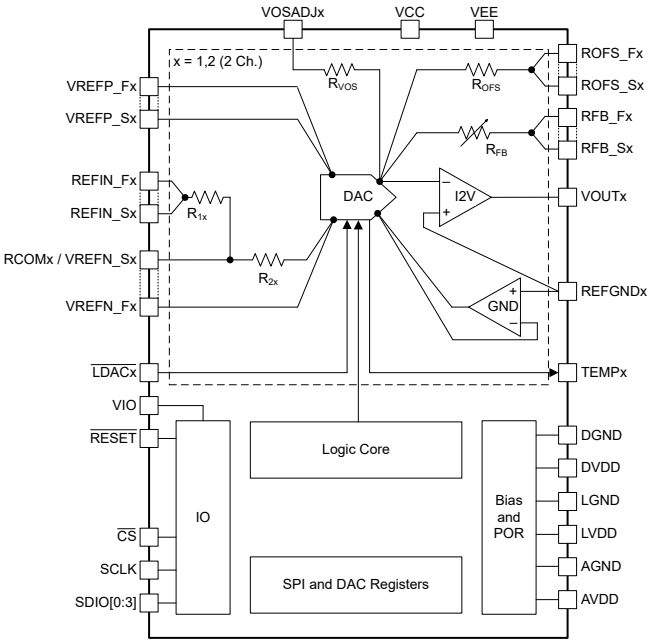
DAC90802, Dual 18-Bit, Voltage Output Multiplying DAC

1 Features

- INL: 1.9ppm (±0.5LSB at 18 bits)
- DNL: 1.9ppm (±0.5LSB at 18 bits)
- V_{REF} range: ±21V
- Integrated ±21V output buffer with high slew rate
- Digitally controlled gain options: 1 ×, 2 ×, and 4 ×
- 50ns settling to 0.1%FSR with 140pVs glitch
- Reference multiplying bandwidth: 25MHz, MFE −90dB at 100kHz
- THD at ±5V output: −125dB (2kHz) and −110dB (100kHz)
- QSPI™-compatible interface: 33MUPS in 16-bit high-speed mode at 66MHz DDR
- Double-buffered registers with per-channel $\overline{\text{LDAC}}$ pins
- Internal power on reset
- Separate 4Q multiplying, Kelvin-connected reference inputs
- Integrated ground buffer

2 Applications

- Automatic test and calibration equipment
- Quantum computing control electronics
- High data rate digital audio
- High fidelity signal generation
- Electrostatic, electromagnetic lenses
- High update rate closed loops



Simplified Block Diagram

3 Description

The DAC90802 is a dual-channel 18-bit, multiplying digital-to-analog converter (MDAC) capable of ±23.5V supply span operation. This device supports a dynamic signal range of ±21V for the reference inputs, and voltage feedback at the RFB pin, where gain options of 1 ×, 2 ×, and 4 × are digitally selectable. The output pins, VOUT support the full output range from VREFP to VREFN.

The DAC90802 provides a low-noise voltage output, and true Kelvin-connection accesses to the integrated configuration resistors of the MDAC. This device maintains very-low thermal variation and excellent long-term drift performance in the core R-2R ladder. The DAC90802 implements selectable optimizations for use in arbitrary waveform generation (AWG) mode, fast-settling mode, or multiplying mode.

A 66MHz serial data interface with up to four serial data lines (SDIO0 through SDIO3) in dual data rate (DDR) mode, supports update rates up to 33MUPS in high-speed 16-bit mode, and 22MUPS in high resolution 18-bit mode. The per-channel edge-sensitive load-DAC $\overline{\text{LDAC}}$ inputs allow fine skew control of the DAC. The DAC90802 supports device reset using the $\overline{\text{RESET}}$ pin.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DAC90802	HTQFP (48)	7mm × 7mm

(1) See *Mechanical, Packaging, and Orderable Information*
(2) The package size (length × width) is a nominal value and includes pins, where applicable

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4 Pin Configuration and Functions

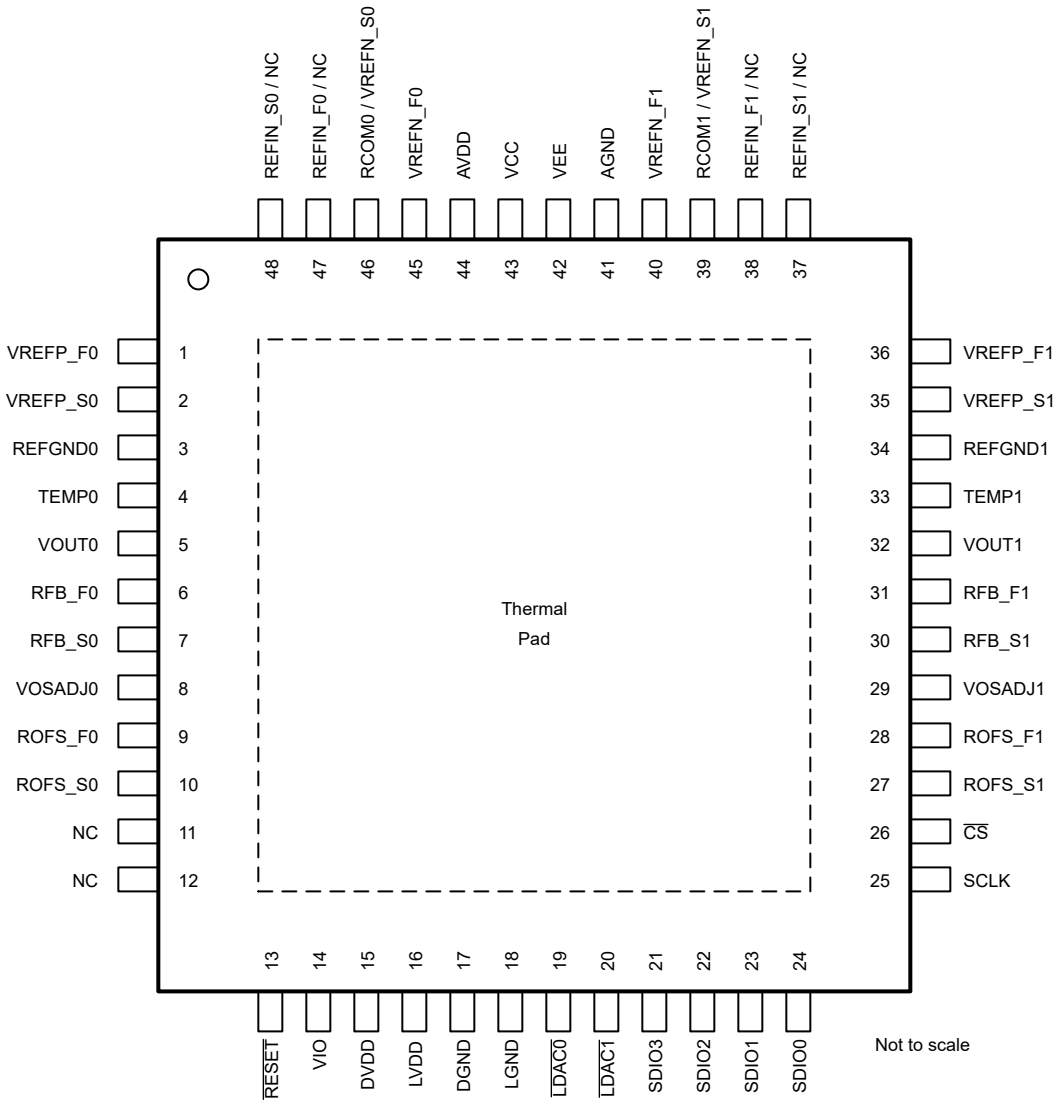

Figure 4-1. DAC90802PHP Package, 48-Pin HTQFP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	41	Ground	Analog ground.
AVDD	44	Power	Analog low voltage supply.
$\overline{CS}$	26	Input	Chip-select, active-low input.
DGND	17	Ground	Digital ground.
DVDD	15	Power	Digital low voltage supply.
$\overline{LDAC0}$	19	Input	Load-DAC0 edge-sensitive active-low input.[6]
$\overline{LDAC1}$	20	Input	Load-DAC1 edge-sensitive active-low input.[6]
LGND	18	Ground	Low Noise DAC clock ground.
LVDD	16	Power	Low Noise DAC clock supply.
NC	11, 12	–	No Connect.[5]
RCOM0 / VREFN_S0	46	Input/Output	DAC0 reference inversion driver precision resistor pair common input / VREFN sense.[1]
RCOM1 / VREFN_S1	39	Input/Output	DAC1 reference inversion driver precision resistor pair common input / VREFN sense.[1]
REFGND0	3	Input	Ground reference input for the DAC0 R-2R network.[1]
REFGND1	34	Input	Ground reference input for the DAC1 R-2R network.[1]
REFIN_F0	47	Input	DAC0 reference inversion driver precision resistor pair force input.[4]
REFIN_F1	38	Input	DAC1 reference inversion driver precision resistor pair force input.[4]
REFIN_S0	48	Output	DAC0 reference inversion driver precision resistor pair sense output.[1]
REFIN_S1	37	Output	DAC1 reference inversion driver precision resistor pair sense output.[1]
$\overline{RESET}$	13	Input	Active-low reset input.
RFB_F0	6	Input	DAC0 precision feedback resistor RFB force input.[3]
RFB_F1	31	Input	DAC1 precision feedback resistor RFB force input.[3]
RFB_S0	7	Output	DAC0 precision feedback resistor RFB sense output.[1]
RFB_S1	30	Output	DAC1 precision feedback resistor RFB sense output.[1]
ROFS_F0	9	Input	DAC0 precision offset resistor force input.[2]
ROFS_F1	28	Input	DAC1 precision offset resistor force input.[2]
ROFS_S0	10	Output	DAC0 precision offset resistor sense input.[1]
ROFS_S1	27	Output	DAC1 precision offset resistor sense input.[1]
SCLK	25	Input	SPI clock input.
SDIO0	24	Input	Quad SPI Input pin.
SDIO1	23	Input	Quad SPI Input pin.
SDIO2	22	Input/Output	Quad SPI IO pin.
SDIO3	21	Input/Output	Quad SPI IO pin.
TEMP0	4	Output	DAC0 internal temperature sensor output.
TEMP1	33	Output	DAC1 internal temperature sensor output.
VCC	43	Power	High voltage positive analog supply.
VEE	42	Power	High voltage negative analog supply.
VIO	14	Power	IO voltage power supply.
VOSADJ0	8	Input	DAC0 analog fine offset-tuning input.[2]
VOSADJ1	29	Input	DAC1 analog fine offset-tuning input.[2]
VOUT0	5	Output	DAC0 voltage output pin.
VOUT1	32	Output	DAC1 voltage output pin.
VREFN_F0	45	Input	Negative DAC0 reference force input.[2]
VREFN_F1	40	Input	Negative DAC1 reference force input.[2]
VREFP_F0	1	Input	DAC0 positive reference force input.[2]
VREFP_F1	36	Input	DAC1 positive reference force input.[2]
VREFP_S0	2	Output	DAC0 positive reference sense output.[1]
VREFP_S1	35	Output	DAC1 positive reference sense output.[1]

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Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
Thermal Pad	Thermal Pad	—	The thermal pad connects to internal PCB VEE plane through multiple vias for good thermal performance. Do not use the thermal pad as means to power the device.

(1) Connect to corresponding force _Fx pin if not used, do not leave unconnected
(2) Connect to AGND if not used, do not leave unconnected
(3) Connect to respective channel VOUT pin when unused, do not leave unconnected
(4) Connect to respective channel RCOM pin when unused, do not leave unconnected
(5) Connect to either VIO or DGND to prevent floating conditions
(6) Connect to LGND pin when unused

Note

DAC90802 implements identical independent DACs and a shared SPI. Pin names using a numerical suffix (except SDIOx) belong to the respective DAC, with identical functions for each DAC. Kelvin-connected pins use suffixes _Fx, and _Sx respectively for force, and sense lines. Pins (except SDIOx) are collectively referenced here by the primary names without suffixes.

Note

Connect the unused pins in accordance with the use case. For example, if a two-wire Kelvin connection is not required, connect the respective _Fx, _Sx pins of the same signal together to maintain the specified performance of the DAC90802.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
	Positive supply voltage	AVDD to AGND	–0.3	6	V
		VCC to VEE	–0.3	48	
		VCC to AGND	–0.3	24	
	Negative supply voltage	VEE to AGND	–24	0.3	V
	Digital supply voltage	LVDD, DVDD to DGND	–0.3	1.65	V
	IO supply voltage	VIO to DGND	–0.3	1.98	V
	Positive reference voltage	VREFPto AGND	V_{EE}	V_{CC}	V
	Negative reference voltage	VREFNto AGND	V_{EE}	V_{CC}	V
	Digital input(s) to DGND		–0.3	V_{IO} + 0.3	V
	VREFN, VREFP, ROFS, REFIN, RCOM, VOSADJ, RFB, VOUT pin voltages	Relative to AGND	V_{EE}	V_{CC}	V
		Relative to VEE	0	48	V
	Digital output, SDIOx to DGND		–0.3	V_{IO} + 0.3	V
	Current into any digital pin		–10	10	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

Over operating free-air temperature range T_A(unless otherwise noted).

		MIN	NOM	MAX	UNIT
	AVDD to AGND	4.5	5	5.5	V
	VEE to AGND	–23.5		–6.5	V
	VCC to AGND	6.5		23.5	V
	VCC to VEE	13		47	V
	DVDD to DGND	1.35	1.5	1.65	V
	LVDD to LGND (functional range)	1.35	1.5	1.65	V
	LVDD to LGND (high dc accuracy)	1.45	1.5	1.55	V
	VIO to DGND	1.15		1.9	V
	AGND to DGND	–0.3		0.3	V
	V_{IH} digital input high voltage	0.7 × V_{IO}			V
	V_{IL} digital input low voltage			0.3 × V_{IO}	V
	Analog Pins to AGND (VREFN, VREFP, ROFS, REFIN, RCOM, VOSADJ, RFB, VOUT)	–21		21	V
T_J	Junction temperature	–35		140	°C
T_A	Operating ambient temperature, $R_{\theta JA}$ = 15°C/W	–40		100	°C

5.4 Thermal Information

THERMAL METRIC[1]		DAC90802 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE (DAC_CONFIG_CHx = 01h)						
N	Resolution		18			Bits
INL	Relative accuracy	Bipolar, V_{REFP} = 5V and V_{REFN} = –5V, gain = 1 ×	–1.9		1.9	ppm
		Bipolar, V_{REFP} = 5V and V_{REFN} = –5V, gain = 2 ×	–3.8		3.8	
		Bipolar, V_{REFP} = 5V and V_{REFN} = –5V, gain = 4 ×	–9.5		9.5	
		Bipolar, V_{REFP} = 20V and V_{REFN} = –20V, gain = 1 ×	–9.5		9.5	
		Unipolar, V_{REFP} = 0V and V_{REFN} = –5V, gain = 1 ×	–3.8		3.8	
		Unipolar, V_{REFP} = 0V and V_{REFN} = –5V, gain = 4 ×	–11.4		11.4	
		Unipolar, V_{REFP} = 0V and V_{REFN} = –20V, gain = 1 ×	–11.4		11.4	
		Unipolar, V_{REFP} = 0V and V_{REFN} = –5V, gain = 2 ×	–3.8		3.8	
	Relative accuracy drift over time	T_A = 25°C, 1000 hours		±0.07		ppm
		T_A = 50°C, 1000 hours		±0.07		
DNL	Differential nonlinearity	Bipolar, V_{REFP} = 5V and V_{REFN} = –5V, gain = 1 ×, 2 ×, 4 ×	–1.9		1.9	ppm
		Unipolar, V_{REFP} = 0V and V_{REFN} = –5V, gain = 1 ×, 2 ×, 4 ×	–2.3		2.3	
		Bipolar, V_{REFP} = 20V and V_{REFN} = –20V, gain = 1 ×	–3.8		3.8	
		Unipolar, V_{REFP} = 0V and V_{REFN} = –20V, gain = 1 ×	–3.8		3.8	
G_{OV}	Gain over-range	For system calibration		2		%
GE_{TC}	Gain-error temperature coefficient			–1.5		ppm FSR/°C
	Zero-code error	Unipolar, V_{REFP} = 0V, V_{REFN} = –5V, gain = 1 ×	–84		84	ppm
		Unipolar, V_{REFP} = 0V, V_{REFN} = –5V, gain = 2 ×	–70		70	
		Unipolar, V_{REFP} = 0V, V_{REFN} = –5V, gain = 4 ×	–65		65	
		Unipolar, V_{REFP} = 0V, V_{REFN} = –20V, gain = 1 ×	–38		38	
	Midcode error	Bipolar, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×, 2 ×, 4 ×	–75		75	ppm
		Bipolar, V_{REFP} = 10V, V_{REFN} = –10V, gain = 1 ×, 2 ×	–75		75	
		Bipolar, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×	–75		75	
	Gain error	Bipolar, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×	–210		210	ppm
		Bipolar, V_{REFP} = 10V, V_{REFN} = –10V, gain = 1 ×	–210		210	
		Bipolar, V_{REFP} = 7.6V, V_{REFN} = –7.6V, gain = 2 ×	–400		400	
		Bipolar, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×	–350		350	
		Bipolar, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×	–450		450	
		Unipolar, V_{REFP} = 0V, V_{REFN} = –5V, gain = 1 ×	–250		250	
		Unipolar, V_{REFP} = 0V, V_{REFN} = –10V, gain = 1 ×	–250		250	
		Unipolar, V_{REFP} = 0V, V_{REFN} = –7.6V, gain = 2 ×	–400		400	
		Unipolar, V_{REFP} = 0V, V_{REFN} = –20V, gain = 1 ×	–350		350	
		Unipolar, V_{REFP} = 0V, V_{REFN} = –5V, gain = 4 ×	–450		450	
	Zero-code-error temperature drift	Unipolar, V_{REFP} = 0V, V_{REFN} = –5V, gain = 1 ×		2		µV/C
		Unipolar, V_{REFP} = 0V, V_{REFN} = –5V, gain = 2 ×		3.5		
		Unipolar, V_{REFP} = 0V, V_{REFN} = –5V, gain = 4 ×		6.5		
		Unipolar,V_{REFP} = 0V, V_{REFN} = –20V, gain = 1 ×		3.5		

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Midcode-error temperature drift	Bipolar, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		3		µV/C
		Bipolar, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×		10		
		Bipolar, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×		8.5		
		Bipolar, V_{REFP} = 5V, V_{REFN} = –5V, gain = 2 ×		5.5		
LTD	Output-voltage-drift over time	T_A = 25°C, V_{OUT} = midscale, 1000 hours		1		ppm
		T_A = 50°C, V_{OUT} = midscale, 1000 hours		1		

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTEGRATED RESISTORS						
R_1	Reference-inversion resistor			4		kΩ
R_2	Reference-inversion resistor			4		kΩ
R_1/R_2	Inversion-resistor-ratio mismatch			200		ppm
$\Delta R_1/R_2$	Inversion-resistor-ratio-mismatch drift			0.6		ppm/C
R_{OFS}	Coarse-offset resistor			8		kΩ
R_{OSADJ}	Fine-offset-adjust resistor			512		kΩ
R_{FB}	Feedback resistor	Gain = 1 ×		4		kΩ
		Gain = 2 ×		8		kΩ
		Gain = 4 ×		16		kΩ

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
	Headroom[(1)]	From VOUT to VCC pins	3			V
		From VOUT to VEE pins			–3	
V_{OUT}	Output-voltage span	Range for VOUT and RFB	–20.5		20.5	V
PSRR	Power-supply-rejection ratio (dc)	V_{CC} = 22V ±1.5V V_{EE} = –23.5V		–105		dB
		V_{CC} = 23.5V , V_{EE} = –22 V ±1.5V		–105		dB
		AVDD= 5V ± 0.5V		–105		dB
		LVDD= 1.5V ± 0.15V		–85		dB
C_L	Output capacitive load[(1)]	AWG mode (DAC_CONFIG_CHx = 00h)			25	pF
		Fast-settling mode (DAC_CONFIG_CHx = 01h), Multiplying mode (DAC_CONFIG_CHx = 02h)			35	
I_{SCVOUT}	Output short-circuit current	VOUT pin		80	135	mA

5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE INPUTS						
I_{REFP}	Reference-input current	VREFP pin (excludes R1, R2 connections)	9.5			mA
I_{REFN}		VREFN pin (excludes R1, R2 connections)			–9.5	
C_{VREF}	Input-capacitance to AGND			10		pF
V_{REF}	DC reference-voltage functional range[(2)]	VREFN and VREFP pins	–21		21	V
V_{REFIN}	REFIN-pin voltage range[(2)]	V_{REFIN} relative to AGND	–21		21	V
V_{OFFSET}	VOSADJ and ROFS pin DC Offset voltage range[(2)]	V_{OSADJ} and V_{ROFS} relative to AGND	–21		21	V

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE - AWG MODE (DAC_CONFIG_CHx = 00h)						
THD	Total harmonic distortion	f_{OUT} = 2kHz full-scale sine wave, f_s = 5MHz, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		–125		dB
		f_{OUT} = 20kHz full-scale sine wave, f_s = 5MHz, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		–120		
		f_{OUT} = 100kHz full-scale sine wave, f_s = 5MHz, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		–110		
SNR	Signal-to-noise ratio	0.1Hz to 20kHz, f_{OUT} = 2kHz full-scale sine wave, f_s = 5MHz, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		122		dB
		0.1Hz to 250kHz, f_{OUT} = 20kHz full-scale sine wave, f_s = 5MHz, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		112		
		0.1Hz to 500kHz, f_{OUT} = 100kHz full-scale sine wave, f_s = 5MHz, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		110		
t_s	Output-voltage settling time	100mV output settling to ±0.0004%, V_{REFP} = 7.6V, V_{REFN} = –7.6V, gain = 1 ×		455		ns
		100mV output settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		500		
		100mV output settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 2 ×		450		
		100mV output settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×		528		
		100mV output settling to ±0.0004%, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×		420		
SR	Slew rate	Full-scale step, measured at VOUT pin, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		70		V/µs
		Full-scale step, measured at VOUT pin, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×		160		
		Full-scale step, measured at VOUT pin, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×		192		

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE - FAST SETTLING MODE (DAC_CONFIG_CHx = 01h)						
	Overshoot	0mV to 100mV output step		2		%
		0V to 10V output step		2		
t_s	Output-voltage settling time	100mV output settling to 0.1%FSR, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		52		ns
		Full-scale output settling to 0.1%FSR, V_{REFP} = 5V, V_{REFN} = –5 V, gain = 1 ×		226		
		200mV output settling to 0.1%FSR, V_{REFP} = 5V, V_{REFN} = –5V, gain = 2 ×		66		
		Full-scale output settling to 0.1%FSR, V_{REFP} = 5V, V_{REFN} = –5V, gain = 2 ×		288		
		400mV output settling to 0.1%FSR, V_{REFP} = 5V, V_{REFN} = –5V, Gain = 4 ×		96		
		Full-scale output settling to 0.1%FSR, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×		450		
		100mV output settling to 0.1%FSR, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×		49		
		Full-scale output settling to 0.1%FSR, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×		290		
t_s	Output-voltage settling time	100mV settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		178		ns
		Full-scale settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		385		
		100mV settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 2 ×		167		
		Full-scale settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 2 ×		1500		
		100mV settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×		237		
		Full-scale settling to ±0.0004%, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×		1903		
		100mV settling to ±0.0004%, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×		154		
		Full-scale settling to ±0.0004%, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×		920		
	Power-on glitch magnitude	Measured at DAC voltage output on channel power up		1		V
	Channel power-on time[1]	Measured at DAC voltage output on channel power up			400	µs
	Code-change glitch impulse, absolute integral[3]	Midscale LSB transition at –5V to +5V range, gain = 1 ×, integrated over $\overline{LDAC}$ edge to settling time (t_s)		140		pV-s
	Code-change glitch impulse, direct integral[4]	Midscale LSB transition at –5V to +5V range, gain = 1 ×, integrated over $\overline{LDAC}$ edge to settling time (t_s)		32		
	Code-change glitch impulse voltage	Midscale LSB transition at –5V to +5V range, gain = 1 ×		9		mV

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	Full-scale step, measured at VOUT pin, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		145		V/µs
		Full-scale step, measured at VOUT pin, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×		188		
		Full-scale step, measured at VOUT pin, V_{REFP} = 20V, V_{REFN} = –20V. gain = 1 ×		217		
	Digital feedthrough (absolute Integral)	Gain = 1 ×, SCLK = 1MHz, all other digital lines are static		15		pV-s

5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE - MULTIPLYING MODE (DAC_CONFIG_CHx = 02h)						
V_{REF}	AC reference voltage range	Input on VREFN, V_{REFP} = REFGND	–21		21	V
MBW	Reference-multiplying bandwidth	V_{REFP} = 0V and V_{REFIN} = ±100mV, gain = 1 ×, full scale		25		MHz
		V_{REFP} = 0V and V_{REFIN} = ±5V, gain = 1 ×, full scale		9		
		V_{REFP} = 0V and V_{REFIN} = ±5V, gain = 4 ×, full scale		2.5		
		V_{REFP} = 0V and V_{REFIN} = ±20V, gain = 1 ×, full scale		3		
MFE	Multiplying feedthrough error	Gain = 4 ×, zero scale, 100kHz, V_{REFP} = 0V, V_{REFIN} = ±5V		–80		dB
		Gain = 1 ×, zero scale, 100kHz, V_{REFP} = 0V, V_{REFIN} = 100mV_{RMS}		–90		
		Gain = 1 ×, zero scale, 100kHz, V_{REFP} = 0V, V_{REFIN} = ±20V		–90		
THD_M	Multiplying THD	f_{IN} = 2 kHz at V_{REFP} = 0, V_{REFIN} = ±5 V, gain = 1 ×		–124		dB
		f_{IN} = 20 kHz at V_{REFP} = 0, V_{REFIN} = ±5 V, gain = 1 ×		–120		
		f_{IN} = 100kHz at V_{REFP} = 0V, V_{REFIN} = ±5V, gain = 1 ×		–108		
SR	Slew rate	Full-scale step, measured at VOUT pin, V_{REFP} = 5V, V_{REFN} = –5V, gain = 1 ×		122		V/µs
		Full-scale step, measured at VOUT pin, V_{REFP} = 5V, V_{REFN} = –5V, gain = 4 ×		112		
		Full-scale step, measured at VOUT pin, V_{REFP} = 20V, V_{REFN} = –20V, gain = 1 ×		194		

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NOISE PERFORMANCE (DAC_CONFIG_CHx = 01h)						
V_n	Output noise	0.1Hz to 10Hz, gain = 1 ×		6		μV_{PP}
		0.1Hz to 10Hz, gain = 4 ×		16		
1/f	Noise corner frequency	Gain = 1 ×		680		Hz
		Gain = 4 ×		580		
	Output noise density	Measured at 10kHz, gain = 1 × (excluding R_1, R_2)		17		nV/√Hz
		Measured at 10kHz, gain = 4 × (excluding R_1, R_2)		52		
	Power-supply-rejection ratio (ac)	200mV_{PP}, 50Hz or 60Hz sine wave superimposed on V_{CC}, V_{CC} = 23.4V, V_{EE} = –23.5V, AVDD= 5V, LVDD = 1.5V		–100		dB
		200mV_{PP}, 50Hz or 60Hz sine wave superimposed on V_{EE}, V_{CC} = 23.5V, V_{EE} = –23.4V, AVDD= 5V, LVDD = 1.5V		–100		
		200mV_{PP}, 50Hz or 60Hz sine wave superimposed on AVDD, V_{CC} = 23.5V, V_{EE} = –23.5V, AVDD= 5V, LVDD = 1.5V		–96		
		50mV_{PP}, 50Hz or 60Hz sine wave superimposed on LVDD, V_{CC} = 23.5V, V_{EE} = –23.5V, AVDD= 5V, LVDD = 1.5V, gain = 1 ×		–90		
		50mV_{PP}, 50Hz or 60Hz sine wave superimposed on LVDD, V_{CC} = 23.5V, V_{EE} = –23.5V, AVDD= 5V, LVDD = 1.5V, gain = 4 ×		–80		

5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR ANALOG OUTPUT MODE						
	Temperature sensing range	TEMP analog output mode	–40		150	℃
V_{TEMP25}	Output voltage	T_J = 25℃		1.8		V
G_{TEMP}	Sensor gain			20		mV/℃
V_{TEMP}	Output voltage span		0.5		4.3	V
	Absolute accuracy			±5		℃
ZOA_{TEMP}	TEMP signal output impedance			0.85		kΩ
TEMPERATURE SENSOR DIGITAL OUTPUT MODE						
T_{OSD}	Over temperature shutdown threshold range	Measured at the junction	29.6		150	℃
VOL_{TEMP}	Low-level output voltage	Into high-impedance digital buffer			0.4	V
VOH_{TEMP}	High-level output voltage	Into high-impedance digital buffer	(V_{IO} – 0.4)			V
ZOD_{TEMP}	TEMP signal output impedance			5		kΩ

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
V_{IL}	Low-level input voltage				0.3	V/V_{IO}
V_{IH}	High-level input voltage		0.7			V/V_{IO}
V_{HYS}	Hysteresis voltage	V_{IO} = 1.8V		0.12		V
	Input current			±1		µA
	Pin capacitance	Per pin		2		pF
DIGITAL OUTPUTS						
V_{OL}	Low-level output voltage	Sinking 200µA			0.4	V
V_{OH}	High-level output voltage	Sourcing 200µA	(V_{IO}– 0.4)			V
I_{OZ}	High-impedance leakage			±1		µA
C_{OZ}	High-impedance output capacitance			2		pF
SPI						
f_{SPI}	SPI Frequency				66	MHz
	DAC update rate	DDR enabled,16-bit mode, 66MHz SCLK, SDIO0 through SDIO3 as inputs, single channel stream mode		33		MUPS
		DDR enabled, 18-bit mode, 66MHz SCLK, SDIO0 through SDIO3 as inputs, single channel stream mode,		22		
		DDR disabled, 16-bit mode, 66MHz SCLK, SDIO0 through SDIO3 as inputs, single channel stream mode		16.5		
		DDR disabled, 18-bit mode, 66MHz SCLK, SDIO0 through SDIO3 as inputs, single channel stream mode		11		
		Daisy chain mode (DDR disabled), 66MHz SCLK, SDIO0 and SDIO1 as SDI, SDIO2 and SDIO3 as SDO, single secondary SPI		3.3		

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5.5 Electrical Characteristics (continued)

At T_A = –40°C to +100°C, V_{CC} = +8.5V to +23.5V, V_{EE}= –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND, see note for V_{REFPX} and V_{REFNX}, all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
I_{VCC_S}	Standby-mode rail current	V_{CC} = 23.5V, V_{EE} = –23.5V, AVDD = 5.4V, DVDD= 1.65V, LVDD= 1.65V		0.16		mA
I_{VEE_S}	Standby-mode rail current	V_{CC} = 23.5V, V_{EE} = –23.5V, AVDD = 5.4V, DVDD= 1.65V, LVDD= 1.65V		–0.16		mA
I_{AVDD_S}	Standby-mode rail current	V_{CC} = 23.5V, V_{EE} = –23.5V, AVDD = 5.4V, DVDD= 1.65V, LVDD= 1.65V		34		uA
I_{LVDD_S}	Standby-mode rail current	V_{CC} = 23.5V, V_{EE} = –23.5V, AVDD = 5.4V, DVDD= 1.65V, LVDD= 1.65V		10		uA
I_{DVDD_S}	Standby-mode rail current	V_{CC} = 23.5V, V_{EE} = –23.5V, AVDD = 5.4V, DVDD= 1.65V, LVDD= 1.65V		15		uA
I_{AVDD}	Current flowing into AVDD	VREFP = 20V, VREFN = –20V, full scale			2.5	mA
I_{VCC}	Current flowing into VCC	VREFP = 20V, VREFN = –20V,full scale			30	mA
I_{VEE}	Current flowing into VEE	VREFP = 20V, VREFN = –20V, zero scale	–30			mA
I_{DVDD}	Current flowing into DVDD	VREFP = 20V, VREFN = –20V, full scale		20		uA
I_{IOVDD}	Current flowing into VIO	V_{REFP} = 20V, V_{REFN} = –20V, full scale code, all digital input pins static at V_{IO}		10		uA

(1) Guaranteed by design or characterization. Not production tested.
(2) Excludes required headroom.
(3) Absolute integral refers to integrating the absolute magnitude of the glitch waveform to arrive at the glitch energy.
(4) Direct integral refers to integrating the signed magnitude of the glitch waveform to arrive at the glitch energy.

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5.6 Timing Requirements

at AVDD = 5.0V, DVDD = 1.5V, T_A = 25°C typical values; minimum and maximum values for the range of recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
SERIAL INTERFACE WRITE AND READ OPERATIONS: 1.65V ≤ V_{IO} < 1.98V					
f_{SCLK}	Serial clock frequency, SDO_EN = 0, FSDO_EN = 1			66	MHz
t_{SCLK}	SCLK cycle time, SDO_EN = 0 or SDO_EN = 1 with FSDO_EN = 1	15.15			ns
$t_{SCLKHIGH}$	SCLK high time, SDO_EN = 0 or SDO_EN = 1 with FSDO_EN = 1	7.6			ns
$t_{SCLKLOW}$	SCLK low time, SDO_EN = 0 or SDO_EN = 1 with FSDO_EN = 1	7.6			ns
f_{SCLK}	Serial clock frequency, SDO_EN = 1 with FSDO_EN = 0			33	MHz
t_{SCLK}	SCLK cycle time, SDO_EN = 1 with FSDO_EN = 0	30.3			ns
$t_{SCLKHIGH}$	SCLK high time, SDO_EN = 1 with FSDO_EN = 0	15.2			ns
$t_{SCLKLOW}$	SCLK low time, SDO_EN = 1 with FSDO_EN = 0	15.2			ns
t_{CSS}	$\overline{CS}$ falling to first SCLK sampling edge setup time	7.5			ns
t_{CSH}	Last SCLK sampling edge to $\overline{CS}$ rising edge	7.5			ns
t_{CSHIGH}	$\overline{CS}$ high time	20			ns
t_{SDIS}	Data setup time	2.5			ns
t_{SDIH}	Data hold time	2.5			ns
t_{SDODLY}	SCLK falling edge to SDO data valid			12	ns
t_{SDODZ}	$\overline{CS}$ rising edge to SDO tri-state			6	ns
t_{SDOZD}	$\overline{CS}$ falling edge to SDO enabled			6	ns
t_{LDACL}	$\overline{LDAC}$ pulse width low state	7			ns
t_{LDACH}	$\overline{LDAC}$ pulse width high state	20			ns
f_{TOGGLE}	$\overline{LDAC}$ toggle frequency			33	MHz
t_{SCLD}	EOP (End of Packet) to $\overline{LDAC}$ falling edge [(1)]			20	ns

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5.6 Timing Requirements (continued)

at AVDD = 5.0V, DVDD = 1.5V, T_A = 25°C typical values; minimum and maximum values for the range of recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
SERIAL INTERFACE WRITE AND READ OPERATIONS: 1.35V ≤ V_{IO} < 1.65V					
f_{SCLK}	Serial clock frequency, SDO_EN = 0, FSDO_EN = 1			50	MHz
t_{SCLK}	SCLK cycle time, SDO_EN = 0 or SDO_EN = 1 with FSDO_EN = 1	20.00			ns
$t_{SCLKHIGH}$	SCLK high time, SDO_EN = 0 or SDO_EN = 1 with FSDO_EN = 1	9			ns
$t_{SCLKLOW}$	SCLK low time, SDO_EN = 0 or SDO_EN = 1 with FSDO_EN = 1	9			ns
f_{SCLK}	Serial clock frequency, SDO_EN = 1 with FSDO_EN = 0			25	MHz
t_{SCLK}	SCLK cycle time, SDO_EN = 1 with FSDO_EN = 0	40			ns
$t_{SCLKHIGH}$	SCLK high time, SDO_EN = 1 with FSDO_EN = 0	18			ns
$t_{SCLKLOW}$	SCLK low time, SDO_EN = 1 with FSDO_EN = 0	18			ns
t_{CSS}	$\overline{CS}$ falling to first SCLK sampling edge setup time	9			ns
t_{CSH}	Last SCLK sampling edge to $\overline{CS}$ rising edge	9			ns
t_{CSHIGH}	$\overline{CS}$ high time	40			ns
t_{SDIS}	Data setup time	5			ns
t_{SDIH}	Data hold time	5			ns
t_{SDODLY}	SCLK falling edge to SDO data valid	14			ns
t_{SDODZ}	$\overline{CS}$ rising edge to SDO tri-state			8	ns
t_{SDOZD}	$\overline{CS}$ falling edge to SDO enabled			8	ns
t_{LDACL}	$\overline{LDAC}$ pulse width low state	7			ns
t_{LDACH}	$\overline{LDAC}$ pulse width high state	20			ns
f_{TOGGLE}	$\overline{LDAC}$ toggle frequency			25	MHz
t_{SCLD}	EOP (End of Packet) to $\overline{LDAC}$ falling edge (1)			25	ns

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5.6 Timing Requirements (continued)

at AVDD = 5.0V, DVDD = 1.5V, T_A = 25°C typical values; minimum and maximum values for the range of recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
SERIAL INTERFACE WRITE AND READ OPERATIONS: 1.08V ≤ V_{IO} < 1.35V					
f_{SCLK}	Serial clock frequency, SDO_EN = 0, FSDO_EN = 1			35	MHz
t_{SCLK}	SCLK cycle time, SDO_EN = 0 or SDO_EN=1 with FSDO_EN = 1	28.57			ns
$t_{SCLKHIGH}$	SCLK high time, SDO_EN = 0 or SDO_EN=1 with FSDO_EN = 1	13.5			ns
$t_{SCLKLOW}$	SCLK low time, SDO_EN = 0 or SDO_EN=1 with FSDO_EN = 1	13.5			ns
f_{SCLK}	Serial clock frequency, SDO_EN = 1 with FSDO_EN = 0			17.5	MHz
t_{SCLK}	SCLK cycle time, SDO_EN = 1 with FSDO_EN = 0	57.14			ns
$t_{SCLKHIGH}$	SCLK high time, SDO_EN = 1 with FSDO_EN = 0	27			ns
$t_{SCLKLOW}$	SCLK low time, SDO_EN = 1 with FSDO_EN = 0	27			ns
t_{CSS}	$\overline{CS}$ falling to first SCLK sampling edge setup time	11			ns
t_{CSH}	Last SCLK sampling edge to $\overline{CS}$ rising edge	11			ns
t_{CSHIGH}	$\overline{CS}$ high time	60			ns
t_{SDIS}	Data setup time	7			ns
t_{SDIH}	Data hold time	7			ns
t_{SDODLY}	SCLK falling edge to SDO data valid	16			ns
t_{SDODZ}	$\overline{CS}$ rising edge to SDO tri-state			10	ns
t_{SDOZD}	$\overline{CS}$ falling edge to SDO enabled			10	ns
t_{LDACL}	$\overline{LDAC}$ pulse width low state	7			ns
t_{LDACH}	$\overline{LDAC}$ pulse width high state	20			ns
f_{TOGGLE}	$\overline{LDAC}$ toggle frequency			17.5	MHz
t_{SCLD}	EOP (End of Packet) to $\overline{LDAC}$ falling edge [(1)]			30	ns

5.6 Timing Requirements (continued)

at AVDD = 5.0V, DVDD = 1.5V, T_A = 25°C typical values; minimum and maximum values for the range of recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
COMMON LOGIC					
$t_{RESETLOW}$	$\overline{RESET}$ pulse width low	100			ns
t_{RSTACT}	$\overline{RESET}$ pulse activation time	100			ns
t_{SLDAC}	VOUT output update delay (From $\overline{CS}$ rising, Soft LDAC, SFT_LDAC_EN = 1)			80	ns
t_{ASYNC}	VOUT output update delay from EOP (End of Packet) (ASYNC_UPDT = 1) (1)			70	ns
t_{LDACR}	VOUT output update delay from $\overline{LDAC}$ falling edge (ASYNC_UPDT = 0)			40	ns
t_{SKEW}	Max channel to channel skew, $\overline{LDAC}$ shorted (FS mode) (ASYNC_UPDT = 0)		0.3		ns
t_{PWRUP}	Wait time before DAC register access (bootup time)			20	ms
t_{RESET}	Shutdown exit time (channel power-up time)			0.8	ms

(1) EOP is the last SCLK sampling edge when SPI_DCH = 0 (STREAM = Any). EOP is $\overline{CS}$ rising edge for SPI_DCH = 1.

5.7 Timing Diagrams

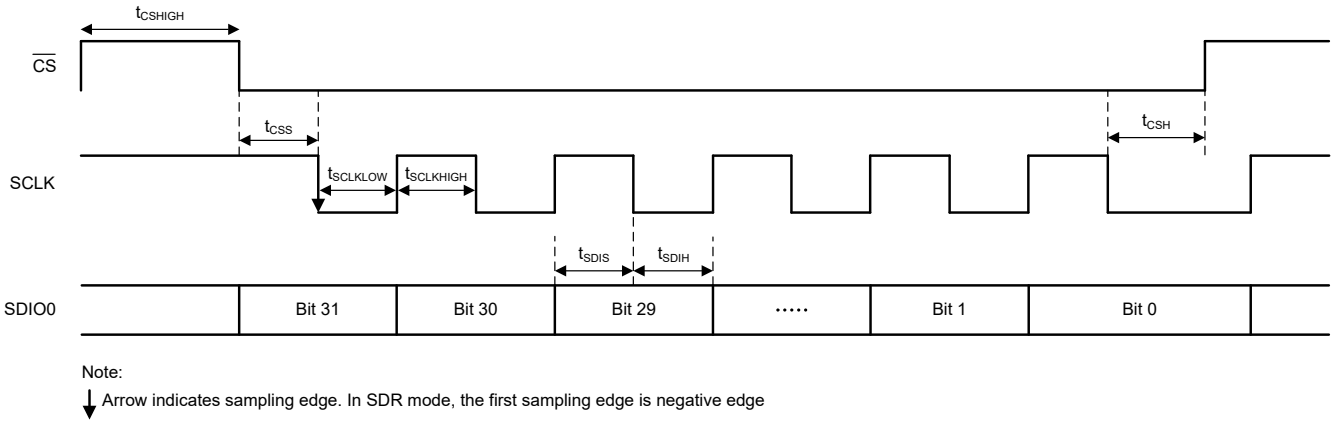

Figure 5-1. SDR Write Mode

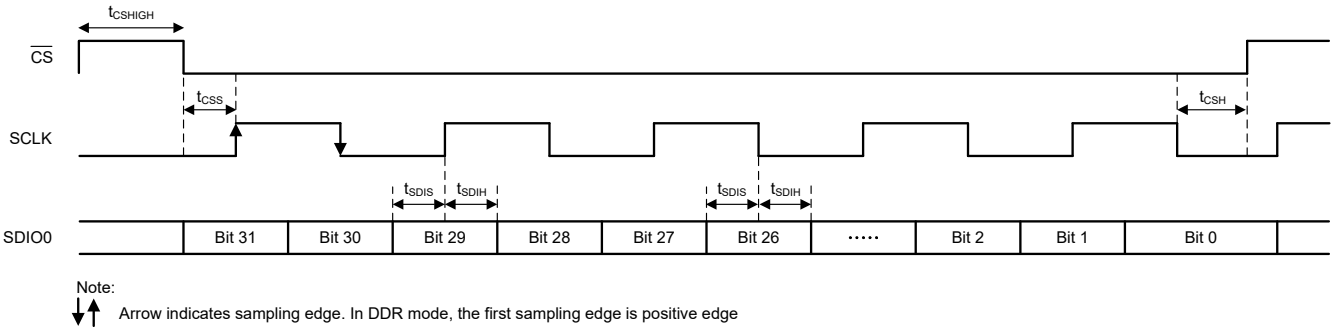

Figure 5-2. DDR Write Mode

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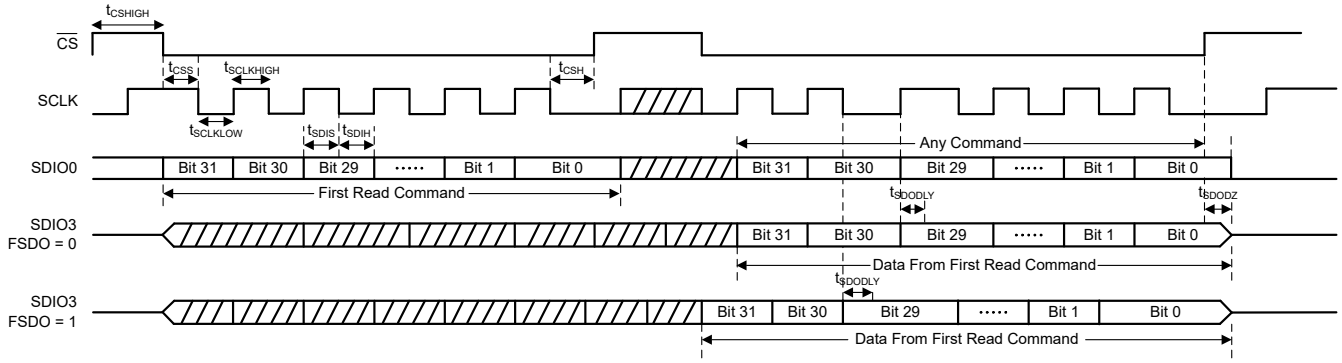


Figure 5-3. Read Frame Mode

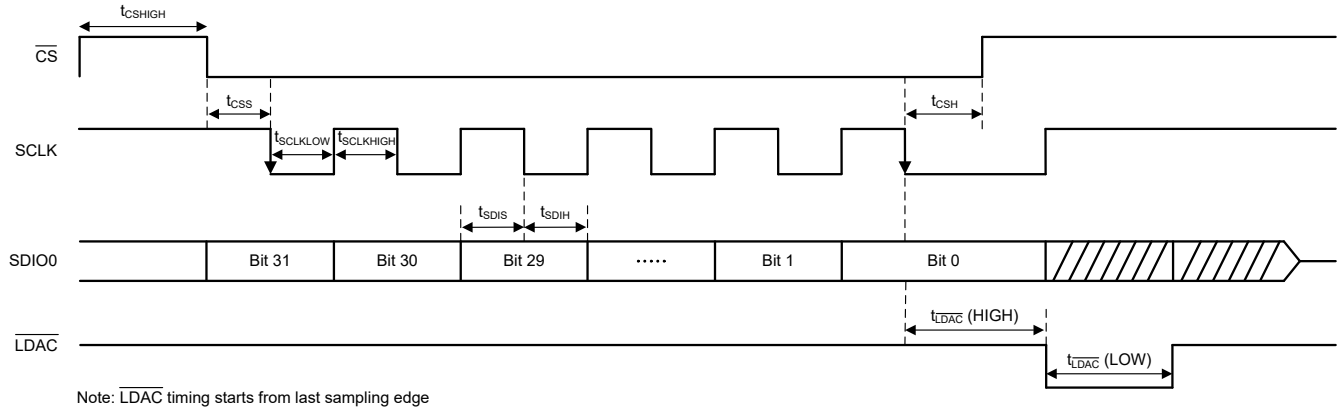


Figure 5-4. $\overline{\text{LDAC}}$ Timing Non Daisy Mode

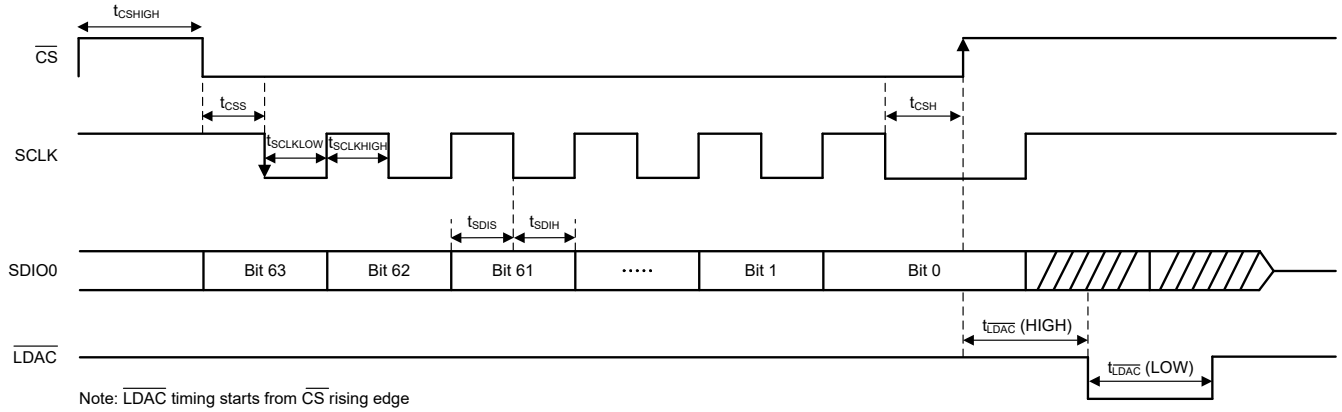


Figure 5-5. $\overline{\text{LDAC}}$ Timing Daisy Mode

5.8 Typical Characteristics

5.8.1 Typical Characteristics: Linearity

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJx = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

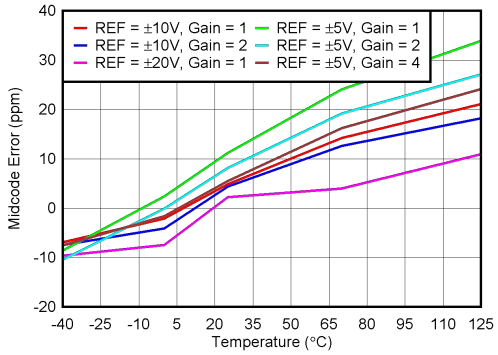


Figure 5-6. Bipolar Midcode Error vs Temperature

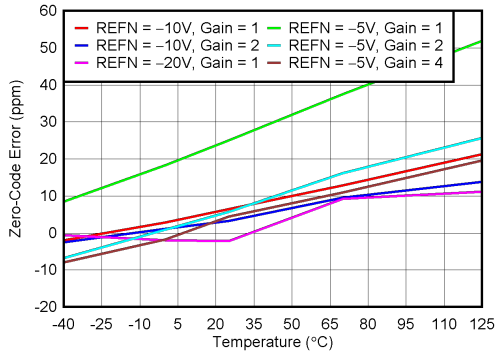
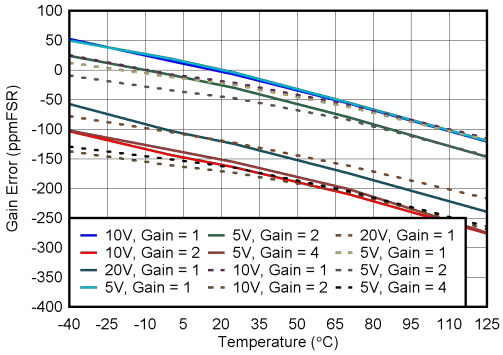
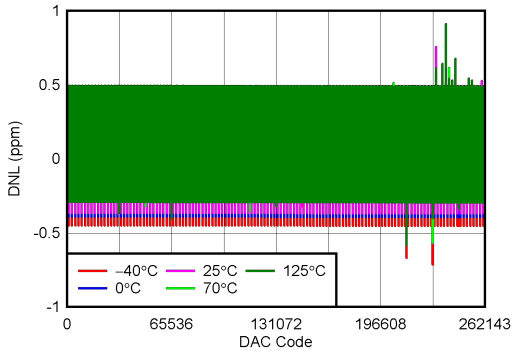


Figure 5-7. Unipolar Zero-Code Error vs Temperature



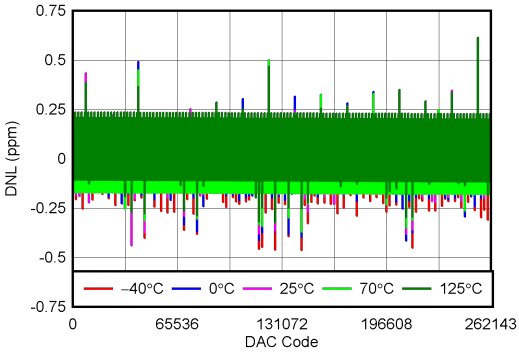
Bipolar (solid line), unipolar (dotted line)

Figure 5-8. Gain Error vs Temperature



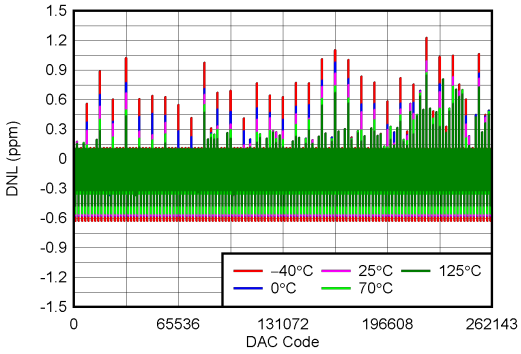
REFPx = 0V, REFNx = –5V, gain = 1, unipolar

Figure 5-9. DNL vs Digital Input Code



REFPx = +5V, REFNx = –5V, gain = 1, bipolar

Figure 5-10. DNL vs Digital Input Code



REFPx = 0V, REFNx = –20V, gain = 1, unipolar

Figure 5-11. DNL vs Digital Input Code

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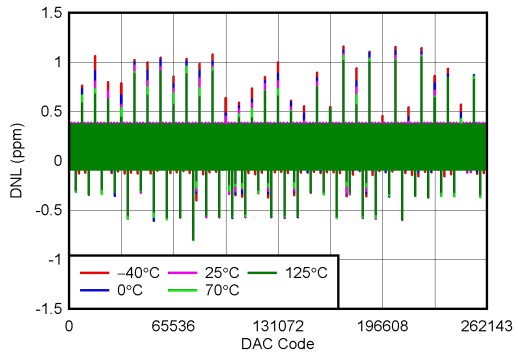
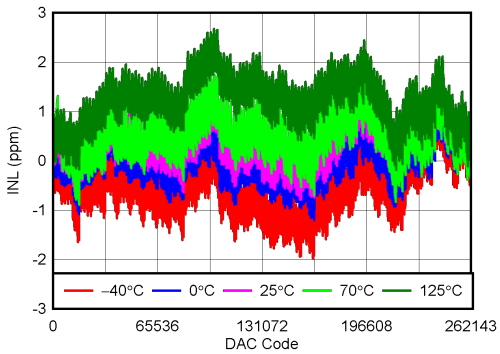
5.8.1 Typical Characteristics: Linearity (continued)

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJx = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



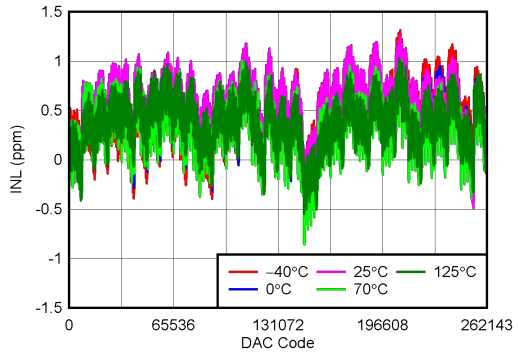
REFPx = +20V, REFNx = –20V, gain = 1, bipolar

Figure 5-12. DNL vs Digital Input Code



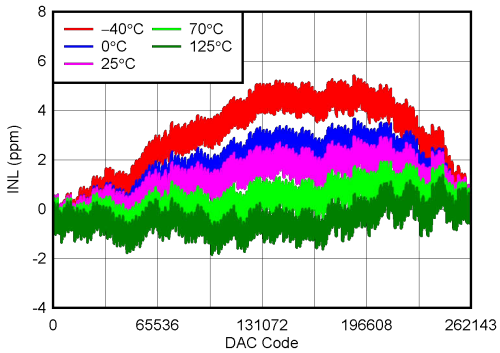
REFPx = 0V, REFNx = –5V, gain = 1, unipolar

Figure 5-13. INL vs Digital Input Code



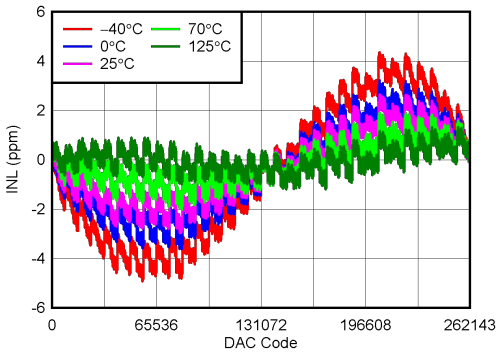
REFPx = +5V, REFNx = –5V, gain = 1, bipolar

Figure 5-14. INL vs Digital Input Code



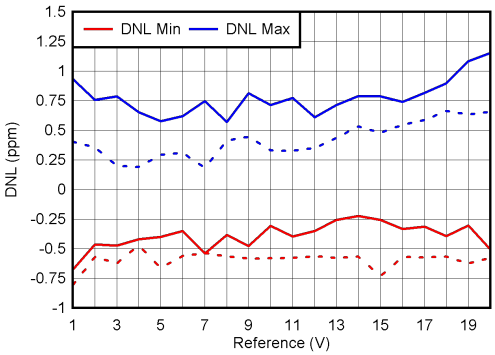
REFPx = 0V, REFNx = –20V, gain = 1, unipolar

Figure 5-15. INL vs Digital Input Code



REFPx = +20V, REFNx = –20V, gain = 1, bipolar

Figure 5-16. INL vs Digital Input Code



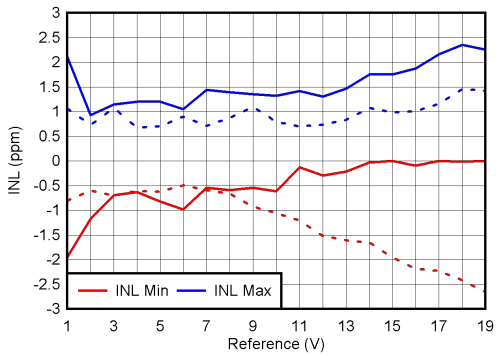
Gain = 1

Unipolar (solid line), bipolar (dotted line)

Figure 5-17. DNL vs Reference

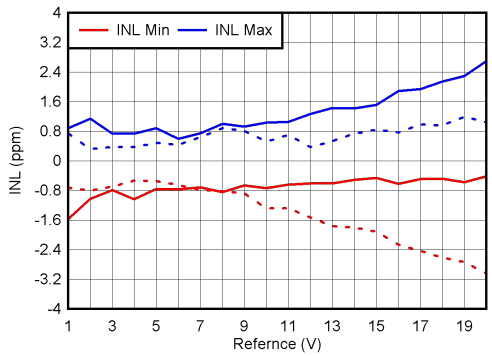
5.8.1 Typical Characteristics: Linearity (continued)

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJx = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



Unipolar (solid line), bipolar (dotted line)

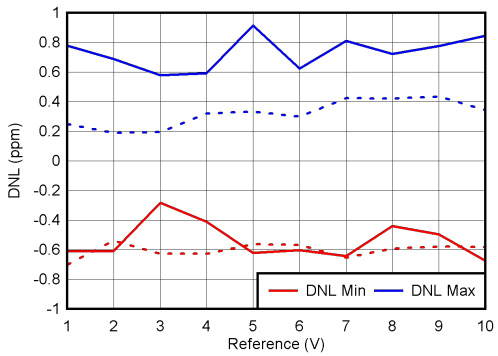
Figure 5-18. INL vs Reference



Gain = 1

Unipolar (solid line), bipolar (dotted line)

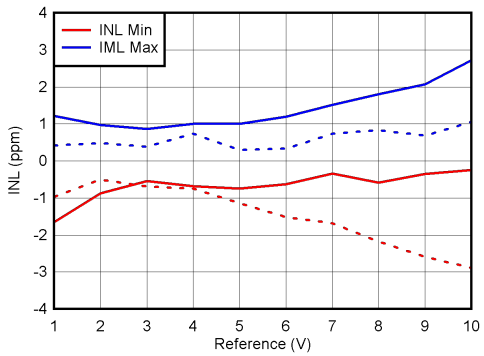
Figure 5-19. INL vs Reference



Gain = 2

Unipolar (solid line), bipolar (dotted line)

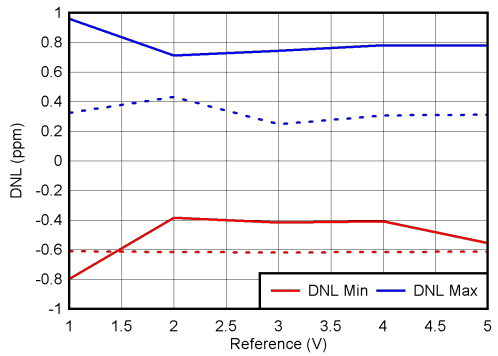
Figure 5-20. DNL vs Reference



Gain = 2

Unipolar (solid line), bipolar (dotted line)

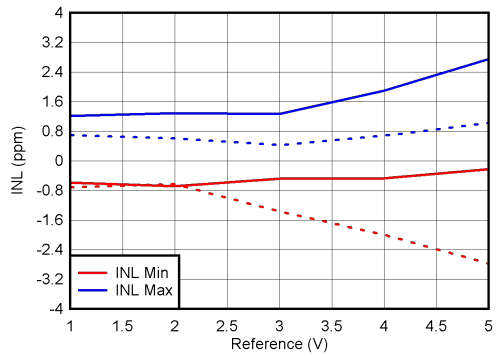
Figure 5-21. INL vs Reference



Gain = 4

Unipolar (solid line), bipolar (dotted line)

Figure 5-22. DNL vs Reference



Gain = 4

Unipolar (solid line), bipolar (dotted line)

Figure 5-23. INL vs Reference

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5.8.1 Typical Characteristics: Linearity (continued)

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJx = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)

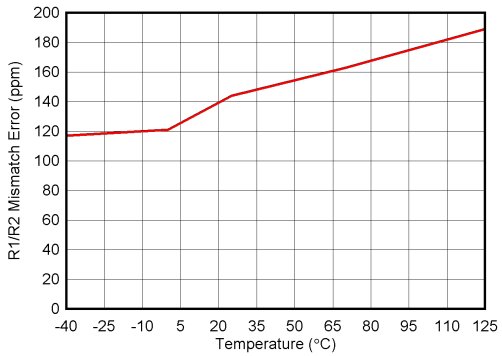
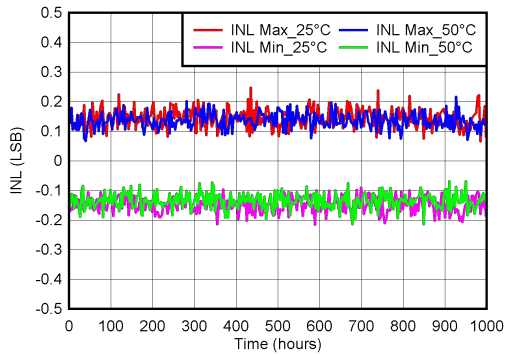
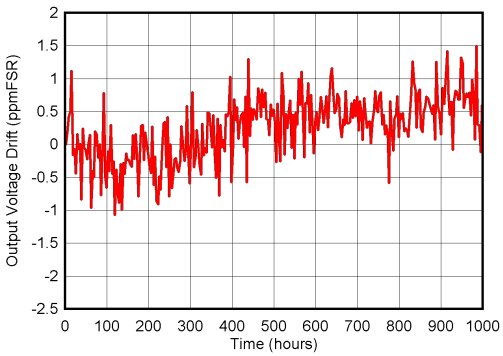


Figure 5-24. R1/R2 Mismatch Error vs Ambient Temperature



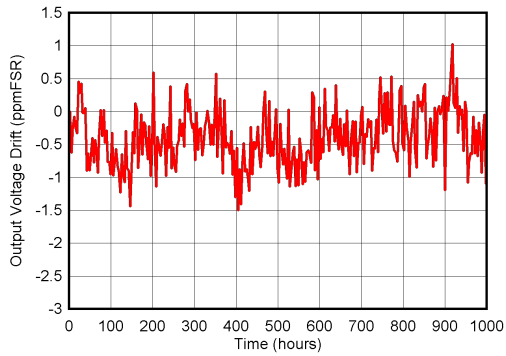
Gain = 1, fast settling mode, bipolar
REFPx and REFNx = ±5V

Figure 5-25. INL Drift Over 1000 Hours



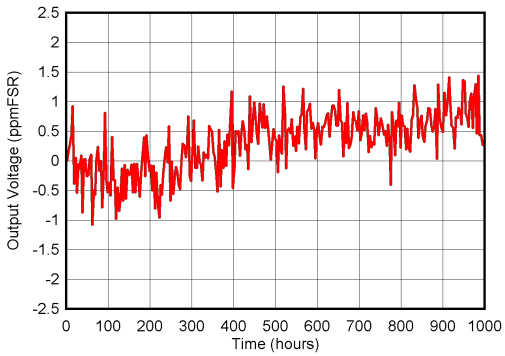
Gain = 1, fast settling mode, bipolar
REFPx and REFNx = ±5V, full code, temperature = 25°C

Figure 5-26. Output Voltage Drift



Gain = 1, fast settling mode, bipolar
REFPx and REFNx = ±5V, zero code, temperature = 25°C

Figure 5-27. Output Voltage Drift

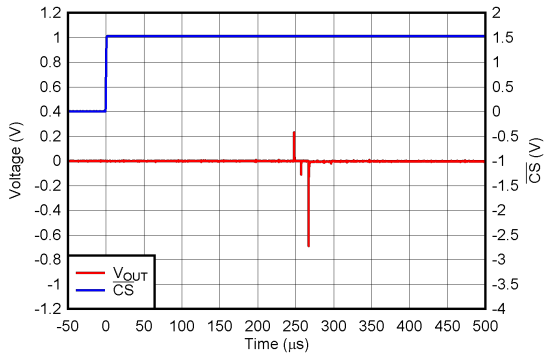


Gain = 1, fast settling mode, bipolar
REFPx and REFNx = ±5V, midcode, temperature = 25°C

Figure 5-28. Output Voltage Drift

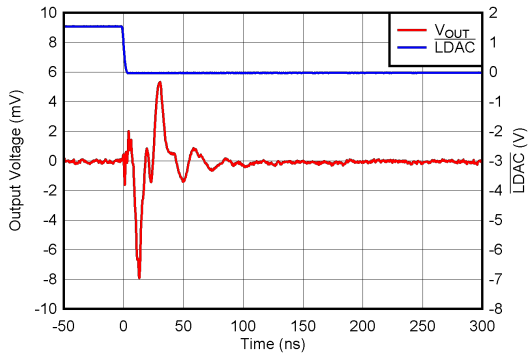
5.8.2 Typical Characteristics: Glitch

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



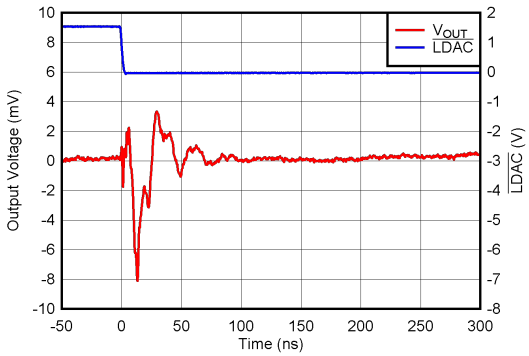
Gain = 1, fast settling mode, bipolar
REFPx = +5V, REFNx = –5V

Figure 5-29. Channel Power ON Glitch



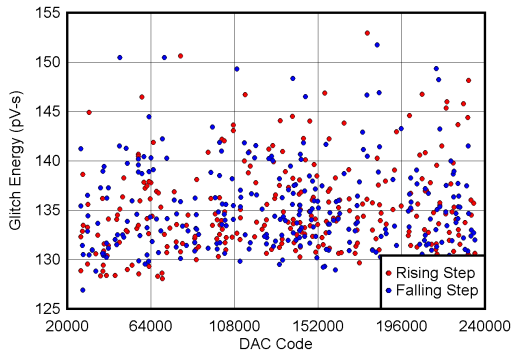
Gain = 1, fast settling mode, bipolar
REFPx = +5V, REFNx = –5V

Figure 5-30. Code Change Glitch



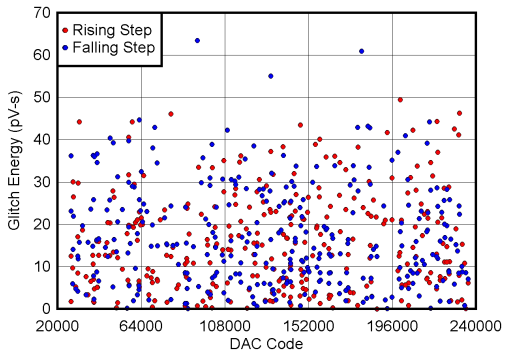
Gain = 4, fast settling mode, bipolar
REFPx = +5V, REFNx = –5V

Figure 5-31. Code Change Glitch



Gain = 1, fast settling mode, bipolar
REFPx = +5V, REFNx = –5V

Figure 5-32. Glitch Variation Across Codes (Absolute Integral)



Gain = 1, fast settling mode, bipolar
REFPx = +5V, REFNx = –5V

Figure 5-33. Glitch Variation Across Codes (Direct Integral)

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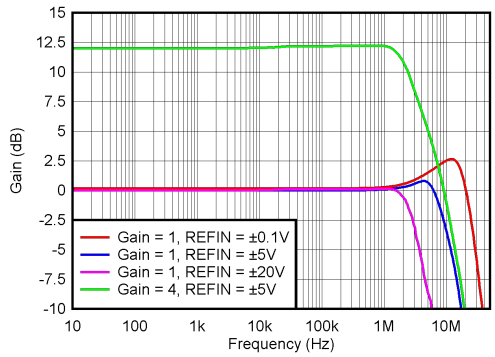
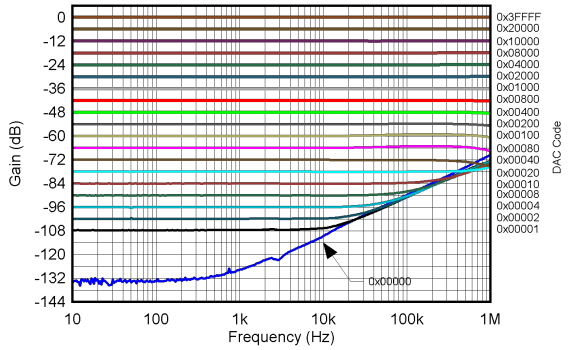
5.8.3 Typical Characteristics: Multiplying Mode

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



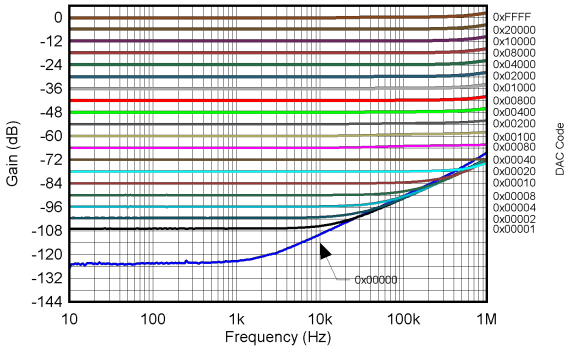
REFP = 0V, unipolar, full code

Figure 5-34. Reference Multiplying Bandwidth



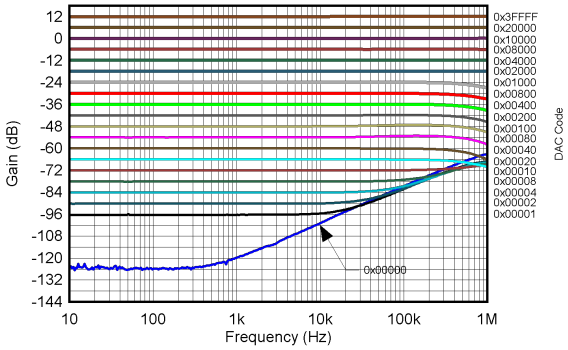
Gain = 1, unipolar, REFIN = $10V_{PP}$, REFP = 0V

Figure 5-35. Multiplying Feedthrough Response



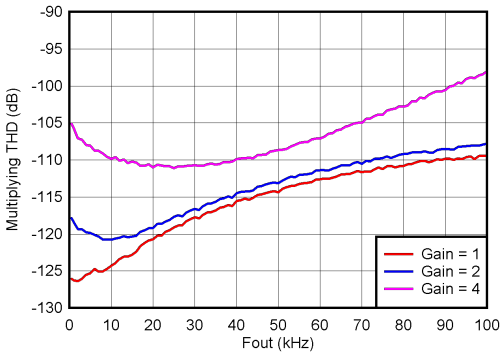
Gain = 1, unipolar, REFIN = $40V_{PP}$, REFP = 0V

Figure 5-36. Multiplying Feedthrough Response



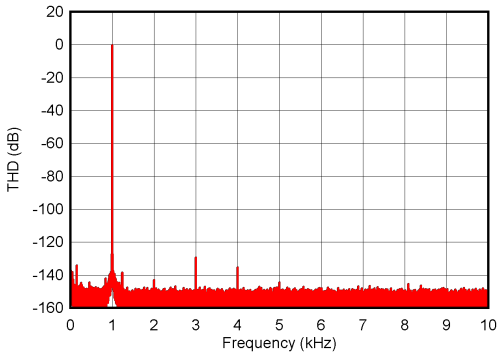
Gain = 4, unipolar, REFIN = $10V_{PP}$, REFP = 0V

Figure 5-37. Multiplying Feedthrough Response



Full code, unipolar mode, REFIN = $10V_{PP}$, REFP = 0V

Figure 5-38. Multiplying THD Across Frequency



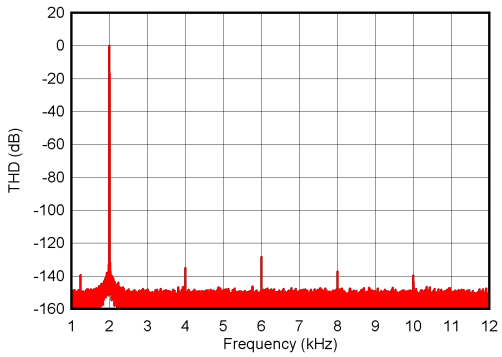
Gain = 1

Full code, unipolar mode, REFIN = $10V_{PP}$, REFP = 0V

Figure 5-39. Multiplying THD at Fout = 1kHz

5.8.3 Typical Characteristics: Multiplying Mode (continued)

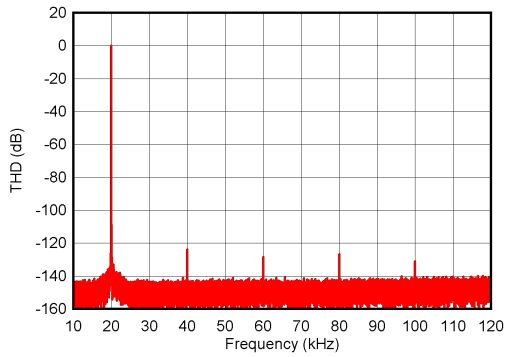
at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



Gain = 1

Full code, unipolar mode, REFIN = $10V_{PP}$, REFP = 0V

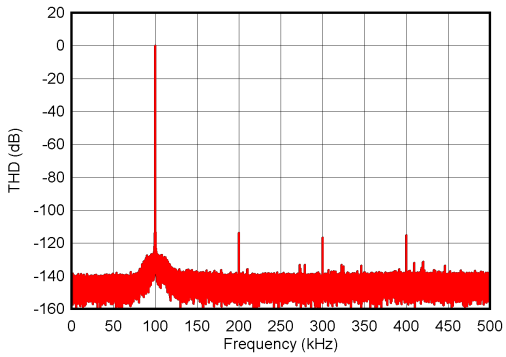
Figure 5-40. Multiplying THD at Fout = 2kHz



Gain = 1

Full code, unipolar mode, REFIN = $10V_{PP}$, REFP = 0V

Figure 5-41. Multiplying THD at Fout = 20kHz



Gain = 1

Full code, unipolar mode, REFIN = $10V_{PP}$, REFP = 0V

Figure 5-42. Multiplying THD at Fout = 100kHz

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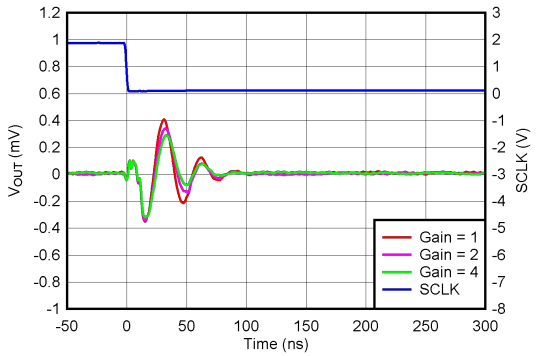
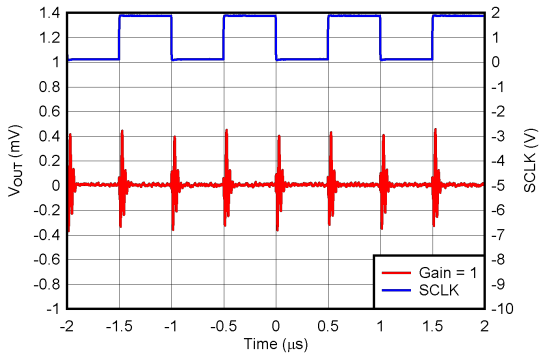
5.8.4 Typical Characteristics: Fast-Settling Mode

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



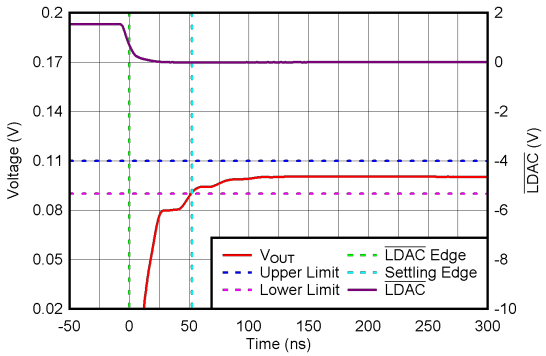
Bipolar mode, REFP = +5V, REFN = –5V

Figure 5-43. Digital Feedthrough Zoomed In



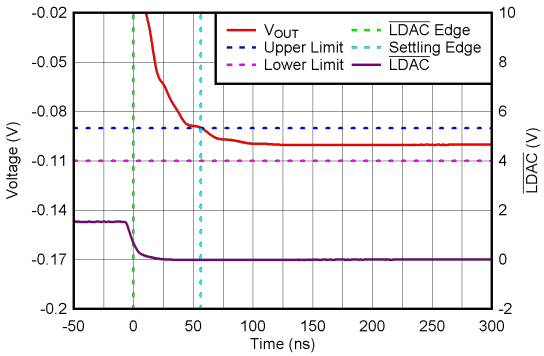
Bipolar mode, REFP = +5V, REFN = –5V
SCLK = 1MHz, midcode

Figure 5-44. Digital Feedthrough Zoomed Out



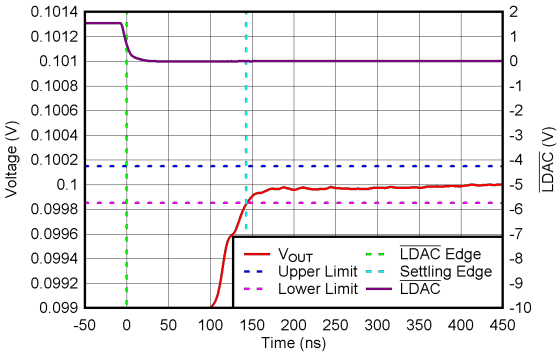
Gain = 1, reference: ±5V, rising step of: 100mV

Figure 5-45. Settling Time to 0.1% FSR



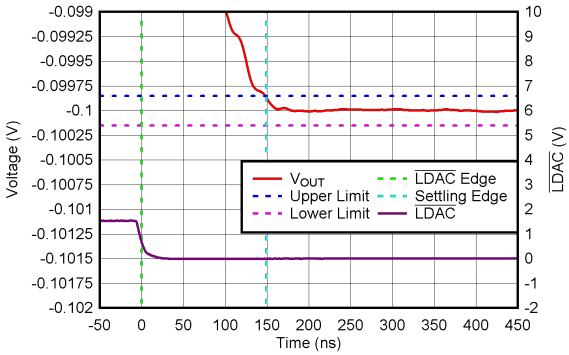
Gain = 1, reference: ±5V, falling step of: 100mV

Figure 5-46. Settling Time to 0.1% FSR



Gain = 1, reference: ±5V, rising step of: 100mV

Figure 5-47. Settling Time to 0.0015% FSR

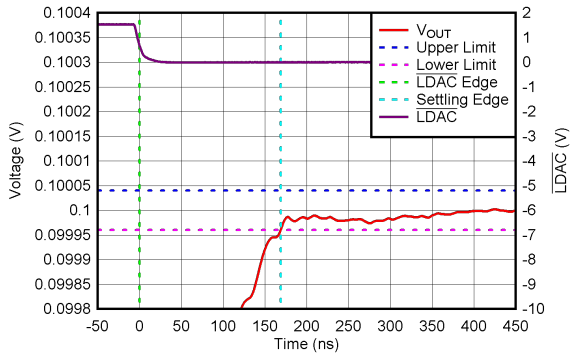


Gain = 1, reference: ±5V, falling step of: 100mV

Figure 5-48. Settling Time to 0.0015% FSR

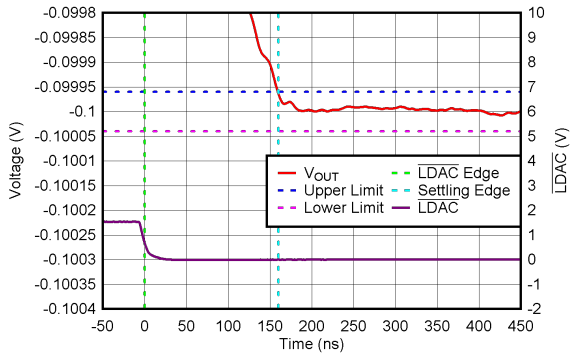
5.8.4 Typical Characteristics: Fast-Settling Mode (continued)

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



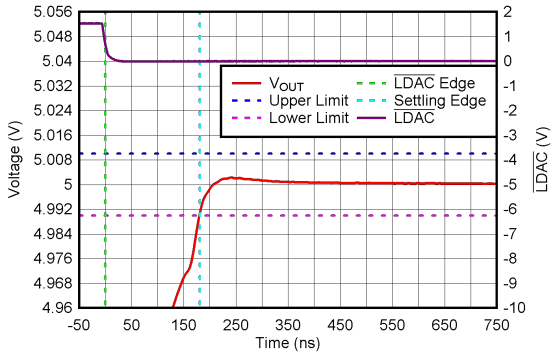
Gain = 1, reference: ±5V, rising step of: 100mV

Figure 5-49. Settling Time to 0.0004% FSR



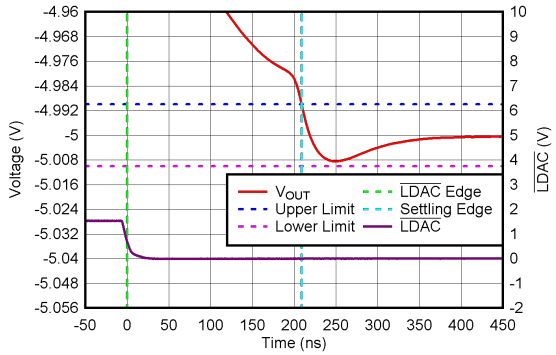
Gain = 1, reference: ±5V, falling step of: 100mV

Figure 5-50. Settling Time to 0.0004% FSR



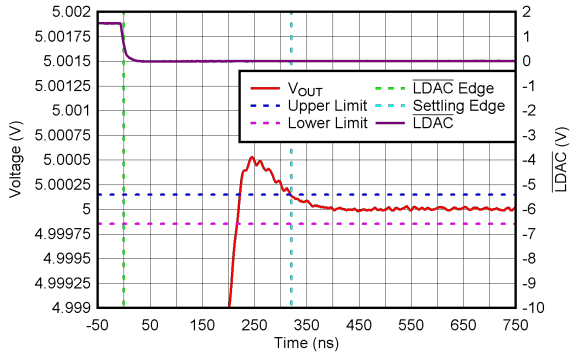
Gain = 1, reference: ±5V, rising step of: 10V

Figure 5-51. Settling Time to 0.1% FSR



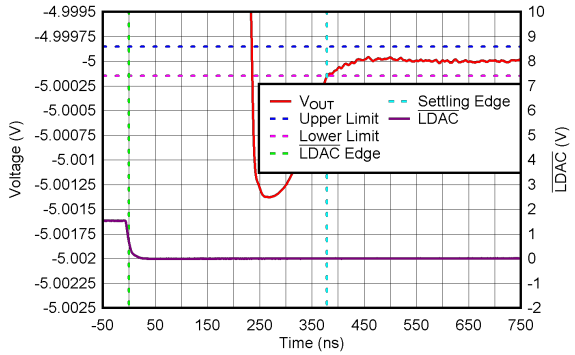
Gain = 1, reference: ±5V, falling step of: 10V

Figure 5-52. Settling Time to 0.1% FSR



Gain = 1, reference: ±5V, rising step of: 10V

Figure 5-53. Settling Time to 0.0015% FSR



Gain = 1, reference: ±5V, falling step of: 10V

Figure 5-54. Settling Time to 0.0015% FSR

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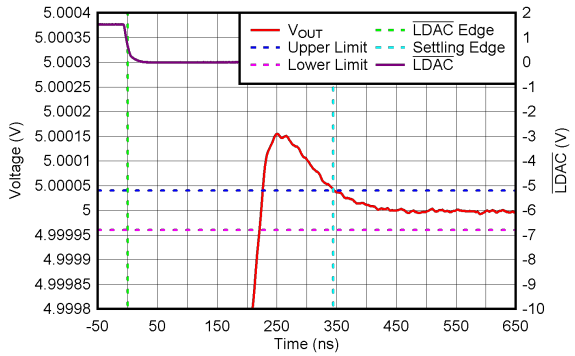
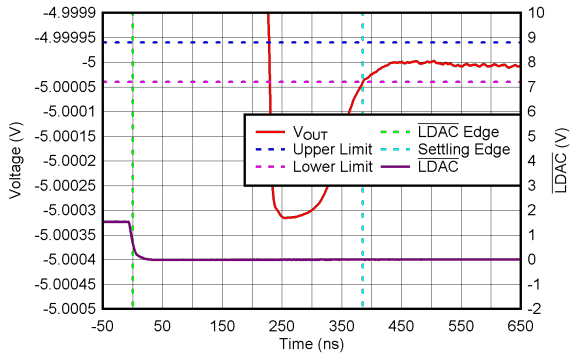
5.8.4 Typical Characteristics: Fast-Settling Mode (continued)

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



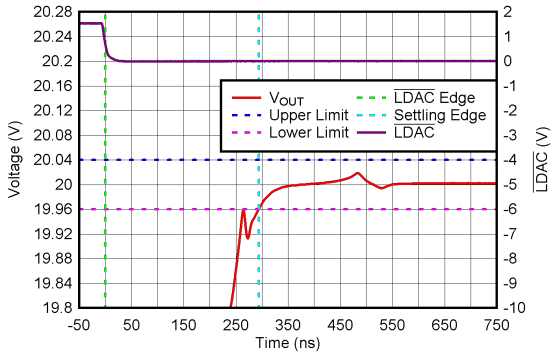
Gain = 1, reference: ±5V, rising step of: 10V

Figure 5-55. Settling Time to 0.0004% FSR



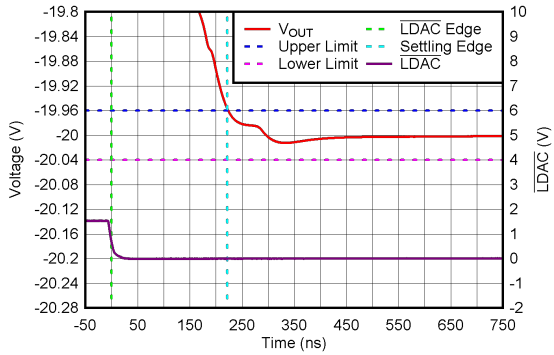
Gain = 1, reference: ±5V, falling step of: 10V

Figure 5-56. Settling Time to 0.0004% FSR



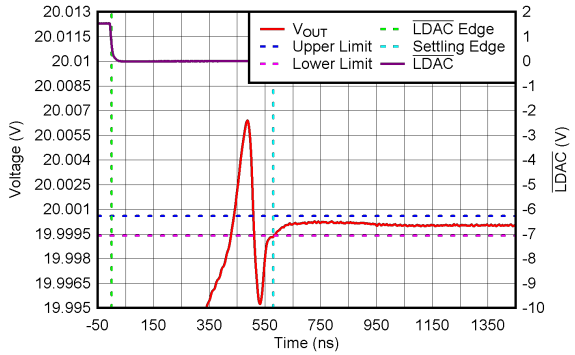
Gain = 1, reference: ±20V, rising step of: 40V

Figure 5-57. Settling Time to 0.1% FSR



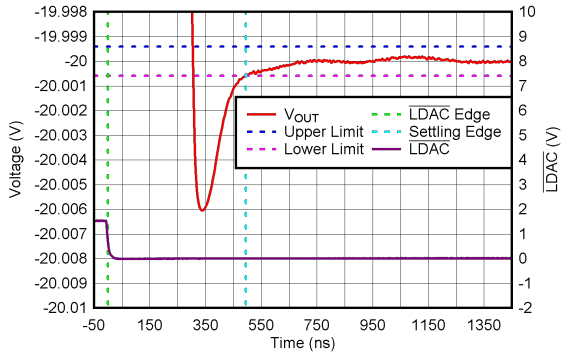
Gain = 1, reference: ±20V, falling step of: 40V

Figure 5-58. Settling Time to 0.1% FSR



Gain = 1, reference: ±20V, rising step of: 40V

Figure 5-59. Settling Time to 0.0015% FSR

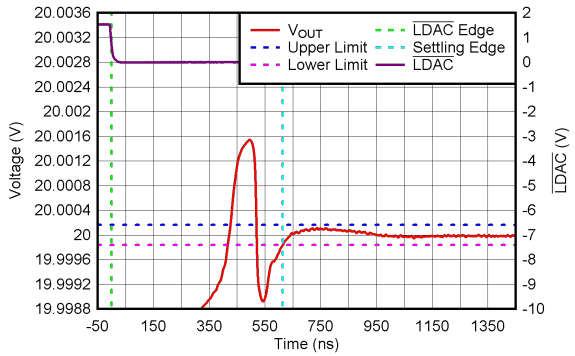


Gain = 1, reference: ±20V, falling step of: 40V

Figure 5-60. Settling Time to 0.0015% FSR

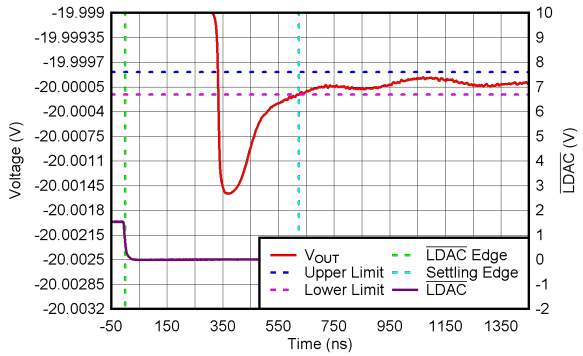
5.8.4 Typical Characteristics: Fast-Settling Mode (continued)

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



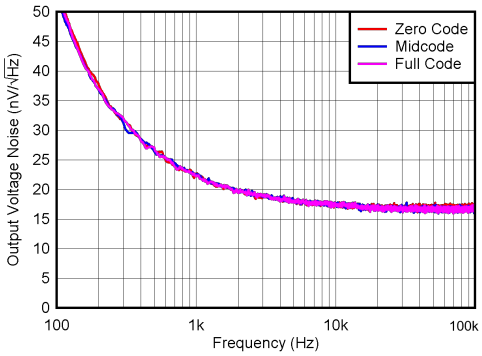
Gain = 1, reference: ±20V, rising step of: 40V

Figure 5-61. Settling Time to 0.0004% FSR



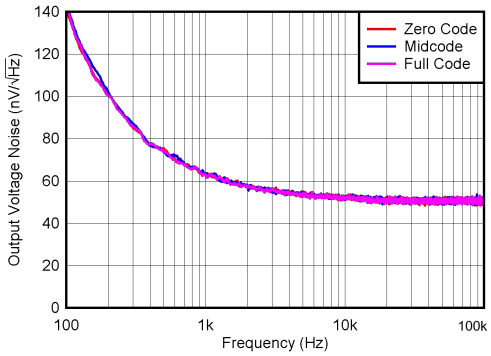
Gain = 1, reference: ±20V, falling step of: 40V

Figure 5-62. Settling Time to 0.0004% FSR



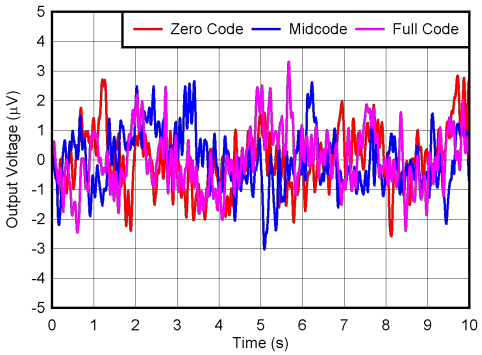
Gain = 1, excluding R1x and R2x resistors, bipolar

Figure 5-63. Output Noise vs Frequency



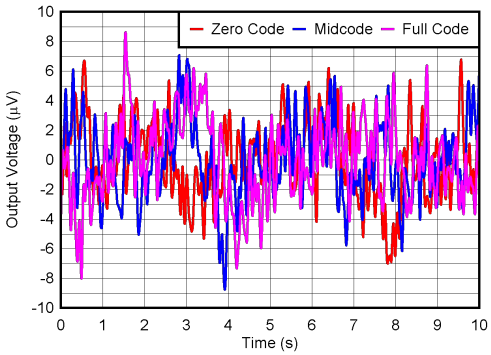
Gain = 4, excluding R1x and R2x resistors, bipolar

Figure 5-64. Output Noise vs Frequency



Gain = 1, bipolar mode

Figure 5-65. 0.1Hz to 10Hz Flicker Noise



Gain = 4, bipolar mode

Figure 5-66. 0.1Hz to 10Hz Flicker Noise

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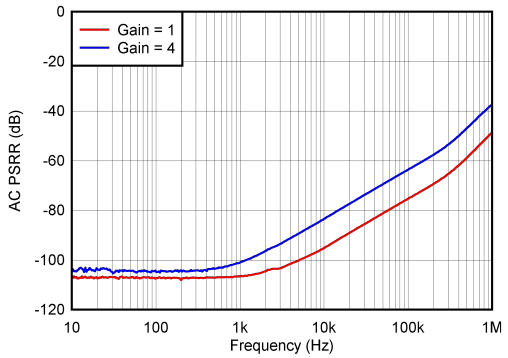
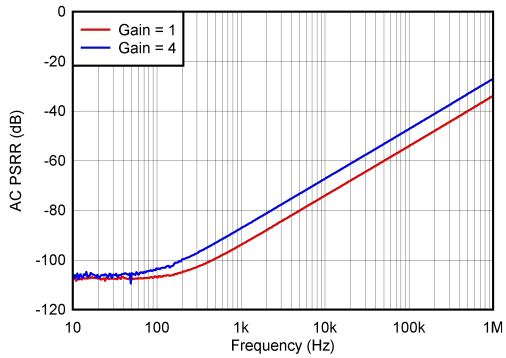
5.8.4 Typical Characteristics: Fast-Settling Mode (continued)

at T_A = –40°C to +125°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



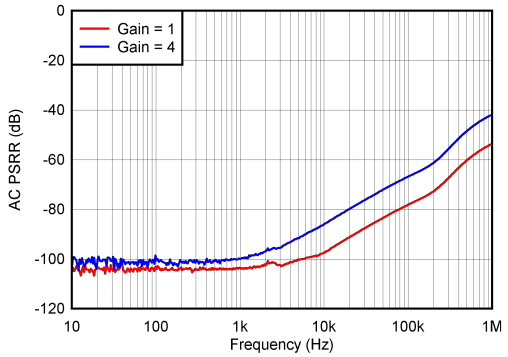
REFPx = +5V, REFNx = –5V, bipolar mode

Figure 5-67. VCC PSRR vs Frequency



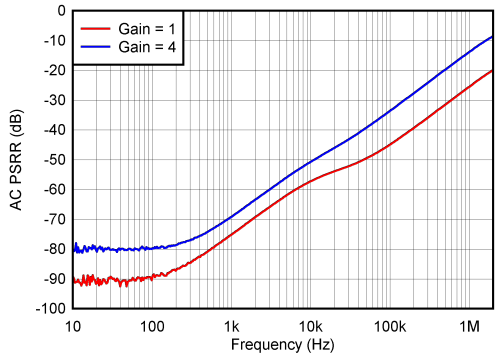
REFPx = +5V, REFNx = –5V, bipolar mode

Figure 5-68. VEE PSRR vs Frequency



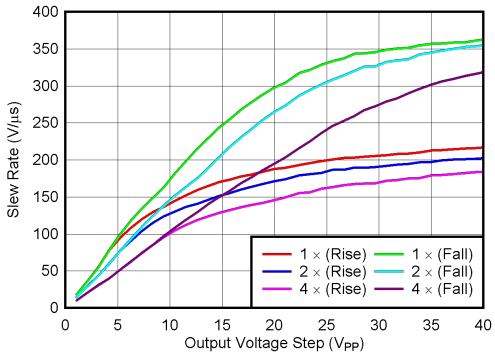
REFPx = +5V, REFNx = –5V, bipolar mode

Figure 5-69. AVDD PSRR vs Frequency



REFPx = +5V, REFNx = –5V, bipolar mode

Figure 5-70. LVDD PSRR vs Frequency

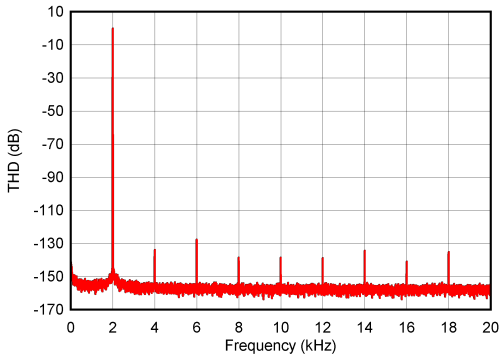


REFPx = +5V, REFNx = –5V

Figure 5-71. Slew Rate vs Output Voltage Step, Bipolar

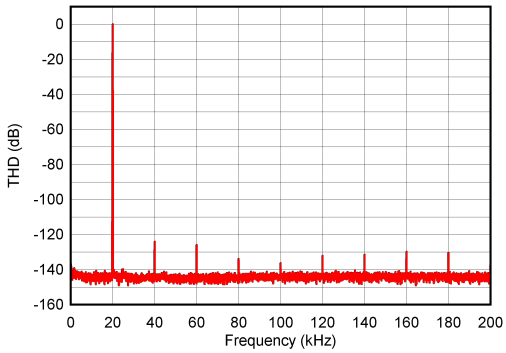
5.8.5 Typical Characteristics: AWG Mode

at T_A = –40°C to +100°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



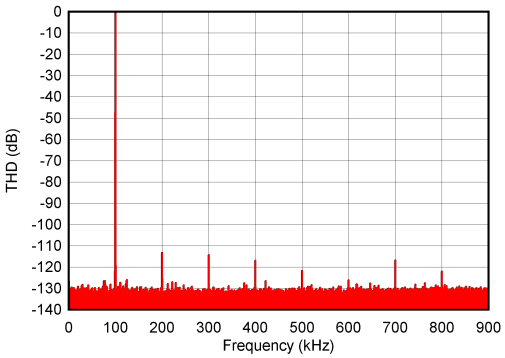
Gain = 1, REFPx = +5V, REFNx = –5V
Output swing: $10V_{PP}$, sampling frequency (f_S): 5MHz

Figure 5-72. Single Tone Spectrums at 2kHz



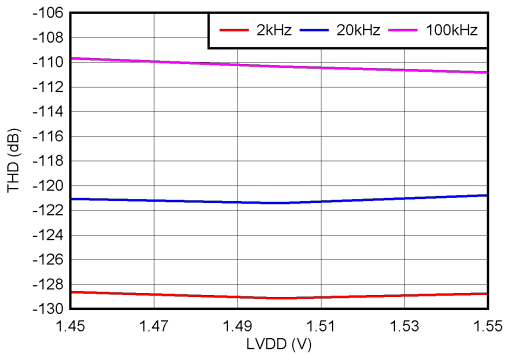
Gain = 1, REFPx = +5V, REFNx = –5V
Output swing: $10V_{PP}$, sampling frequency (f_S): 5MHz

Figure 5-73. Single Tone Spectrums at 20kHz



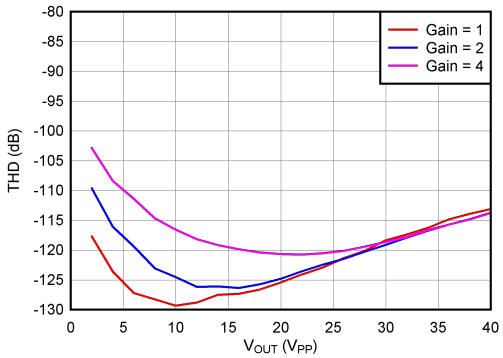
Gain = 1, REFPx = +5V, REFNx = –5V
Output swing: $10V_{PP}$, sampling frequency (f_S): 5MHz

Figure 5-74. Single Tone Spectrum at 100kHz



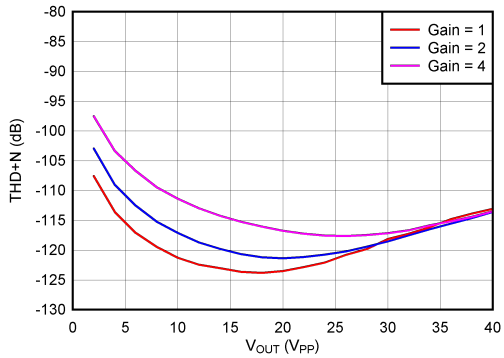
Gain = 1, REFPx = +5V, REFNx = –5V
Output swing: $10V_{PP}$, sampling frequency (f_S): 5MHz

Figure 5-75. THD vs LVDD



References scaled to accommodate full swing at given gain
Sampling frequency (f_S): 5MHz

Figure 5-76. THD vs V_{OUT} Swing at 2kHz



References scaled to accommodate full swing at given gain
Sampling frequency (f_S): 5MHz

Figure 5-77. THD+N vs V_{OUT} Swing at 2kHz

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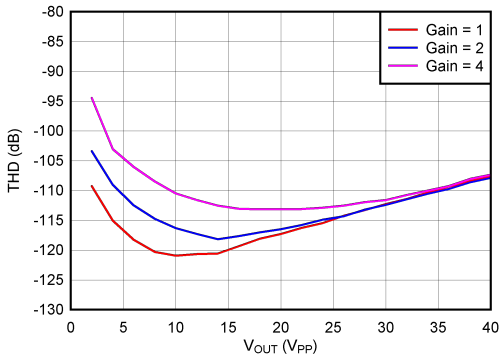
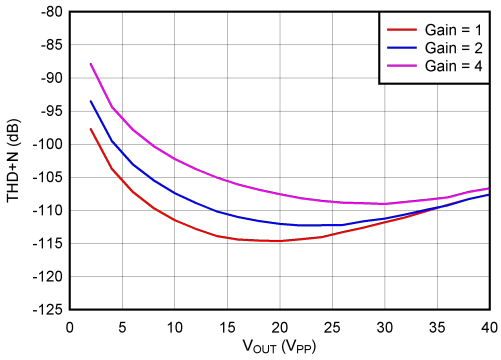
5.8.5 Typical Characteristics: AWG Mode (continued)

at T_A = –40°C to +100°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



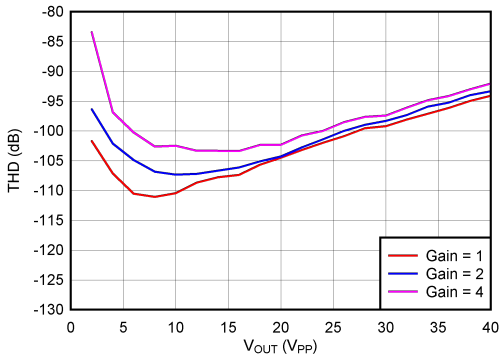
References scaled to accommodate full swing at given gain
Sampling frequency (f_S): 5MHz

Figure 5-78. THD vs V_{OUT} Swing at 20kHz



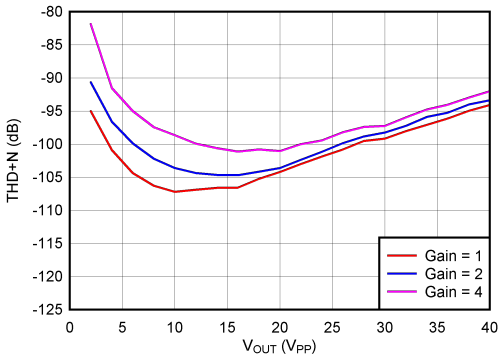
References scaled to accommodate full swing at given gain
Sampling frequency (f_S) : 5MHz

Figure 5-79. THD+N vs V_{OUT} at 20kHz



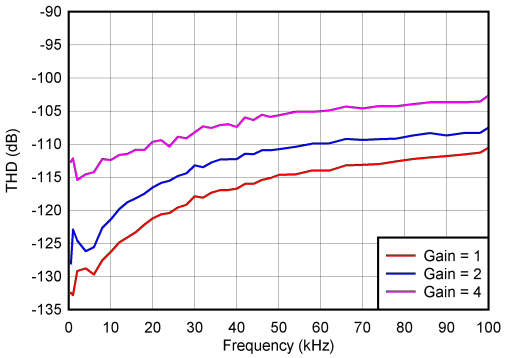
References scaled to accommodate full swing at given gain
Sampling frequency (f_S): 5MHz

Figure 5-80. THD vs V_{OUT} Swing at 100kHz



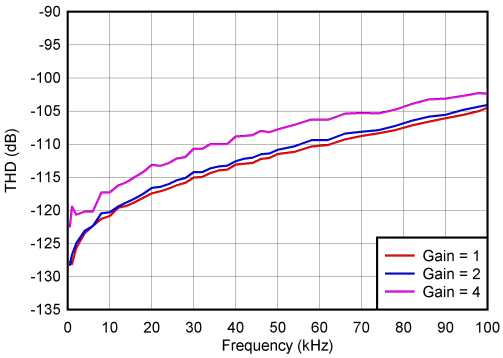
References scaled to accommodate full swing at given gain
Sampling frequency (f_S): 5MHz

Figure 5-81. THD+N vs V_{OUT} Swing at 100kHz



References scaled to accommodate full swing at given gain
Sampling frequency (f_S) : 5MHz

Figure 5-82. THD vs Frequency at V_{OUT} Swing $10V_{PP}$

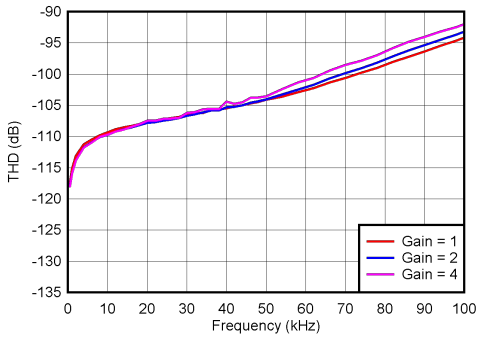


References scaled to accommodate full swing at given gain
Sampling frequency (f_S) : 5MHz

Figure 5-83. THD vs Frequency at V_{OUT} Swing $20V_{PP}$

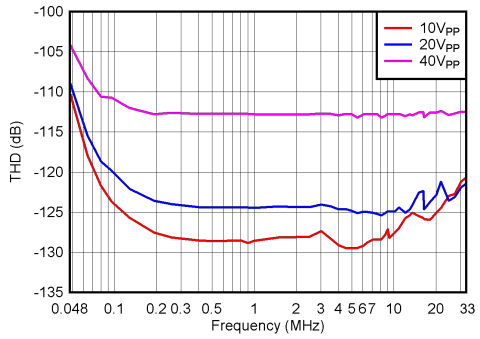
5.8.5 Typical Characteristics: AWG Mode (continued)

at T_A = –40°C to +100°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



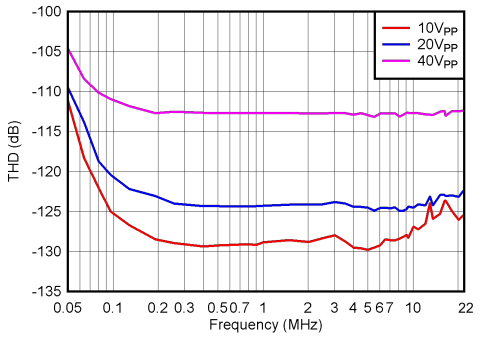
References scaled to accommodate full swing at given gain
Sampling frequency (f_S) : 5MHz

Figure 5-84. THD vs Frequency at V_{OUT} Swing $40V_{PP}$



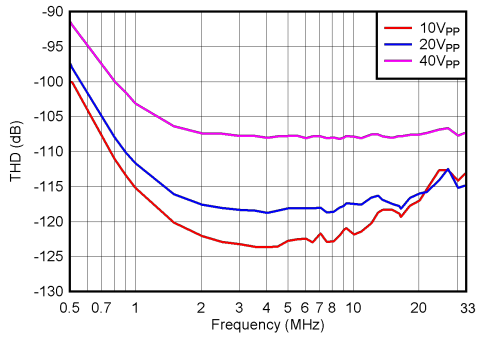
Gain = 1
References scaled to accommodate full swing at given gain

Figure 5-85. THD vs Sampling (f_S) Frequency Across Output Amplitudes for f_{OUT} = 2kHz, High Speed Mode (16-bit)



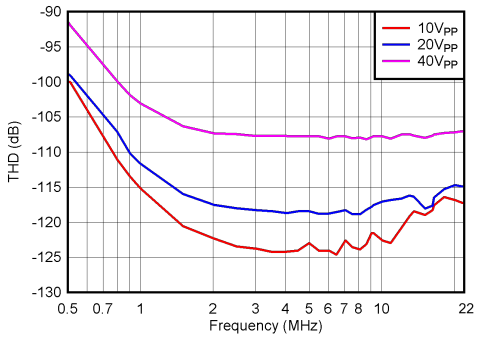
Gain = 1
References scaled to accommodate full swing at given gain

Figure 5-86. THD vs Sampling (f_S) Frequency Across Output Amplitudes for f_{OUT} = 2kHz, High Resolution Mode (18-bit)



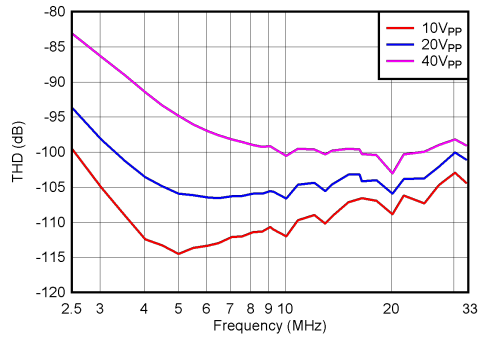
Gain = 1
References scaled to accommodate full swing at given gain

Figure 5-87. THD vs Sampling (f_S) Frequency Across Output Amplitudes for f_{OUT} = 20kHz, High Speed Mode (16-bit)



Gain = 1
References scaled to accommodate full swing at given gain

Figure 5-88. THD vs Sampling (f_S) Frequency Across Output Amplitudes for f_{OUT} = 20kHz, High Resolution Mode (18-bit)



Gain = 1
References scaled to accommodate full swing at given gain

Figure 5-89. THD vs Sampling (f_S) Frequency Across Output Amplitudes for f_{OUT} = 100kHz, High Speed Mode (16-bit)

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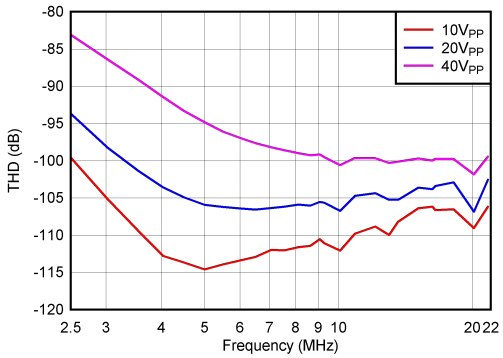
5.8.5 Typical Characteristics: AWG Mode (continued)

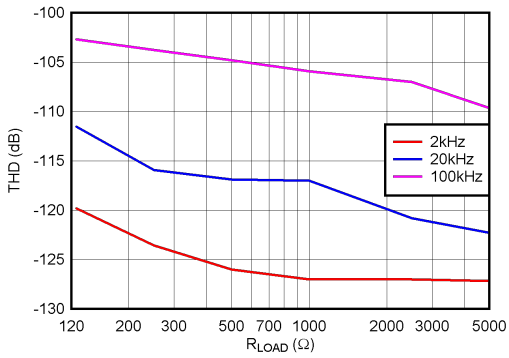
at T_A = –40°C to +100°C, VCC = +8.5V to +23.5V, VEE = –8.5V to –23.5V, AVDD = 5.0V, DVDD = 1.5V, LVDD = 1.5V, VIO = 1.5V, VOSADJ_ENx = 0, OFS_ENx = 0, ROFS_F = ROFS_S = VOSADJ = AGND see note for VREFP and VREFN, and all typical values at T_A = 25°C, output unloaded (unless otherwise noted)



Gain = 1

References scaled to accommodate full swing at given gain

Figure 5-90. THD vs Sampling (f_S) Frequency Across Output Amplitudes for f_{OUT} = 100kHz, High Resolution Mode (18-bit)



Gain = 1

Figure 5-91. THD vs R_{LOAD} at $10V_{PP}$

6 Detailed Description

6.1 Overview

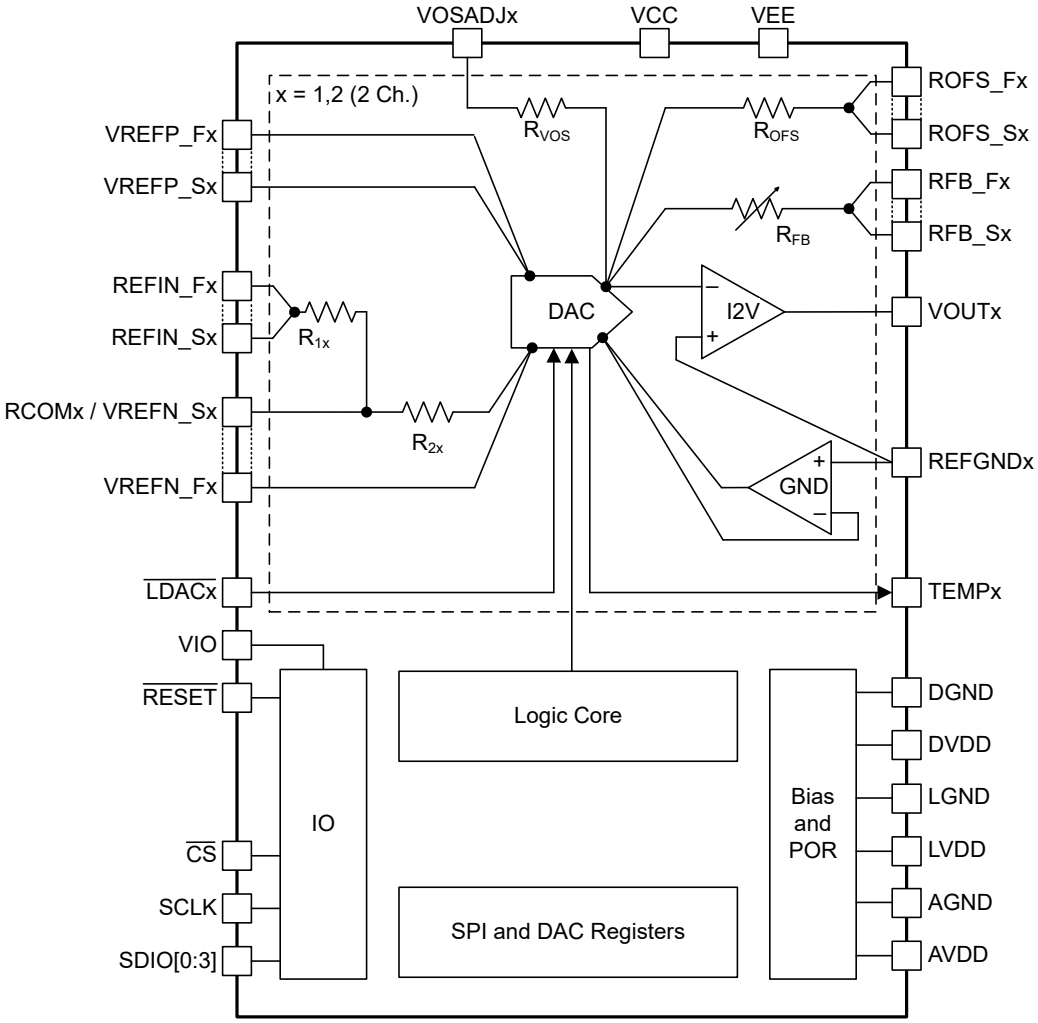
The DAC90802 is a dual-channel, 18-bit, voltage output, digital-to-analog converter (DAC) using a proprietary multiplying DAC (MDAC) architecture.

Each channel has an independent full-featured DAC, including resistor connections for feedback (RFB), offset (ROFS), offset-adjust (VOSADJ), Load-DAC ($\overline{\text{LDAC}}$), temperature sensor outputs (TEMP), references (VREFP, VREFN), and matched reference inversion (REFIN, RCOM).

The channels of the DAC90802 share a quad-SPI compatible serial data interface, with four data input-output lines (SDIO0-SDIO3), chip-select ($\overline{\text{CS}}$), and serial clock (SCLK) inputs. Use the asynchronous active-low $\overline{\text{RESET}}$ pin to reset DAC codes and the functional state of the device. In addition, use the $\overline{\text{LDAC}}$ inputs to synchronize the DAC outputs with the overall system signals.

The DAC90802 requires external reference voltages. Select among unipolar, biploar, and asymmetric operation using the reference, reference inversion, and offset pin configurations. Configure the offset adjust pin to finetune the offset errors in the overall system. The DAC90802 incorporates a power-on reset (POR) circuit to make sure that the DAC outputs are pulled down to zero using a 5kΩ resistor.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Digital-to-Analog Converters

The DAC90802 implements a current-steering R-2R ladder architecture. Figure 6-1 shows a typical equivalent DAC channel. Each DAC contains a matching feedback resistor for use with the internal I-to-V conversion amplifier. The RFB pins are connected to the output of the amplifier.

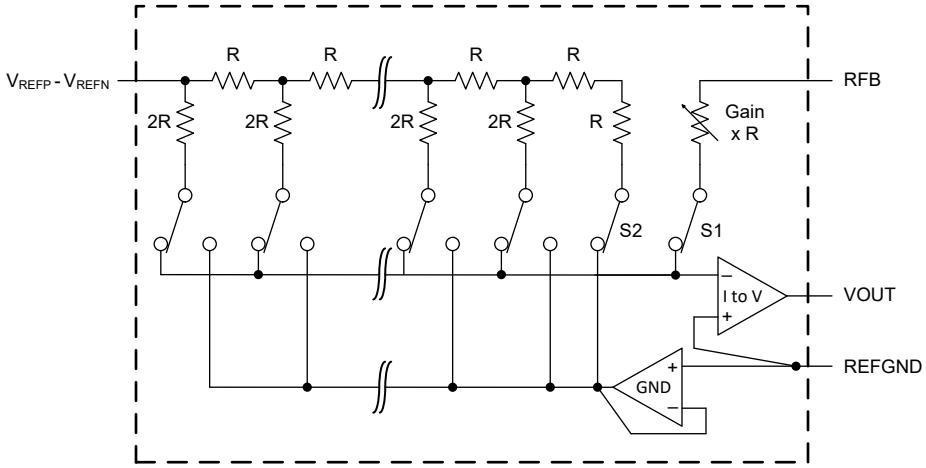

Figure 6-1. Typical Equivalent DAC Channel

The DAC90802 support both DC and AC reference voltage inputs. A matched internal feedback resistor network at RFB allows users to digitally select the gain G_{FB} of the DAC output voltage either as 1V/V, 2V/V or as 4V/V. Power along with the proper gain selection must be applied to the device to achieve continuity while measuring RFB. Equation 1 defines the DAC transfer function.

$$V_{OUT} = -\left[G_{FB} \cdot \left(V_{REFP} - V_{REFP}\frac{n}{2^N} + V_{REFN}\frac{n}{2^N}\right) + G_{OFF} \cdot V_{OFF} + G_{ADJ} \cdot V_{ADJ}\right] \cdot [1 + G_{OV}] \quad (1)$$

Where,

$G_{FB} = \frac{R_{FB}}{R_{DAC}}$ is the gain setting of the DAC,

n is the programmed DAC code,

N is the DAC resolution,

V_{REFP}, V_{REFN} are the reference voltages applied to VREFP and VREFN pins respectively,

V_{OFF}, V_{ADJ} are the coarse-offset and fine-offset voltages applied to using ROFS and VOSADJ pins, respectively (see Section 6.3.1.4 for details),

$G_{OFF} = \frac{R_{FB}}{R_{OFS}}$, $G_{ADJ} = \frac{R_{FB}}{R_{VOS}}$ are the coarse-offset adjust and fine-offset adjust gains respectively (see Section 6.3.1.4 for details),

and,

V_{OUT} is the DAC output voltage

Note

Use the DAC resolution N according to the register used to write the code n. For example, when using the 16b register in the 18-b DAC90802, N is 16.

For basic unipolar operation (without offset or adjust voltages), where $V_{REFP} = 0$, $V_{REFN} = -V_{REF}$

$$V_{OUT} = G \times V_{REF} \frac{n}{2^N} \tag{2}$$

and the zero-code, mid-code and full code values are

$V_{OUT}^{n=0} = 0$, $V_{OUT}^{n=2^{N-1}} = G \times \frac{V_{REF}}{2}$, $V_{OUT}^{n=2^N-1} = G \times V_{REF}\left(1 - \frac{1}{2^N}\right)$ respectively.

For basic bipolar operation (without offset or adjust voltages), where $V_{REFP} = V_{REF}$, $V_{REFN} = -V_{REF}$

$$V_{OUT} = -G\left(V_{REF} - 2\,V_{REF}\frac{n}{2^N}\right) = G \times V_{REF}\left(\frac{2n - 2^N}{2^N}\right) \tag{3}$$

and the zero-code, mid-code and full code values are

$V_{OUT}^{n=0} = -G \times V_{REF}$, $V_{OUT}^{n=2^{N-1}} = 0$, $V_{OUT}^{n=2^N-1} = G \times V_{REF}\left(1 - \frac{1}{2^{N-1}}\right)$ respectively.

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6.3.1.1 Reference

The architecture of DAC90802 enables use of both AC and DC reference signals, and accommodates input reference voltages up to V_{REF} as specified in *Electrical Characteristics* on each independent DAC channel. The reference voltage inputs VREFP, and VREFN exhibit a constant nominal input resistance across codes. Design reference driving circuits to enable drive capability as described by I_{REFP}, and I_{REFN}. Use of the matched reference-inversion resistors connected between REFIN and RCOM with an appropriate op amp for signal inversion is optional. Include the linearity of R_1/R_2 in system error calculations for full-bipolar operation when using the single-reference connection. Tie REFGND as a ground sense line for any reference voltages used for the DAC.

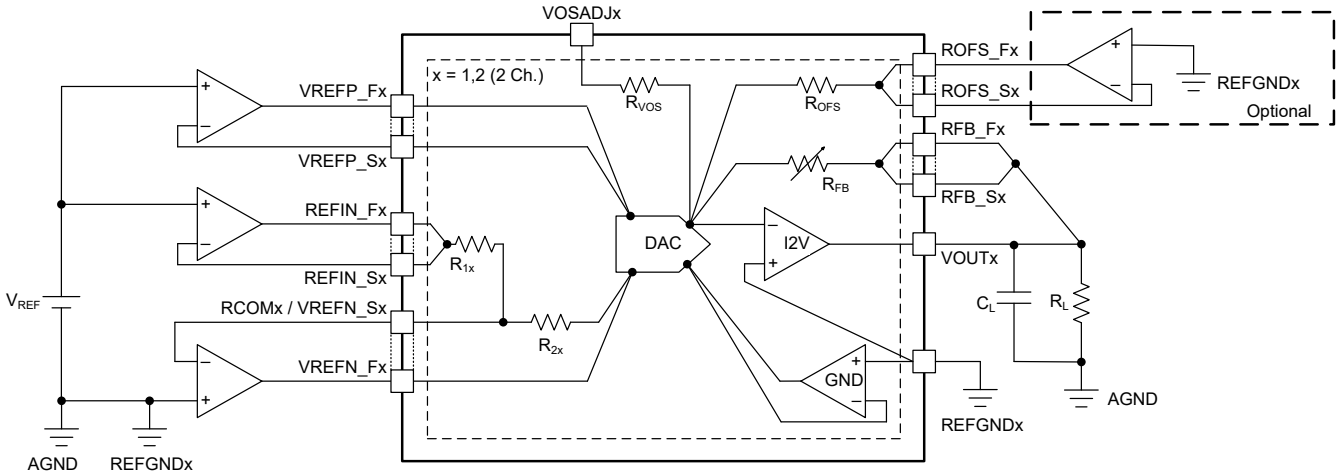

Figure 6-2. Single Reference Connections

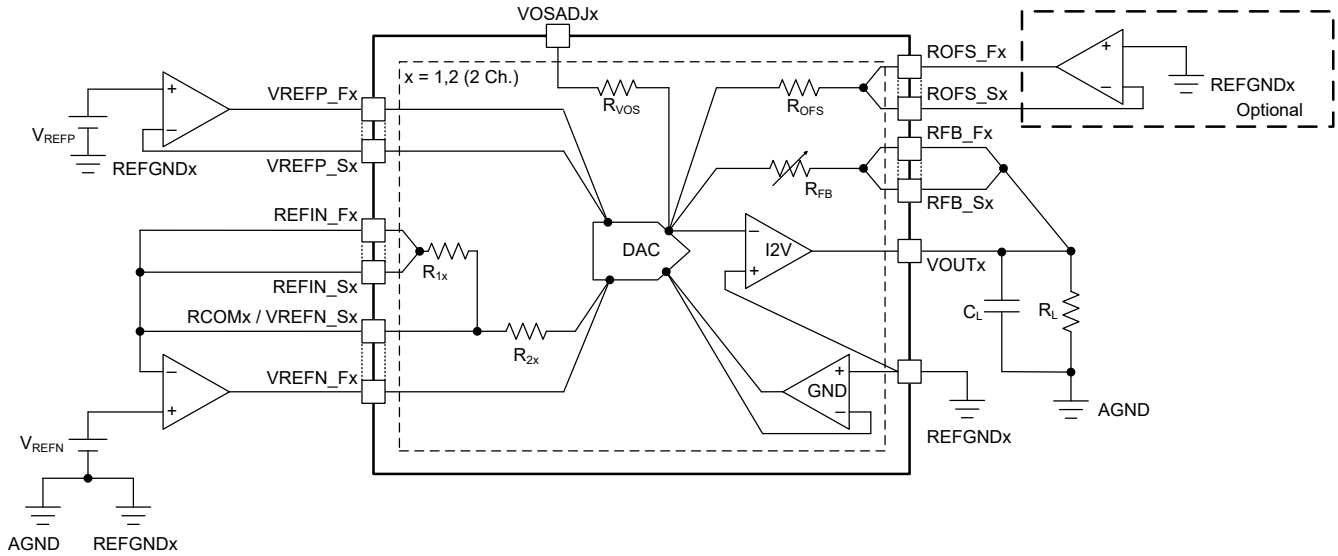

Figure 6-3. Dual Reference Connections

6.3.1.2 Output Span

The DAC90802 voltage output is limited by the output range of the I-to-V to V_{OUT} (as specified in *Electrical Characteristics*). Connect the voltage at VOUT to the feedback RFB maintaining output capacitance within the specified maximum C_{LOAD} for high speed, stable performance of the internal I-to-V amplifier. Insert a series resistor to extend the usable C_{LOAD} range.

Use the ROFS pin to introduce a coarse offset into the current output node of the DAC90802. The internal R_{OFS} coarse offset resistor is matched to R_{DAC} for a fixed gain G_{OFF}. Use the VOSADJ pin to introduce a fine offset into the current output node of the DAC90802. The internal R_{VOS} fine offset resistor is matched to R_{DAC} for a fixed gain G_{ADJ}. Typical use of this adjustment includes calibration of small offsets for the DAC output.

6.3.1.2.1 Gain Overrange

Feedback resistor options at RFB pins include a gain overrange G_{OV} in the nominal gain G. Gain overrange allows the post calibration system performance to have a full dynamic range with the correct gain. Use the full resolution N of the DAC90802 to maintain DNL performance with no missing codes for the overall system. All end-point code error specifications of DAC90802 in Section 5.5 are specified with overrange accounted for.

6.3.1.3 Output Synchronization

As shown in Figure 6-4, the DAC90802 uses a double buffered architecture that allows precise timing control of the output.

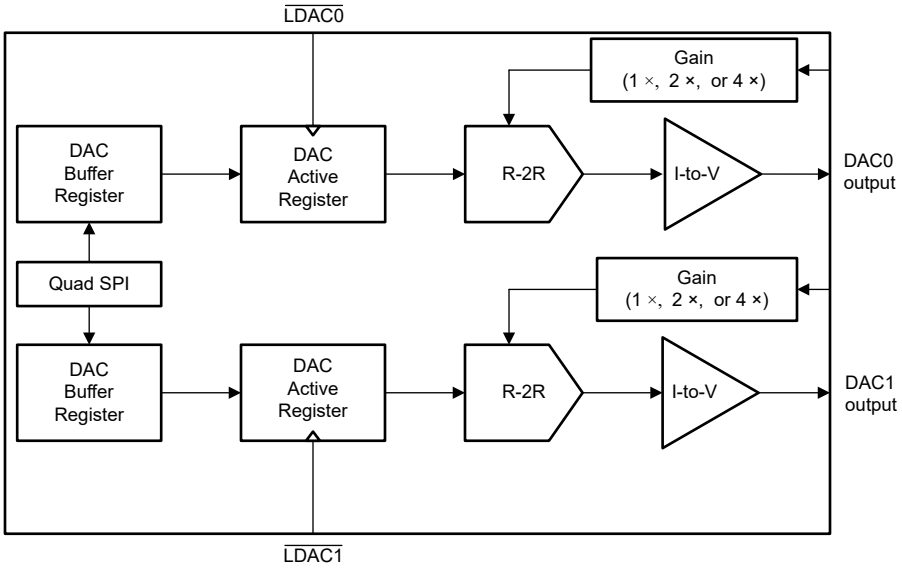

Figure 6-4. Double Buffered DAC Architecture

The DAC90802 supports timing control in one of three following DAC update methods.

- Asynchronous update (ASYNC_UPDT = 1, SFT_LDAC_EN = Don't care)
  - The End-Of-Packet (EOP) in the SPI frame controls the DACs last output buffer independently per channel; the $\overline{LDAC}$ input does not have any effect
  - For 16-bit data registers, EOP is the end of the second 8-bit data byte, with actual cycle count being a function of the SPI mode of operation
  - Since DAC90802 does not implement a broadcast mode, this mode is not recommended if multiple channels of the DAC need synchronization
  - This mode has the lowest latency intended for use in fast control loops and similar applications where latency is the primary constraint; for example, in fast settling mode
- Synchronous SPI based update (ASYNC_UPDT = 0, SFT_LDAC_EN = 1)

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  - SFT_LDAC triggers the buffer update; the $\overline{\text{LDAC}}$ input does not have any effect
  - The EOP in the SFT_LDAC SPI frame triggers the DAC update
  - Complementary to the asynchronous update method, synchronous SPI based update provides a direct method to synchronize all channels of the DAC90802 using SPI since the SFT_LDAC_EN allows every selected channel to receive the update simultaneously.
  - In the absence of a physical $\overline{\text{LDAC}}$ input, the SFT_LDAC provides a method to synchronize DAC channels for the best AC performance; for example, in multiplying mode
- Synchronous $\overline{\text{LDAC}}$ update (ASYNC_UPDT = 0, SFT_LDAC_EN = 0)
  - $\overline{\text{LDAC}}$ acts as a high precision, low jitter, clock input to the last buffer of the DAC enabling the most precise timing control
  - Synchronous $\overline{\text{LDAC}}$ control via precision clock signals is the most accurate method for DAC output timing and skew control
  - DAC90802 supports independent $\overline{\text{LDAC}}$ inputs per DAC channel. This feature enables multiple use cases such as output interpolation, full signal chain skew equalization, and so on
  - For ultra-low THD applications, use synchronous $\overline{\text{LDAC}}$ update using a low-jitter clock to achieve the best performance with the DAC; for example, in AWG mode

6.3.1.4 Thermal Sensors

The DAC90802 features a per channel thermal sensor output that is selectable between an analog voltage or an internally triggered thermal flag digital state output. Pin output capabilities differ in each mode, and are specified in Section 5.5.

The DAC90802 is designed with ultra high precision, ultra low thermal coefficient matched resistors for low thermal noise applications that are yet capable of high voltages. Thermal management and systematic self heating compensation is a requirement for high voltage, low noise applications. Use the TEMP analog output mode, and an external ADC to adjust for systematic self-heating digitally in the system controller or FPGA that is used to drive the DAC. For applications that do not require the self-heating correction, use the TEMP in digital mode (with appropriate digital fan-out buffers, if needed) as a thermal flag output.

6.3.2 Power-On

The DAC90802 requires multiple power supply rails. The DAC90802 incorporates a power on reset (POR) circuit to make sure that the DAC outputs are pulled down to zero using a 5kΩ resistor.. Asserting an active low signal on $\overline{\text{RESET}}$ resets the device and clears all registers, with the same result as a POR event. While any sequence of power domains followed by reference voltages is usable, the recommended sequence is per Table 6-1.

Table 6-1. Power Supplies and Reference Recommended Sequence

Sequence	Purpose	Pins
1	Analog High Voltage Negative Rail	VEE
2	Analog High Voltage Positive Rail	VCC
3	Analog Low Voltage Rail	AVDD
4	Digital and Communications Power	LVDD, VIO
5	Digital Core Power	DVDD
6	References (as used)	VREFP, VREFN, REFIN, ROFS, VOSADJ

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6.3.3 Serial Data Interface

The DAC90802 uses a versatile, shared quad–SPI for the two DAC channels. The SPI port supports wiring in various methods from high-speed, write-only quad-SPI (four data input pins) mode to daisy-chain mode (multiple devices on shared wires). This device supports both SDR (single data rate) and DDR (dual data rate) at up to 66MHz SCLK frequency in most configurations, with some limitations in daisy-chain and readback modes. Data is always aligned MSB first.

In the SDR mode, data placed on the active SDIO pins is clocked into the register starting with the first valid falling edge of SCLK. In this mode, each active SDIO pin per SCLK cycle captures one bit from the data frame. In the DDR mode, data are clocked into the register on both valid rising and falling edges of SCLK, the first sampling being done at the rising edge. In this mode, two bits of data are captured at each active SDIO pin per SCLK cycle.

An SCLK edge is valid when $\overline{CS}$ is low, after accounting for the specified set-up and hold times. Holding the $\overline{CS}$ pin low for cycle counts inconsistent with the selected operating mode is not recommended. This condition can lead to incorrect data capture or ignored data packet.

6.3.3.1 SPI Configurations

In the default SPI mode of operation the SPI write of DAC90802 uses a 40-bit data frame for all registers, except for the DAC_DATA_CHx_X registers. The CHx_DATA_HS register uses a 24-bit frame and the CHx_DATA_HR register uses a 32 bit frame. The R/W bit and the seven address bits are followed by either 32, 24 or 16 bits of data. In configurations where data readback is supported, the readback data frame also confirms to the write cycle preceding the readback. In SPI stream mode, the R/W bit and address bits are skipped, allowing faster data transfer to the DACs.

For standard SPI, while using only SDIO0 as input, the frame length options are shown in Figure 6-5, Figure 6-7, and Figure 6-6.

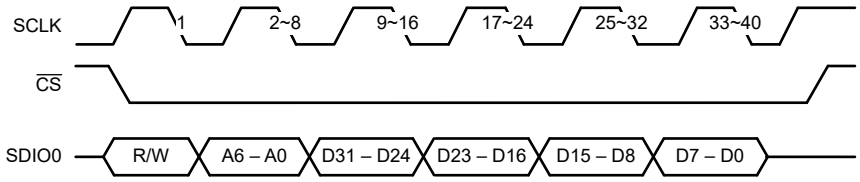

Figure 6-5. SDR Standard SPI 40 Bits Frame

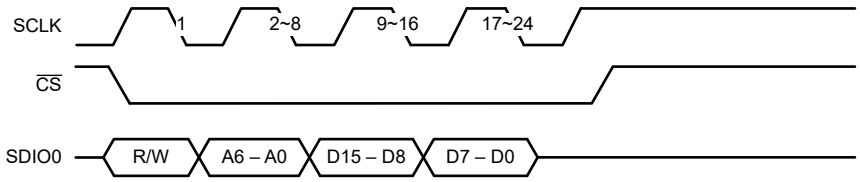

Figure 6-6. SDR Standard SPI 24 Bits Frame for CHx_DATA_HS Registers

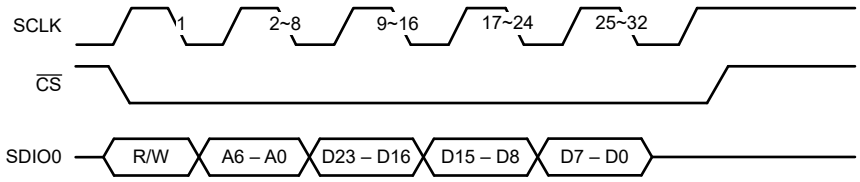

Figure 6-7. SDR Standard SPI 32 Bits Frame for CHx_DATA_HR Registers

The quad-SPI width is also selectable between standard SPI, dual-SPI, and quad-SPI with pin configurations as per Table 6-2. This device supports single or dual data-rate communication including stream mode for data registers in any SPI-width configuration. The default configuration is SDR mode with standard SPI.

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Table 6-2. Supported Quad-SPI Pin Widths

SPI Width Mode	Standard SPI (SPI_CFG.SPI_MIO = 0x0)		Dual SPI (SPI_CFG.SPI_MIO = 0x1)		Quad SPI (SPI_CFG.SPI_MIO = 0x2)	
Data Rate Mode (SPI_CFG.SPI_DDR)	SDR	DDR	SDR	DDR	SDR	DDR
Serial Data Inputs	SDIO0 only		SDIO0, and SDIO1		SDIO0, SDIO1, SDIO2, and SDIO3	
Serial Data Outputs	SDIO3 only	DDR not supported	SDIO2 and SDIO3	DDR not Supported	Readback not supported	

Table 6-3. Supported Data Frame Lengths With Address Bytes

Field	Address Bytes	Data Bytes	Standard SPI		Dual SPI		Quad SPI	
			SDR	DDR	SDR	DDR	SDR	DDR
CHx_DATA_HS	1	2	24 cycles	12 cycles	12 cycles	6 cycles	6 cycles	3 cycles
CHx_DATA_HR	1	3	32 cycles	16 cycles	16 cycles	8 cycles	8 cycles	4 cycles
Others	1	4	40 cycles	20 cycles	20 cycles	10 cycles	10 cycles	5 cycles

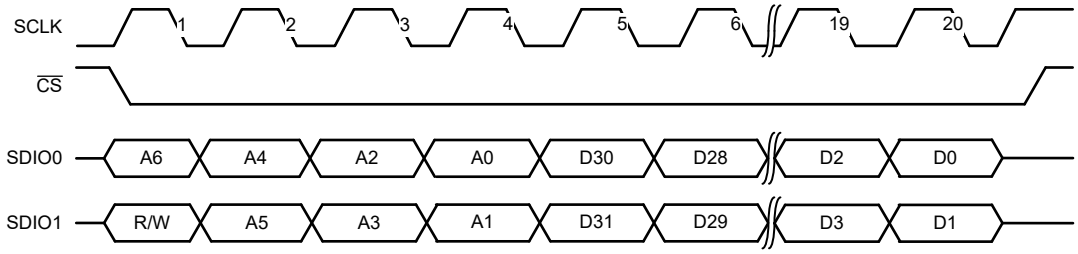

Figure 6-8. SDR Dual-SPI 40-Bit Frame

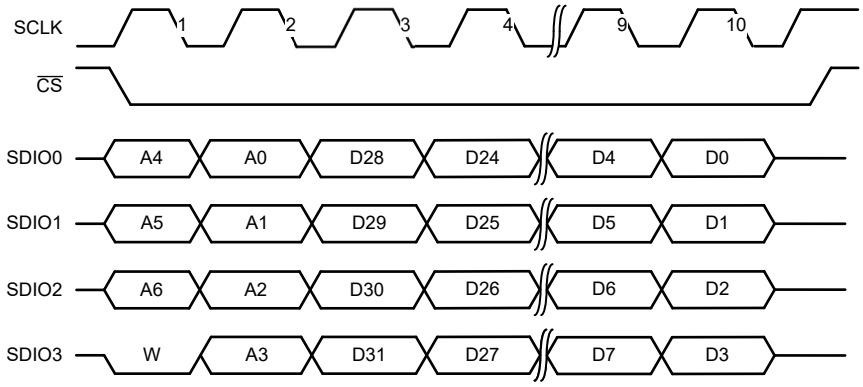

Figure 6-9. SDR Quad-SPI 40-Bit Frame

6.3.3.2 SPI Stream Mode

Use the DAC90802 stream mode to maximize write throughput to the DAC, and avoid the repeated use of an address byte. In stream mode, the SPI supports only writes. Configuration and other registers besides DAC_DATA_CHx_X registers do not support stream mode. Table 6-4 shows the clock cycle count, and DAC update rate achievable at the highest 66MHz SCLK frequency.

Table 6-4. SPI Stream Mode Update Rates, SCLK 66MHz

Data Register Field	Data Bytes	Standard SPI		Dual SPI		Quad SPI	
		SDR	DDR	SDR	DDR	SDR	DDR
CHx_DATA_HS	2	16 cycles 4.125MUPS	8 cycles 8.25MUPS	8 cycles 8.25MUPS	4 cycles 16.5MUPS	4 cycles 16.5MUPS	2 cycles 33MUPS
CHx_DATA_HR	3	24 cycles 2.75MUPS	12 cycles 5.5MUPS	12 cycles 5.5MUPS	6 cycles 11MUPS	6 cycles 11MUPS	3 cycles 22MUPS

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Use SPI_CFG.SS_EN to configure how the SPI stream data is distributed to the two channels in DAC90802. To use the stream mode, begin the SDI input with the R/W bit as 0b. Use the address of the DAC_DATA_CHx_X register for the channel to receive the first data word with this header, followed by subsequent data words while holding $\overline{CS}$ low. As shown in the examples below, finish the stream write at a word boundary corresponding to the configured data width of the registers, by bringing $\overline{CS}$ high.

SPI_CFG.SS_EN = 0 is default, and enables interleaving of alternate data packets between the corresponding data registers of the two channels. The two channels automatically receive alternate data packets starting with the address provided, and the next data packet for the corresponding address on the alternate channel. Use SPI_CFG.SS_EN = 1 to use the highest throughput mode for a single DAC. The stream mode write is identical to SPI_CFG.SS_EN = 0, except the device uses every sequential data packet for the channel of the address provided, and no data packet from the stream is received by the alternate device channel. Sequential data update examples using standard, dual, and quad-SPI in SDR, and DDR modes are as shown below.

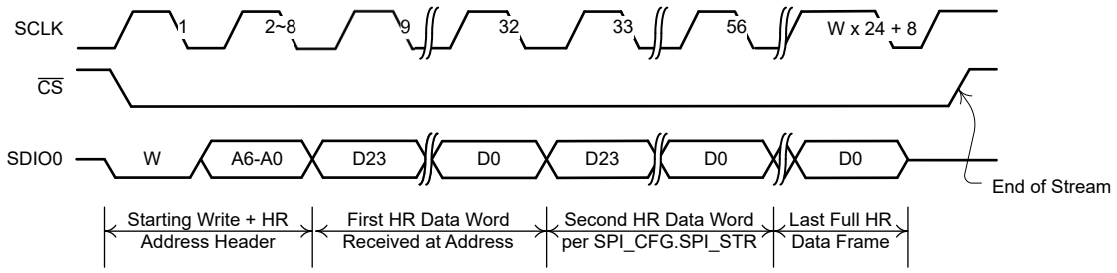

Figure 6-10. Standard SPI SDR Stream Mode for CHx_DATA_HR

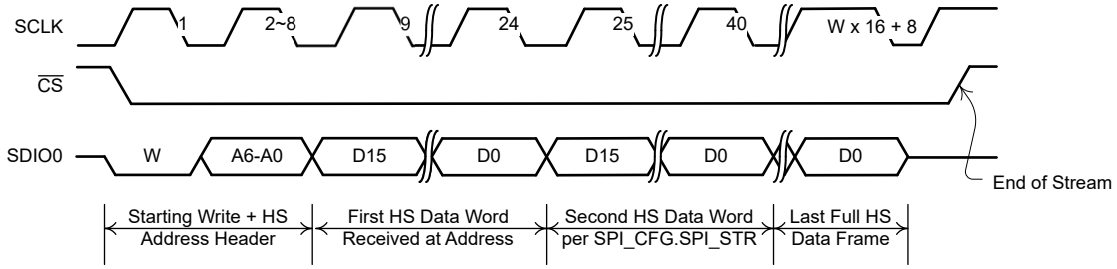

Figure 6-11. Standard SPI SDR Stream Mode for CHx_DATA_HS

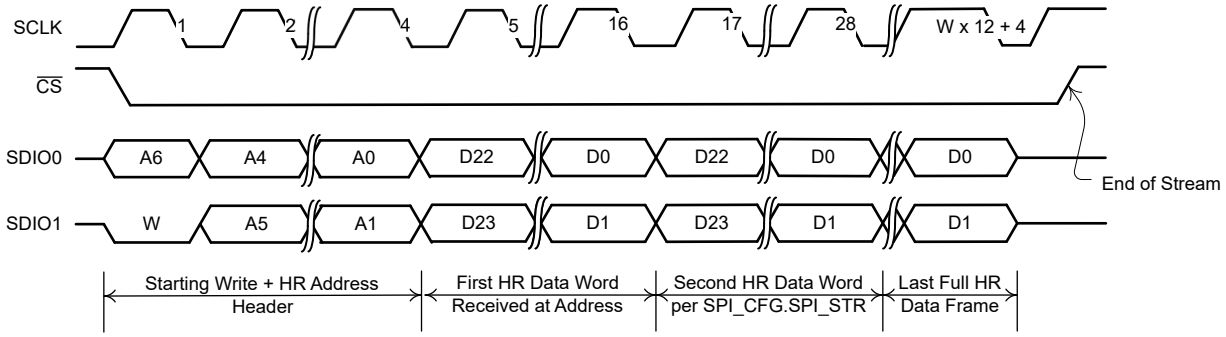

Figure 6-12. Dual SPI SDR Stream Mode for CHx_DATA_HR

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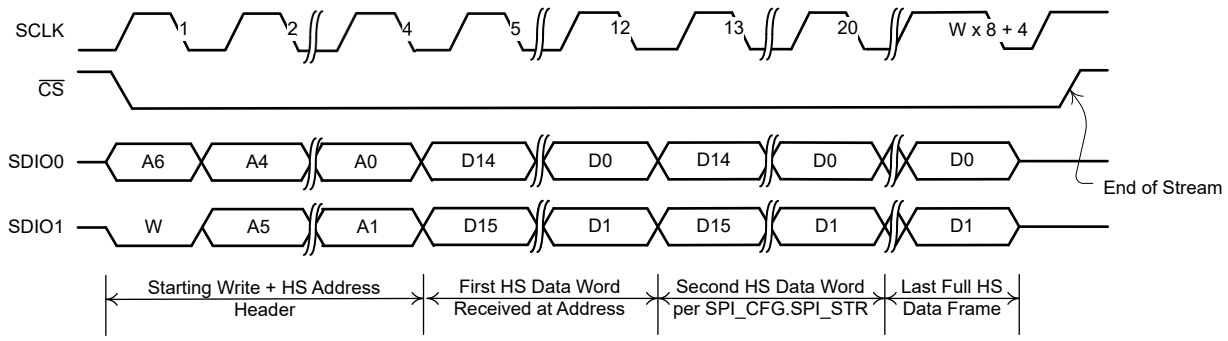

Figure 6-13. Dual SPI SDR Stream Mode for CHx_DATA_HS

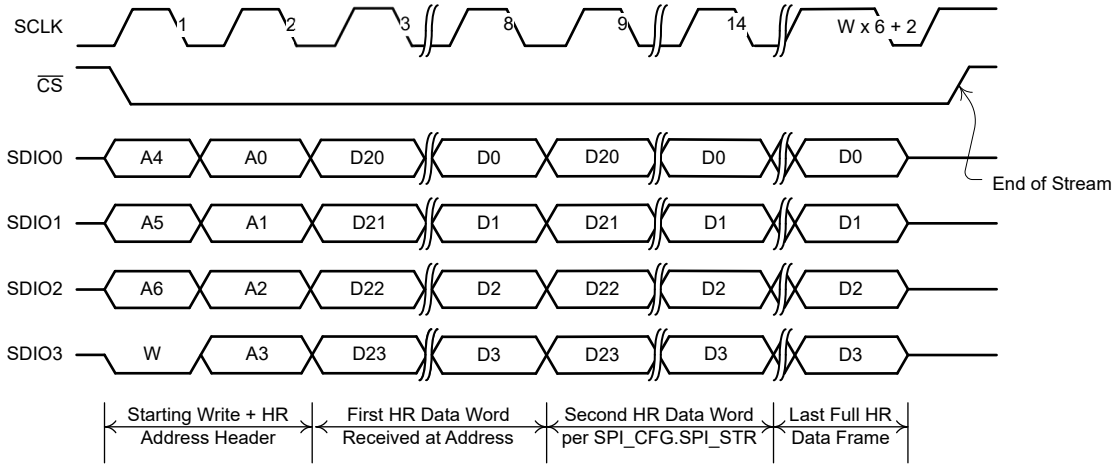

Figure 6-14. Quad SPI SDR Stream Mode for CHx_DATA_HR

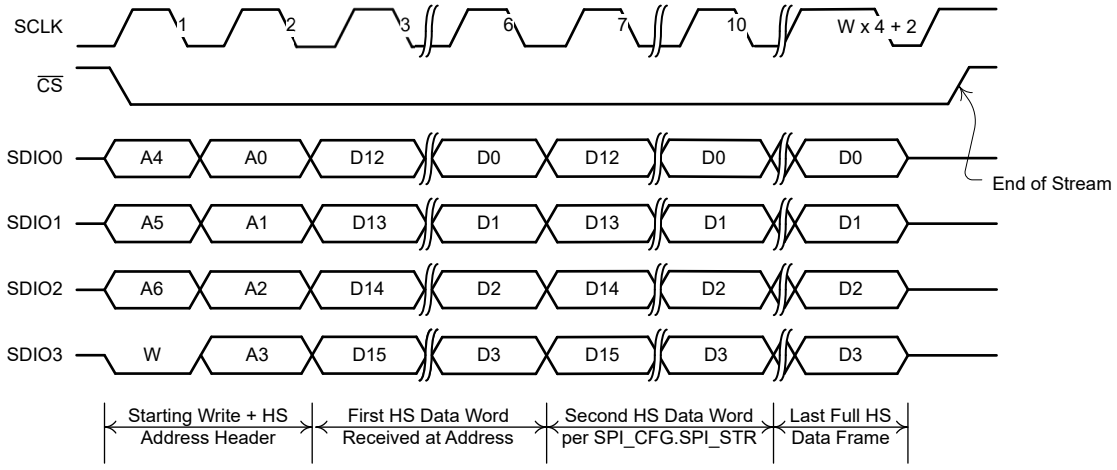

Figure 6-15. Quad SPI SDR Stream Mode for CHx_DATA_HS

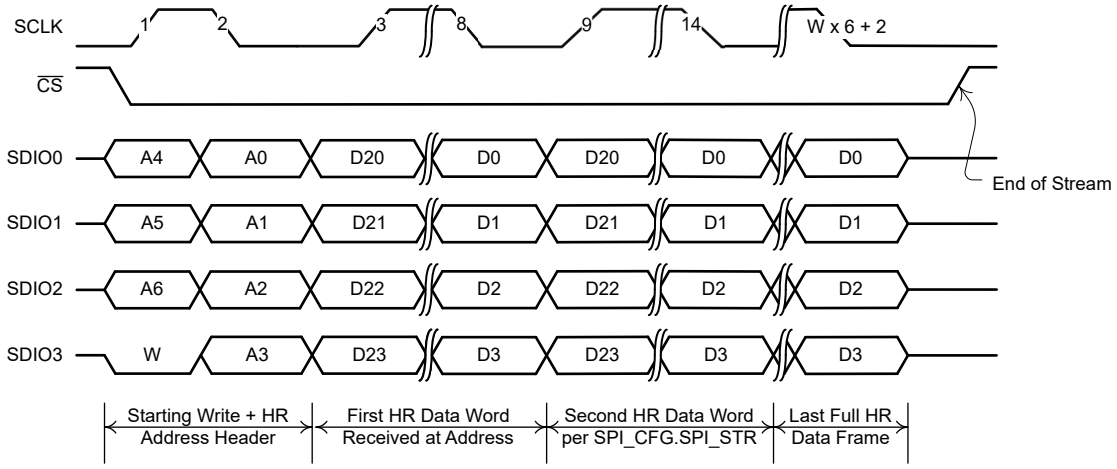

Figure 6-16. Quad SPI DDR Stream Mode for CHx_DATA_HR

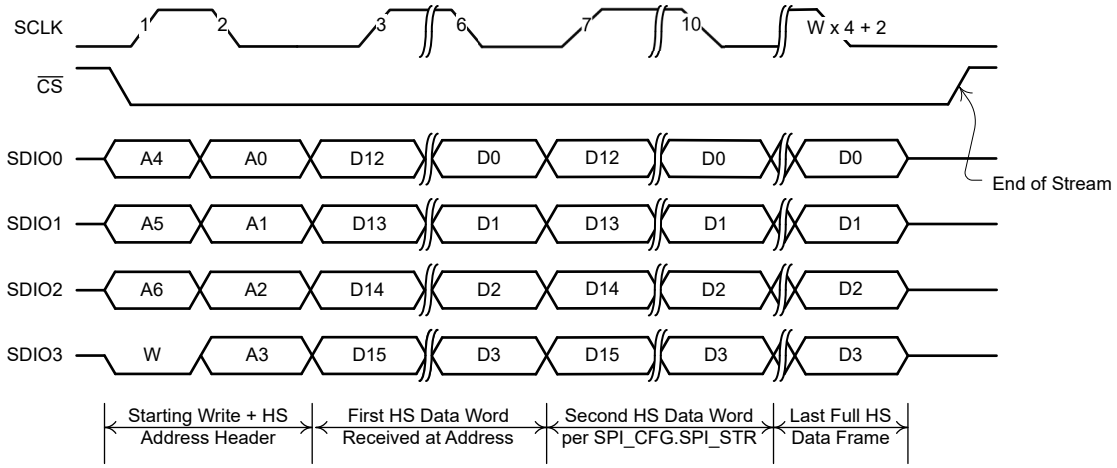

Figure 6-17. Quad SPI DDR Stream Mode for CHx_DATA_HS

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6.3.3.3 SPI Daisy Chain Mode

Use the daisy chain mode (SPI_CFG.SPI_DCH = 1) to minimize the number of SPI lines the system uses for multiple ICs or other peripherals. Figure 6-18 shows the connection of the daisy chain. Figure 6-19 shows the frame timing for the daisy-chain mode. Only the SDR mode is supported when daisy-chain mode is enabled. Dual-SPI is supported when the entire daisy chain supports dual-SPI. Figure 6-19 shows the timing sequence from SDI to SDO for the DAC in daisy-chain mode.

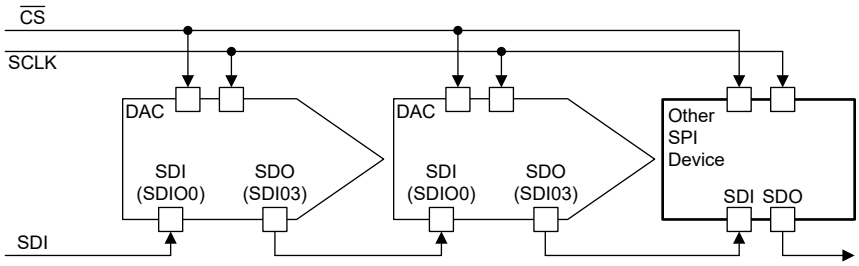

Figure 6-18. Daisy Chain Mode Connections

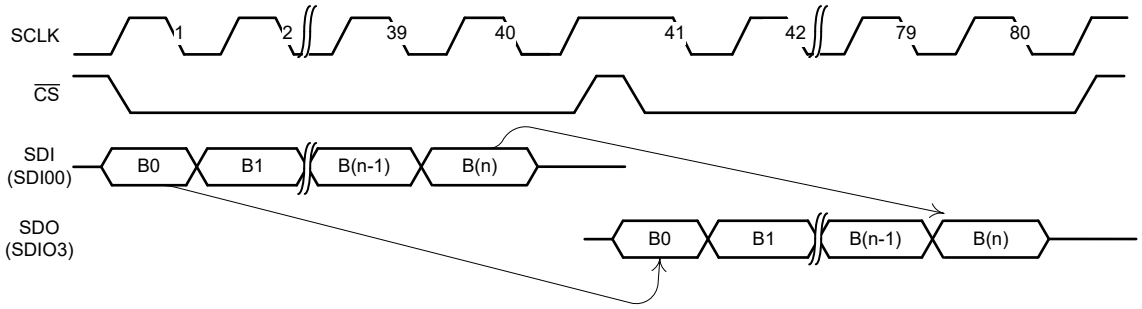

Figure 6-19. Daisy Chain Mode Timing

6.4 Device Functional Modes

The DAC90802 delivers optimized performance in three distinct use cases or modes. As shown in Table 6-5, the DAC_CONFIG_CHx bits in the DEVICE_CONFIG register configure these modes independently for each DAC channel.

Table 6-5. Operational Mode Configuration

DAC_CONFIG_CHx Setting	Operational Mode
00h	AWG mode
01h	Fast-settling mode
02h	Multiplying mode

Note

While the use of the incorrect configuration does not inhibit device functionality, best specified performance is only achieved with the appropriate configuration settings. For high precision applications that require calibration of the DAC to verify system performance, ascertain DAC calibration data independently per DAC_CONFIG_CHx selection.

6.4.1 AWG Mode

The arbitrary waveform generation (AWG) mode optimizes the DAC90802 as a signal source for waveform generation applications that need low-THD performance with a fixed dc reference. In this mode, use a high sampling ratio between the desired output signal frequency (f_{OUT}) and the DAC sampling frequency (f_s). For best performance, configure the DAC in bipolar mode.

6.4.2 Fast Settling Mode

The fast-settling (FS) mode optimizes the DAC for the best time domain response with a fixed dc reference. Use the FS mode for precision dc voltage generation and control loop applications. In the FS mode, the DAC90802 configures the analog signal chain for the best dc precision and fastest settling time. This mode optimizes both unipolar and bipolar operations.

6.4.3 Multiplying Mode

In the multiplying mode, the DAC90802 configures the signal chain to operate using an ac input reference with a fixed DAC code. The DAC code effectively *multiplies* the ac reference to attenuate the reference. Use the multiplying mode in the unipolar configuration of the DAC with REFPx terminal grounded. For the best performance, use this mode in conjunction with the reference-inversion resistors.

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7 Register Maps

7.1 COMMON Registers

Table 7-1 lists the memory-mapped registers for the COMMON registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. COMMON Registers

Address	Acronym	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
		Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	NOP	NOP							
		NOP							
		NOP							
		NOP							
0x01	DEVICE_CFG	DAC_CONFIG_CH1					DAC_CONFIG_CH0		
		DAC_CONFIG_CH0		VOSADJ_EN1	TEMP_SEL1		RESERVED	VOSADJ_EN0	TEMP_SEL0
		TEMP_SEL0	RESERVED		POL_CFG1	POL_CFG0	EN_CH1	EN_CH0	DEVICE_ID
		DEVICE_ID				VERSION_ID			
0x02	DEVICE_CTRL	RESERVED							
		RESERVED							
		RESERVED					SFT_LDAC	BOOT	BOOT_FAIL
		SFT_RST							
0x03	CH0_CFG	RESERVED							
		RESERVED							OFS_EN0
		RESERVED		RESERVED	ASYNC_UPDT_0	SFT_LDAC_EN0	GAIN_CH0		VREF_SQ0
		VREF_SQ0							
0x04	CH1_CFG	RESERVED							
		RESERVED							OFS_EN1
		RESERVED		RESERVED	ASYNC_UPDT_1	SFT_LDAC_EN1	GAIN_CH1		VREF_SQ1
		VREF_SQ1							
0x05	SPI_CFG	RESERVED							
		RESERVED							
		RESERVED							
		RESERVED	SPI_DCH	SPI_STR	FSDO_EN	SDO_EN	SPI_DDR	SPI_MIO	
0x08	ALERT_CFG	TSD_LVL1						TSD_LVL0	
		TSD_LVL0				RESERVED			
		RESERVED				TMPALRT_1	TMPALRT_0	TMPALRT_L1	TMPALRT_L0
		TMPALRT_CLR	TMPALRT_ACT			TMPALRT_MSK		TMPALRT_LAP	TMPALRT_ENP

Complex bit access types are encoded to fit into small table cells. Table 7-2 shows the codes that are used for access types in this section.

Table 7-2. COMMON Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WtoPH	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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7.1.1 NOP Register (Address = 0x00) [Reset = 0x00000000]

Return to the Summary Table.

Table 7-3. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	NOP	R/W	0x0	No-Operation. Read Only Register . 0x0 = Default Value

7.1.2 DEVICE_CFG Register (Address = 0x01) [Reset = 0x000000B3]

Return to the Summary Table.

Table 7-4. DEVICE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	DAC_CONFIG_CH1	R/W	0x0	DAC application mode selection for channel 1. Unlisted field values are RESERVED. 00h = AWG Mode 01h = Fast Settling Mode 02h = Multiplying Mode
26-22	DAC_CONFIG_CH0	R/W	0x0	DAC application mode selection for channel 0. Unlisted field values are RESERVED. 00h = AWG Mode 01h = Fast Settling Mode 02h = Multiplying Mode
21	VOSADJ_EN1	R/W	0x0	Enable the VOSADJ1 input for channel 1. 0x0 = VOSADJ input disabled. 0x1 = VOSADJ input enabled.
20-19	TEMP_SEL1	R/W	0x0	Temperature output TEMP1 output signal selection for channel 1. 0x0 = Temperature output disabled. 0x1 = Temperature output enabled in analog output mode. 0x2 = Temperature output enabled in TSD mode.
18	RESERVED	R	0x0	
17	VOSADJ_EN0	R/W	0x0	Enable the VOSADJ0 input for channel 0. 0x0 = VOSADJ input disabled. 0x1 = VOSADJ input enabled.
16-15	TEMP_SEL0	R/W	0x0	Temperature output TEMP0 output signal selection for channel 0. 0x0 = Temperature output disabled. 0x1 = Temperature output enabled in analog output mode. 0x2 = Temperature output enabled in TSD mode.
14-13	RESERVED	R	0x0	
12	POL_CFG1	R/W	0x0	Unipolar / Bipolar DAC configuration for channel 1. 0x0 = DAC unipolar configuration. 0x1 = DAC bipolar configuration.
11	POL_CFG0	R/W	0x0	Unipolar / Bipolar DAC configuration for channel 0. 0x0 = DAC unipolar configuration. 0x1 = DAC bipolar configuration.
10	EN_CH1	R/WtoPH	0x0	Channel enable (power up) control for channel 1. 0x0 = Channel disable (power down) 0x1 = Channel enable (power up). This bit self-resets in case of an alert.
9	EN_CH0	R/WtoPH	0x0	Channel enable (power up) control for channel 0. 0x0 = Channel disable (power down) 0x1 = Channel enable (power up). This bit self-resets in case of an alert.
8-4	DEVICE_ID	R	0xB	Device Identifier (Read Only)
3-0	VERSION_ID	R	0x3	Version Identifier (Read Only)

7.1.3 DEVICE_CTRL Register (Address = 0x02) [Reset = 0x00000000]

Return to the Summary Table.

Table 7-5. DEVICE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0x0	
30-11	RESERVED	R	0x0	
10	SFT_LDAC	R/WtoPH	0x0	Software controlled LDAC signal. Simultaneously asserts LDAC for both channels. Channel and SFT_LDAC_EN for the channel must both be enabled to receive the LDAC assertion. 0x0 = Assert LDAC. This bit is self-resetting.

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Table 7-5. DEVICE_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	BOOT	R	0x0	Bit to indicate device bootup in progress after POR. (Read Only) 0x0 = Device not in boot sequence 0x1 = Device executing boot sequence
8	BOOT_FAIL	R	0x0	Read only signal indicating the device bootup has failed and there's issue with the OTP. 0x0 = Device passed boot up sequence 0x1 = Device passed boot up sequence
7-0	SFT_RST	R/W	0x0	Code for software controlled reset signal . Equivalent to asserting the hardware $\overline{\text{RESET}}$. 0xAA = Reset asserted

7.1.4 CH0_CFG Register (Address = 0x03) [Reset = 0x00000219]

Return to the Summary Table.

Table 7-6. CH0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0x0	
29	RESERVED	R	0x0	
28-26	RESERVED	R	0x0	
25-22	RESERVED	R	0x0	
21-17	RESERVED	R	0x0	
16	OFS_EN0	R/W	0x0	Enable ROFS for channel-0. This is used to give an asymmetric push to the output depending on the voltage applied on the ROFS pin
15-14	RESERVED	R	0x0	
13	RESERVED	R	0x0	
12	ASYNC_UPDT_0	R/W	0x0	Sets the DAC0 register update mode 0x0 = asynchronous update mode 0x1 = synchronous update mode
11	SFT_LDAC_EN0	R/W	0x0	Enabling soft ldac for channel0
10-9	GAIN_CH0	R/W	0x1	Channel 0 Voltage Gain Selection 0x0 = Gain 1 × 0x1 = Gain 4 × 0x2 = Gain 2 ×
8-0	VREF_SQ0	R/W	0x19	(Gain * Voltage Reference)^2 has to be set in this Reg

7.1.5 CH1_CFG Register (Address = 0x04) [Reset = 0x00000219]

Return to the Summary Table.

Table 7-7. CH1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0x0	
29	RESERVED	R	0x0	
28-26	RESERVED	R	0x0	
25-22	RESERVED	R	0x0	
21-17	RESERVED	R	0x0	
16	OFS_EN1	R/W	0x0	Enable ROFS for channel-1. This is used to give an asymmetric push to the output depending on the voltage applied on the ROFS pin
15-14	RESERVED	R	0x0	
13	RESERVED	R	0x0	
12	ASYNC_UPDT_1	R/W	0x0	Sets the DAC0 register update mode 0x0 = asynchronous update mode 0x1 = synchronous update mode
11	SFT_LDAC_EN1	R/W	0x0	Enabling soft ldac for channel0
10-9	GAIN_CH1	R/W	0x1	Channel 1 Voltage Gain Selection 0x0 = Gain 1 × 0x1 = Gain 4 × 0x2 = Gain 2 ×
8-0	VREF_SQ1	R/W	0x19	(Gain × Voltage Reference)^2 has to be set in this register

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7.1.6 SPI_CFG Register (Address = 0x05) [Reset = 0x00000000]

Return to the Summary Table.

Table 7-8. SPI_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0x0	
30-7	RESERVED	R	0x0	
6	SPI_DCH	R/W	0x0	SPI Daisy Chain mode enable / disable bit. 0x0 = Daisy Chain Mode Disabled 0x1 = Daisy Chain Mode Enabled
5	SPI_STR	R/W	0x0	Stream Mode configurations 0x0 = Dual Channel Stream Enabled 0x1 = Single Channel Stream Enabled
4	FSDO_EN	R/W	0x0	SDO latching control 0x0 = No Latch at the SDO port 0x1 = Output will be Latched
3	SDO_EN	R/W	0x0	SDO Enable Control 0x0 = SDO ports get disabled 0x1 = SDO ports enabled
2	SPI_DDR	R/W	0x0	DDR Mode Enable 0x0 = SDR Mode (Single Data Rate) 0x1 = DDR Mode (Double Data Rate)
1-0	SPI_MIO	R/W	0x0	SPI IO Modes Control 0x0 = Standard SPI 0x1 = Dual SPI 0x2 = Quad SPI 0x3 = Reserved

7.1.7 ALERT_CFG Register (Address = 0x08) [Reset = 0xEFB0001E]

Return to the Summary Table.

Table 7-9. ALERT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	TSD_LVL1	R/W	0x3B	Code for Temp Shut Down Threshold (Reset Value : 6x3B : 140°C) 0x0 = 30°C 0x3F = 150°C
25-20	TSD_LVL0	R/W	0x3B	Code for Temp Shut Down Threshold (Reset Value : 6x3B : 140°C) 0x0 = 30°C 0x3F = 150°C
19-18	RESERVED	R	0x0	
17-16	RESERVED	R	0x0	
15-12	RESERVED	R	0x0	
11	TMPALRT_1	R	0x0	Read Only Signal indicating the Non-Latched Temp Alert
10	TMPALRT_0	R	0x0	Read Only Signal indicating the Non-Latched Temp Alert
9	TMPALRT_L1	R	0x0	Read Only Signal indicating the Latched Temp Alert
8	TMPALRT_L0	R	0x0	Read Only Signal indicating the Latched Temp Alert
7	TMPALRT_CLR	R/WtoPH	0x0	Latched temperature alerts clear command 0x0 = No action 0x1 = Latched temperature alert clear. This bit is self-resetting.
6-4	TMPALRT_ACT	R/W	0x1	Response to temperature alert being asserted. Unlisted field values are RESERVED 0x0 = No action. 0x1 = Shut-down asserting channel only when alert is asserted. No power up allowed until latched synchronous alert goes low 0x2 = Shut-down asserting channel only with alert is asserted. Power up is allowed anytime after assertion. 0x5 = Shut down all channels when alert is asserted onnay channel. No power up allowed until latched synchronous alert goes low. 0x6 = Shut down all channelswhen alert is asserted onnay channel. Power up is allowed anytime after assertion.
3-2	TMPALRT_MSK	R/W	0x3	Temperature alert masking on TEMP Pin. 0x0 = Alerts are masked (On TEMP Pin) 0x3 = (dafault) alerts are un masked (On TEMP Pin) Unlisted bits are reserved
1	TMPALRT_LAP	R/W	0x1	Latched temperature alerts on TEMP pin 0x0 = Disable 0x1 = Enable

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Table 7-9. ALERT_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TMPALRT_ENP	R/W	0x0	Temperature alerts on TEMP pin (non-latched) 0x0 = Disable 0x1 = Enable

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7.2 HS_DATA Registers

Table 7-10 lists the memory-mapped registers for the HS_DATA registers. All register offset addresses not listed in Table 7-10 should be considered as reserved locations and the register contents should not be modified.

Table 7-10. HS_DATA Registers

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x60	CH0_DATA_HS	CH0_DATA_HS							
		CH0_DATA_HS							
0x61	CH1_DATA_HS	CH1_DATA_HS							
		CH1_DATA_HS							

Complex bit access types are encoded to fit into small table cells. Table 7-11 shows the codes that are used for access types in this section.

Table 7-11. HS_DATA Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.2.1 CH0_DATA_HS Register (Address = 0x60) [Reset = 0x0000]

Return to the Summary Table.

Table 7-12. CH0_DATA_HS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CH0_DATA_HS	R/W	0x0	High speed DAC data register for channel 0. Data word is 16-b wide, MSB aligned, QSPI input with optional stream mode support.

7.2.2 CH1_DATA_HS Register (Address = 0x61) [Reset = 0x0000]

Return to the Summary Table.

Table 7-13. CH1_DATA_HS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CH1_DATA_HS	R/W	0x0	High speed DAC data register for channel 1. Data word is 16-b wide, MSB aligned, QSPI input with optional stream mode support.

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7.3 HR_DATA Registers

Table 7-14 lists the memory-mapped registers for the HR_DATA registers. All register offset addresses not listed in Table 7-14 should be considered as reserved locations and the register contents should not be modified.

Table 7-14. HR_DATA Registers

Address	Acronym	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x64	CH0_DATA_HR	CH0_DATA_HR							
		CH0_DATA_HR							
		CH0_DATA_HR							
0x65	CH1_DATA_HR	CH1_DATA_HR							
		CH1_DATA_HR							
		CH1_DATA_HR							

Complex bit access types are encoded to fit into small table cells. Table 7-15 shows the codes that are used for access types in this section.

Table 7-15. HR_DATA Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.3.1 CH0_DATA_HR Register (Address = 0x64) [Reset = 0x000000]

Return to the Summary Table.

Table 7-16. CH0_DATA_HR Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CH0_DATA_HR	R/W	0x0	High speed DAC data register for channel 0. Data word is 18-b wide, MSB aligned, QSPI input with optional stream mode support.

7.3.2 CH1_DATA_HR Register (Address = 0x65) [Reset = 0x000000]

Return to the Summary Table.

Table 7-17. CH1_DATA_HR Register Field Descriptions

Bit	Field	Type	Reset	Description
23-0	CH1_DATA_HR	R/W	0x0	High speed DAC data register for channel 1. Data word is 18-b wide, MSB aligned, QSPI input with optional stream mode support.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application

DAC90802 is optimized for applications that demand high DC accuracy and precision, ultra-low glitch energy and output noise with advanced waveform generation capability. Typical applications include high-performance source-measure units (SMUs), ultra-low-THD arbitrary waveform generators (AWGs), closed-loop control systems such as MEMS actuators, linear and precision motor drives, electrostatic-lens control in advanced microscopy, quadruple mass-spectrometry, and other demanding instrumentation.

8.2 Design Requirements

8.2.1 Reference Signal Chain Information

8.2.1.1 DC Reference

The DAC90802 references remain nominally constant throughout AWG mode and fast settling mode operation. For improved THD performance in AWG mode, a 2-wire connection with a dedicated low-impedance driver amplifier for each signal is recommended. This minimizes dynamic reference loading while changing DAC codes. If a 2-wire design is not used (for example, when sharing references across channels), short the _Fx and _Sx pins. The following two reference generation methods are recommended for these application cases:

- DC Reference Signal Chain Using Internal Inversion: This configuration utilizes internal temperature-coefficient (temp-co) matched resistors (R_1 and R_2, see Section 5.5) to generate the negative reference using an external operational amplifier as Figure 8-1 shows

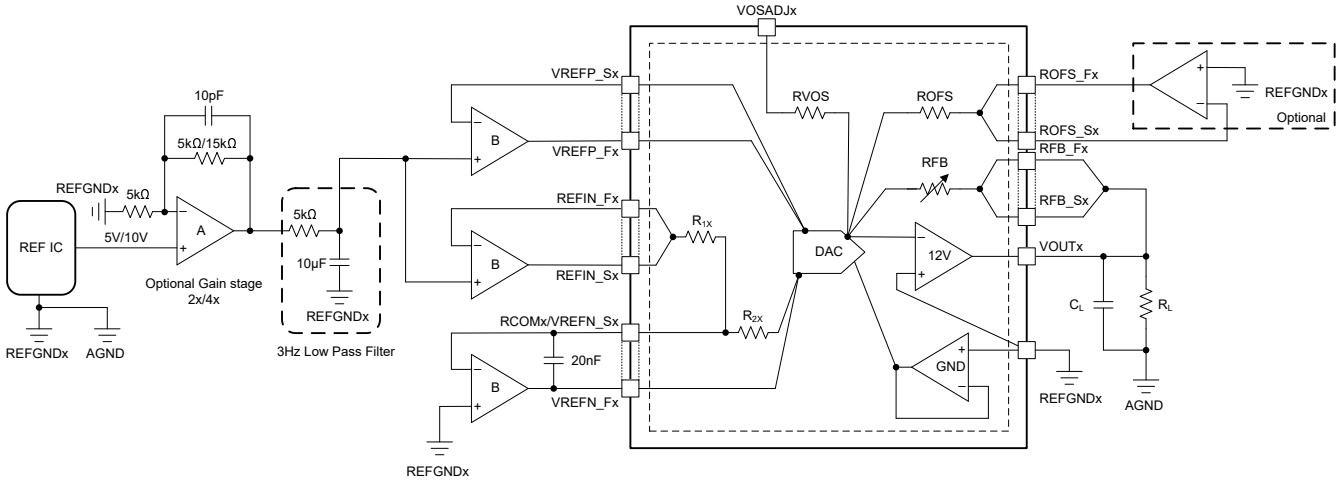

Figure 8-1. DC Reference Signal Chain Using Internal Inversion

- DC Reference Signal Chain Using External inversion: This method is recommended when internal resistor temperature-coefficient matching is insufficient for reference inversion, when a stable negative reference voltage is available at the system-level, or when the reference is shared between multiple channels as Figure 8-2 shows

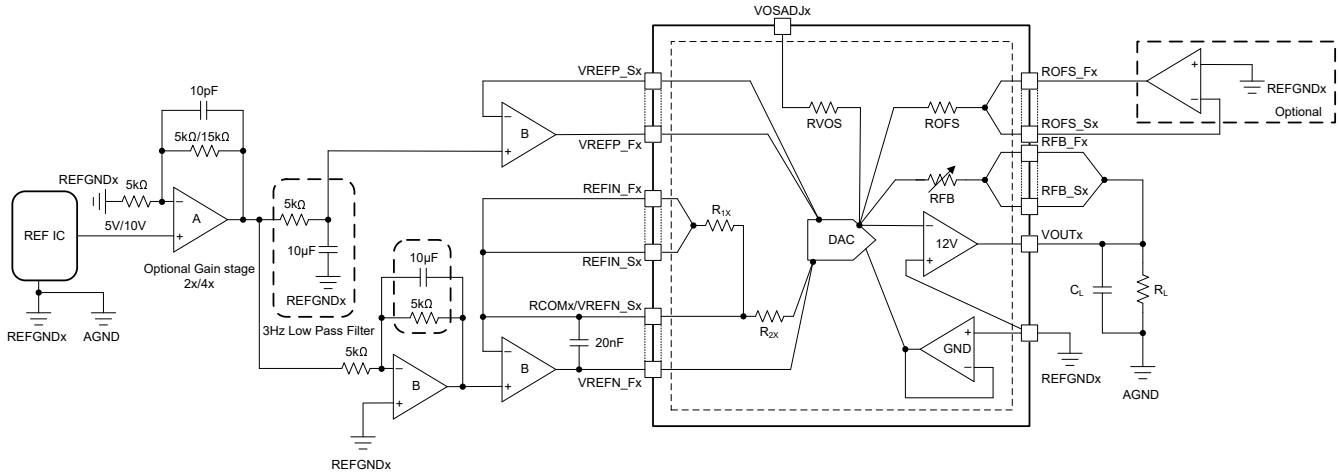

Figure 8-2. DC Reference Signal Chain Using External Inversion

Use a gain stage following the voltage reference to achieve high reference voltages (≥10V). To reduce signal chain noise, use an additional (3Hz shown) low-pass filter before the DAC reference buffers. To maximize the performance of the DAC90802, the selection of the reference IC and reference buffers must consider the following aspects:

- Reference IC selection:
  - Output Voltage Accuracy (initial tolerance): Output voltage inaccuracy results in absolute gain error; therefore, select ICs with appropriate initial output voltage accuracy, and tolerance according to application requirements
  - Output Voltage Temperature Coefficient: Output voltage temperature coefficient affects DAC accuracy and precision (End-point errors, INL, and DNL) across temperature. The equation below gives a good estimate of the temperature coefficient requirement of the reference device corresponding to the DAC resolution. Output of the reference IC for a ΔT change in temperature shown in Equation 4. For N-bit DAC to keep the change below 1LSB shown in Equation 5.

$$\mathrm{VREF} = \mathrm{VREF_{initial}}\left(1 + \left(\mathrm{Temp_{co}}\right) \times \Delta\mathrm{T} \times 10^{-6}\right)\left(\mathrm{Temp_{co}\ in\ ppm/C}\right) \tag{4}$$

$$\Delta\mathrm{VREF} = \left(\mathrm{VREF_{initial}} \times \mathrm{Temp_{co}} \times \Delta\mathrm{T} \times 10^{-6}\right) < \left(1\mathrm{LSB} = \frac{\mathrm{VREF_{initial}}}{2^{\mathrm{N}}}\right) \tag{5}$$

$$\mathrm{Temp_{co}} < \frac{10^{6}}{2^{\mathrm{N}} \times \Delta\mathrm{T}}\left(\mathrm{About\ 0.76\,ppm/C\ for\ a\ 5°C\ \Delta T\ at\ 18\ bit\ precision}\right) \tag{6}$$

  - Output Noise: For high precision applications, reference output voltage noise becomes a critical source of system noise
    - Flicker Noise: Flicker noise is defined as the integrated 0.1Hz to 10Hz noise in the time-domain (V_{PP}). This primarily affects the dc output characteristics such as INL, DNL and end-point errors. For best performance, the flicker noise level must be well below 1LSB; for an 18-bit DAC and ±5V reference, this translates to a target of < 3.8µV_{PP} (0.1LSB)
    - Thermal/Broadband Noise: Thermal noise predominantly affects AC performance, serving as the primary noise source for SNR and THD+N measurements. Since the dc reference signal chain remains static during operation, a single-order low-pass filter is sufficient to mitigate reference device thermal noise. Figure 8-1 and Figure 8-2 indicate a 3Hz low-pass filter for this purpose. When selecting the capacitor for this filter, a polypropylene film capacitor is highly recommended.
- Operational Amplifier Selection: The following specifications are critical when selecting operational amplifiers for the proposed reference signal chains (Figure 8-1 and Figure 8-2):

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- Voltage noise
- Current noise
- Voltage offset
- Bias current offset
- Output impedance

The impact of these characteristics at each stage of the signal chain is described below:

- Amp (A): Op-amp (A) acts as the gain stage to generate high voltage reference inputs (up to 21V) for DAC90802 using low-voltage reference ICs
  - Voltage Noise and Offset: The gain configuration of the op amp directly translates the input-referred noise and offset to the output. A low-pass filter placed after this stage helps eliminate thermal noise, leaving flicker noise as the critical specification for op amp selection.
  - Bias Current: The bias current noise, and offset translate to the output voltage noise and offset through the op amp's feedback resistor
- Amp (B): Op-amps (B) serve as the DAC reference buffers and require low output impedance across the operating frequency
  - Voltage Noise and Offset: The op amp's voltage noise and offset translate directly to the DAC's output noise and offset
  - Bias Current Noise and Offset: The noise and offset from the bias current translate to the DAC's output voltage noise and offset through the first-order low-pass filter (comprising the resistor and capacitor) in the signal chain. Additionally, place a capacitor between the VREFN_F and VREFN_S pins of a channel to filter the thermal noise generated by inversion resistor

Table 8-1, Table 8-2 and Table 8-3 provide recommendations for voltage-reference devices, op amp, and signal-chain configuration, respectively.

As an example, select OPA189 as AMP (A), followed by OPA828 as AMP (B). OPA189 provides low offset voltage and low flicker noise, making the gain stage appropriate. The subsequent low-pass filter helps minimize low thermal-noise contribution, while OPA828 is selected as AMP (B) to provide low-noise signal buffering and drive capability.

Table 8-1. Voltage Reference Device Recommendation

REF IC	V_{REF}(V)	Thermal Noise (nV/$\sqrt{Hz}$)	Flicker Noise (μV_{PP})	Initial Tolerance (%)	Temp Drift (ppm/°C)
REF54(C_{NR}: 1µF)	5	5	1.2	±0.02	0.8
REF70	5	20	1.15	±0.025	2
REF81	10	60	1.2	±0.1	0.1

Table 8-2. Operational Amplifier Recommendation

OP-AMP	Offset (µV)	Bias Current (pA)	Voltage Thermal Noise (nV/$\sqrt{Hz}$)	Flicker Noise (μV_{PP})	Current Thermal Noise(pA/$\sqrt{Hz}$))
OPA828	±50	±1	4	0.34	0.0012
OPA189	±0.4	±70	5.2	0.1	0.165
OPA182	±0.45	±50	5.7	0.119	0.165
OPA1611	±100	±60000	1.1	0.1	1.7

Table 8-3. Signal Chain Recommendation

REF IC	GAIN	AMP (A)	AMP (B)	V_{REF}(V)	ESTIMATED VREF_Px/ VREF_Nx THERMAL NOISE (nV/$\sqrt{Hz}$	ESTIMATED VREF_Px/ VREF_Nx FLICKER NOISE (0.1Hz TO 10Hz) (μV_{PP})
REF54 (C_{NR}:1µF)	1 ×	OPA189	OPA828	5	4.33	1.25
REF54 (C_{NR}:1µF)	2 ×	OPA189	OPA828	10	4.33	2.5
REF54 (C_{NR}:1µF)	4 ×	OPA189	OPA828	20	4.33	5

Table 8-3. Signal Chain Recommendation (continued)

REF IC	GAIN	AMP (A)	AMP (B)	V_{REF}(V)	ESTIMATED VREF_Px/ VREF_Nx THERMAL NOISE (nV/√Hz	ESTIMATED VREF_Px/ VREF_Nx FLICKER NOISE (0.1Hz TO 10Hz) (μV_{PP})
REF70	1 ×	OPA189	OPA828	5	4.33	1.18
REF70	2 ×	OPA189	OPA828	10	4.33	2.36
REF70	4 ×	OPA189	OPA828	20	4.33	4.72
REF81	1 ×	OPA189	OPA828	10	4.33	1.7
REF81	2 ×	OPA189	OPA828	20	4.33	3.36

8.2.1.2 AC Reference

The DAC90802 architecture enables time-varying reference input (AC reference) in Multiplying Mode. Electrical parameters of importance in this mode are Multiplying Bandwidth, Multiplying THD and Multiplying Feedthrough. The device supports two reference-input configurations in this mode:

- REFIN Configuration: REFIN configuration is recommended to achieve the best multiplying mode performance and utilizes the internal temperature-coefficient-matched resistors of DAC90802 (refer to inversion-resistor-ratio-mismatch drift from Section 5.5). This method preserves the phase of the scaled signal and requires VREFP_Sx and VREFP_Fx to be connected to a quiet analog ground, as illustrated in Figure 8-3.

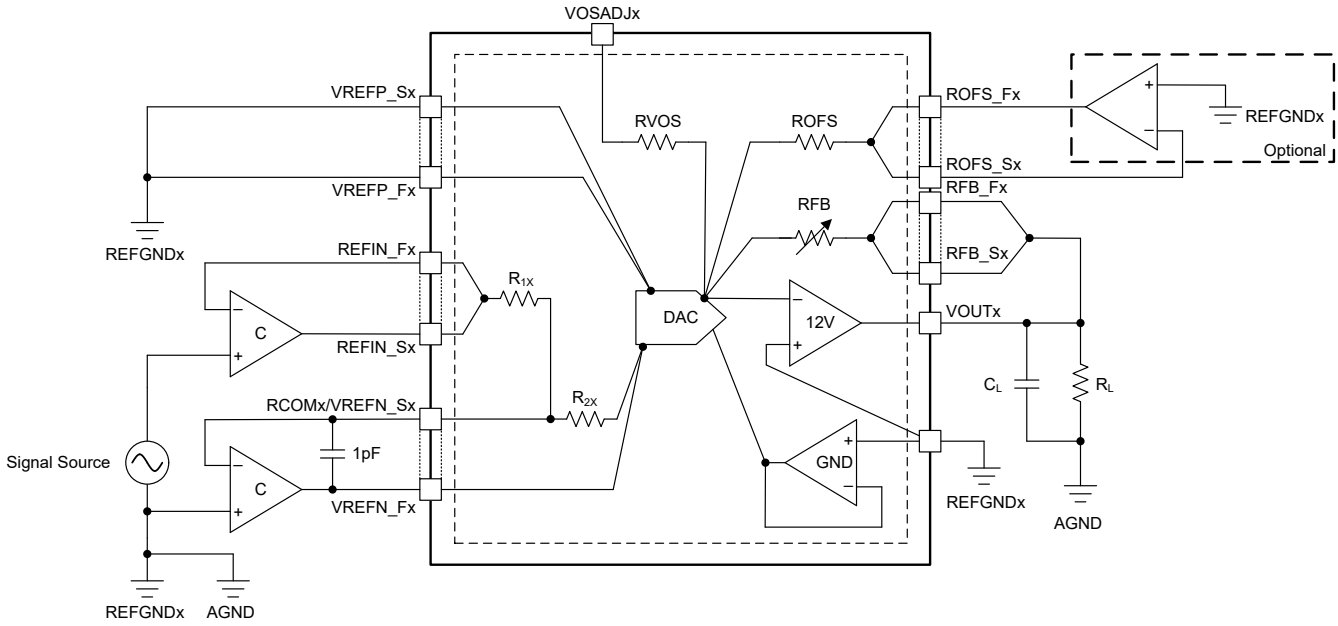

Figure 8-3. AC Reference Signal Chain Using Internal Inversion

- REFN Configuration (Direct Reference): In REFN configuration, VREFP_Sx and VREFP_Fx are connected to a quiet analog ground (see Figure 8-4). This method provides the most compact implementation and results in a phase inversion at the output.

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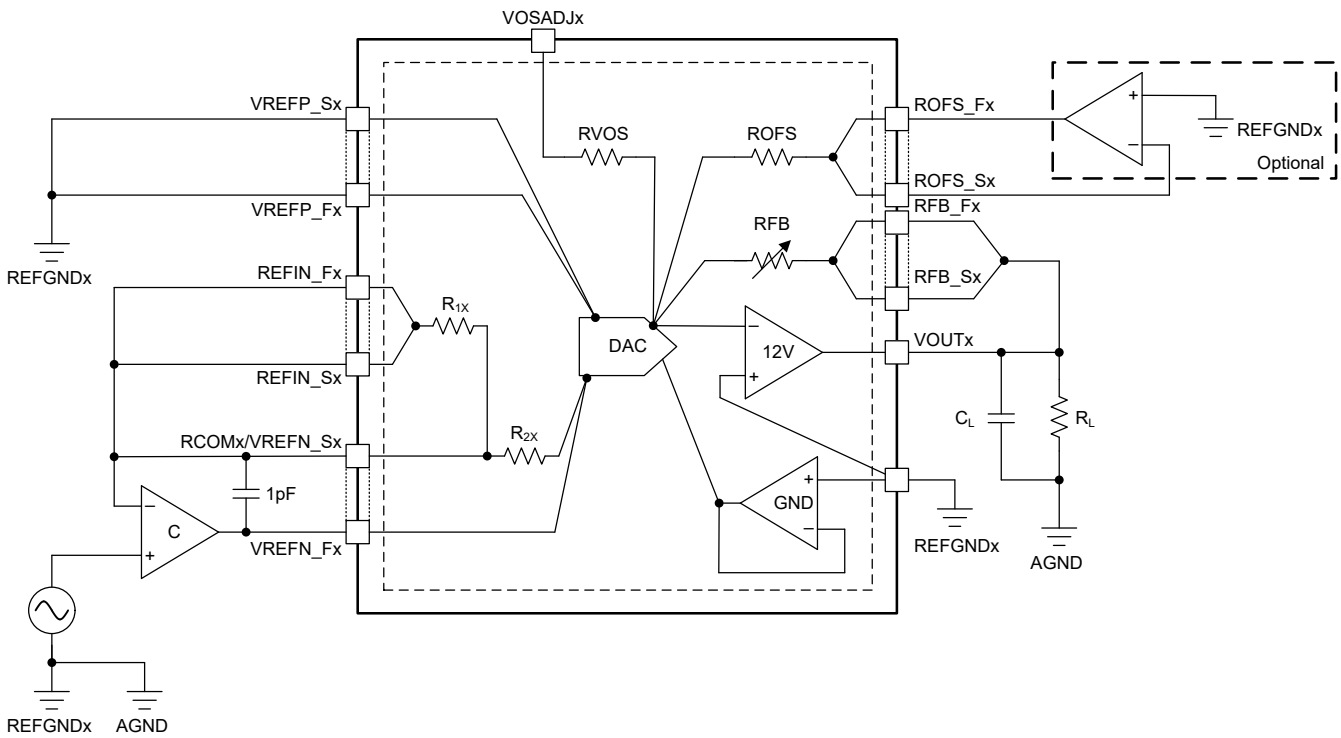

Figure 8-4. AC Reference Signal Chain Using External Inversion

Depending on the application, the reference buffer must be chosen appropriately to achieve best device performance:

- Multiplying bandwidth Requirement: The amplifier (C) must exhibit sufficient bandwidth and slew rate to accommodate the reference voltage swing.
- THD measurements: The amplifier (C) must provide ultra-low THD at the reference voltage and frequency range of interest.

Recommended operational amplifier selections for multiplying mode are listed in Table 8-4.

Table 8-4. Operational Amplifiers Recommendation for Multiplying Mode

OP-AMP	GAIN-BANDWIDTH (MHz)	SLEW RATE (V/µs)	THD (dB) at 100kHz	DESCRIPTION
TH4631	210	550	< –90	THS4631 provides the best bandwidth across output swing to large slew rate
OPA891	180	105	< –119	OPA891 provides the best THD across frequency while supporting respectable bandwidth across output swing

8.2.2 Optimising the Self-Heating Trim to Achieve Lowest THD Across Frequencies for High Voltage Swing

At high output voltage swings (>15V_{PP}) and high output frequencies, the third harmonic distortion (HD3) of the DAC90802 can be sub-optimal. To mitigate this, the DAC90802 provides a correction mechanism through the CHx_CFG registers By adjusting the 9-bit VREF_SQx field (values ranging from 0 to 511), users can optimize harmonic performance.

The recommended value for VREF_SQx is calculated using the following equation:

$$\mathrm{VREF_SQ_x} = \mathrm{Amp}^2 \times \left(\frac{\mathrm{b}}{1 + \mathrm{a} \times \mathrm{freq}} + \mathrm{c}\right) \tag{7}$$

where

- Amp is the amplitude of the output signal (in V_{Pk}).
- freq = Frequency in Hz
- a = 1.1×10^{-4}, b = 0.85, c = 0.15

Figure 8-5 illustrates the relationship between the normalized vref sq value and frequency (kHz). The normalized vref sq value is defined by the following relationship:

- Normalized Vref Sq Value = Programmed VREF_SQx / Amp^2

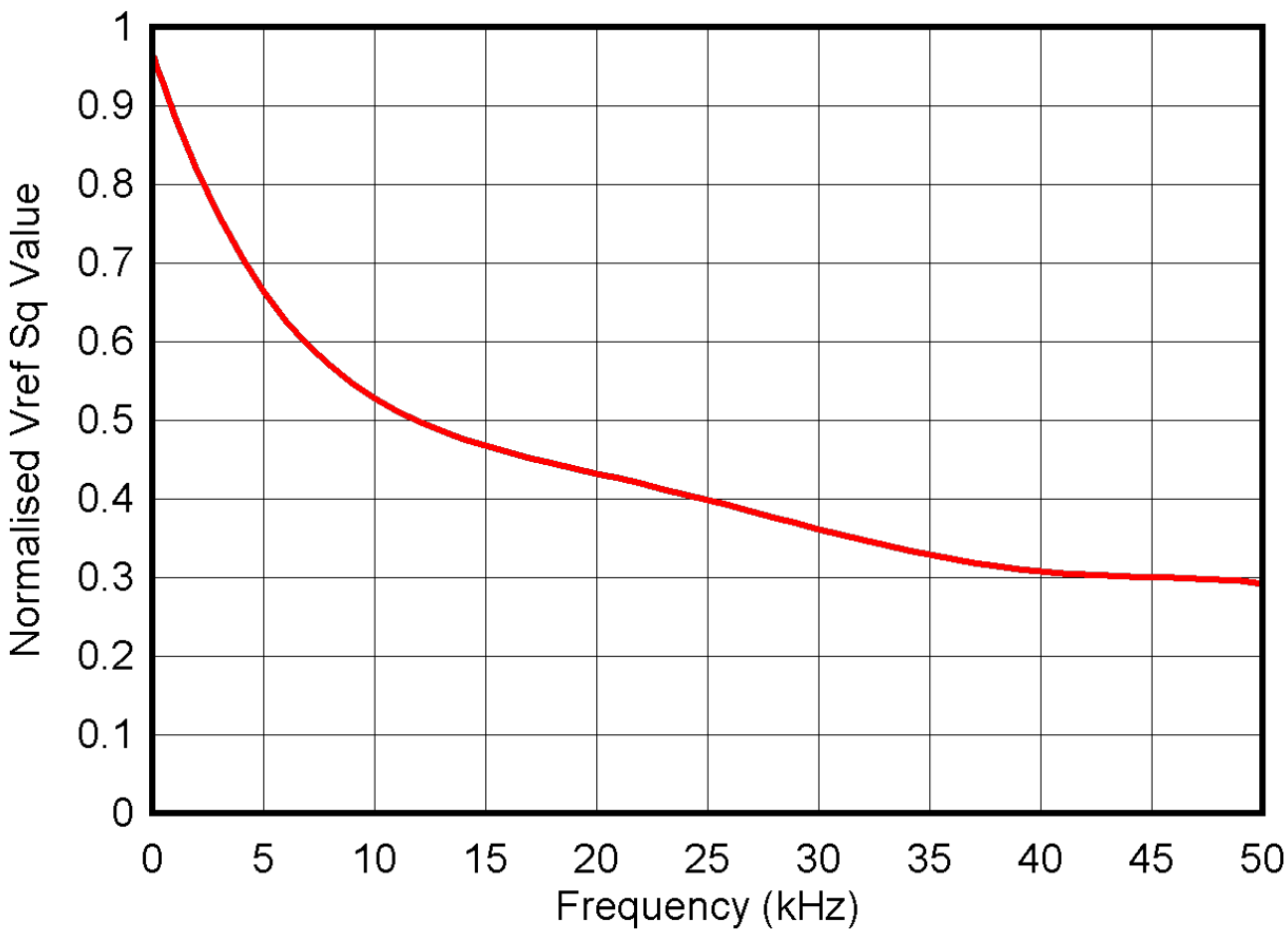

Figure 8-5. Optimised Normalized Vref Sq Value vs Frequency(kHz)

8.2.3 Digital Interface

The DAC90802 works with a four-wire (extendable to six-wire) SPI. The digital interface of the device can be an FPGA or processor, as shown in Section 8.2.3. The DAC90802 has two $\overline{\text{LDAC}}$ input options for synchronous output update for each channel. In ac-signal-generation applications, the jitter in the $\overline{\text{LDAC}}$ signal contributes to the signal-to-noise ratio (SNR) at the output. Therefore, the $\overline{\text{LDAC}}$ signals must be generated from a low-jitter clock source in the FPGA or processor. All active-low signals ($\overline{\text{LDAC}}$, $\overline{\text{RESET}}$, $\overline{\text{CS}}$) can be pulled up to VIO using appropriate resistors. When operating at high SCLK frequencies, use appropriate termination resistors(optional), as shown in Figure 8-6. Digital signals which are unused can be tied to either VIO or to the ground.

Phase noise on $\overline{\text{LDAC}}$ can degrade DAC output noise, especially at higher output frequencies. A stable (better than ±50ppm frequency stable), low random jitter (≤ 3.0ps) clocks (like TI's CDC6C) are recommended.

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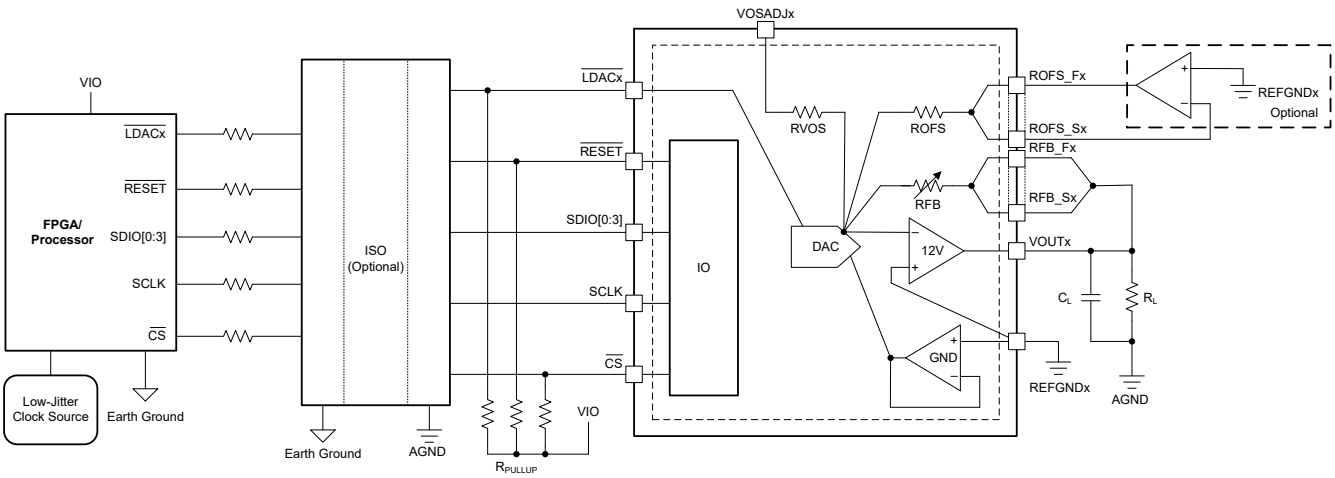

Figure 8-6. DAC90802 Interfacing to FPGA or Processor

8.2.4 Grounding Recommendations

To achieve the best performance from the DAC90802, careful grounding and decoupling are essential. Using a PCB with a ground-plane reference helps confine digital return currents effectively. By creating a low mutual inductance path directly beneath high-frequency digital traces, return currents follow the signal paths, which minimizes crosstalk. In precision applications, managing the ground plane is critical to limiting common-impedance coupling, as dc signals tend to spread across the plane rather than staying confined under specific traces.

Effective isolation between REFGND and AGND is also necessary to prevent common-mode current flow between the grounds. While these grounds must remain isolated from current flow, maintain the same DC potential across grounds. The most reliable method for achieving this is through a single-point connection located near the reference device as Figure 8-7 shows.

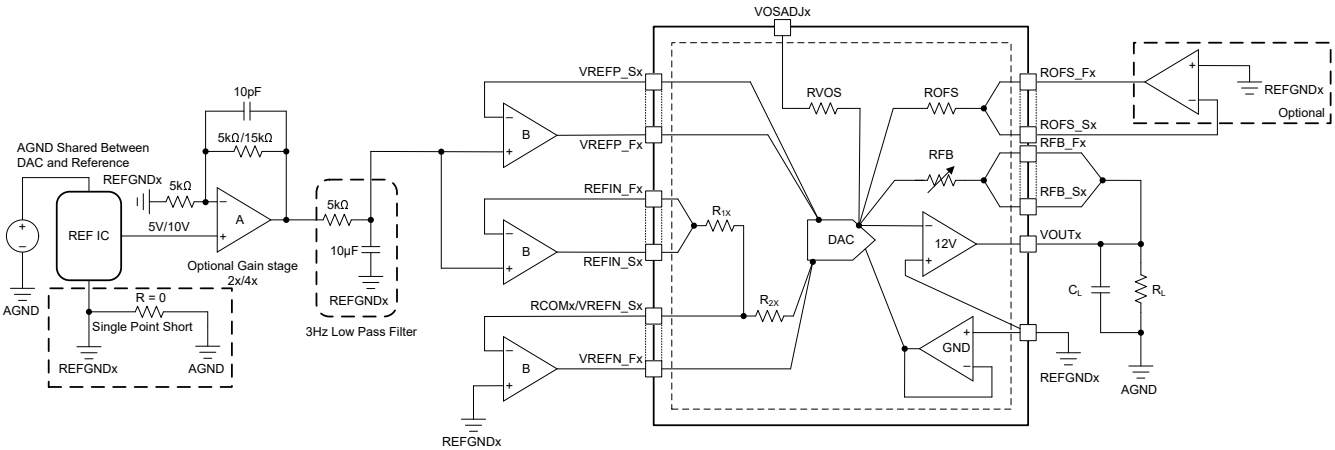

Figure 8-7. DAC90802 Grounding Recommendation

8.3 Power Supply Recommendations

This device can operate within the specified supply voltage range. The power applied is well-regulated and low-noise. To further minimize noise from the power supplies, a strong recommendation is to include a 100pF to 1nF capacitor and a 0.1µF to 1µF bypass capacitor very close to each of the power pins. The current consumption of the power pins, the short-circuit current limit, and typical load current for these devices is in Section 5.5. Select a power supply for these devices to meet the aforementioned current requirements.

8.4 Layout

8.4.1 Layout Recommendation

The PCB layout is critical for achieving the specified ac and dc performance of the DAC90802. Although the device is designed to segregate analog, reference, and digital grounds to minimize noise coupling, a simplified layout can still provide excellent results. By utilizing a single ground plane for the reference section and a separate plane for the digital and analog I/O sections connected through a single-point connection as shown in Figure 8-8 adequate performance is achieved while significantly simplifying the design process.

To enhance signal integrity, digital signals and power supplies must be routed in such a way that digital switching noise is prevented from coupling into the sensitive analog signal path.

To achieve the best signal integrity, place all critical components of the signal chain on the top layer with a solid analog ground from subsequent inner layers to minimize loop inductance. For effective power-supply decoupling, position bypass capacitors near the respective power pins. Furthermore, providing unbroken ground return planes beneath the digital signal traces, particularly for high-speed digital signals, minimizes loop inductance and preserves signal quality.

Use X7R 100nF and 1µF capacitors in parallel for decoupling VCC, VEE, DVDD, VIO, and AVDD. For LVDD, an X7R 10µF capacitor is required; placing this capacitor as close as possible to the LVDD and LGND pins is critical to minimizing glitches.

Reference Buffer and Decoupling Placement of the reference buffer near the DAC reference force and sense pins is critical. A 100pF bypass capacitor (recommended specifically for dc applications) placed directly between the force and sense pins with minimal trace length minimizes parasitic impedance. This configuration provides local charge storage for transient reference currents during DAC switching and allows the sense connection to accurately track the reference voltage at the DAC input, improving overall system dynamic performance.

Provide thermal relief (must be connected to VEE) in the bottom layer with an area > $2in^2$ for best thermal performance.

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8.4.2 Layout Example

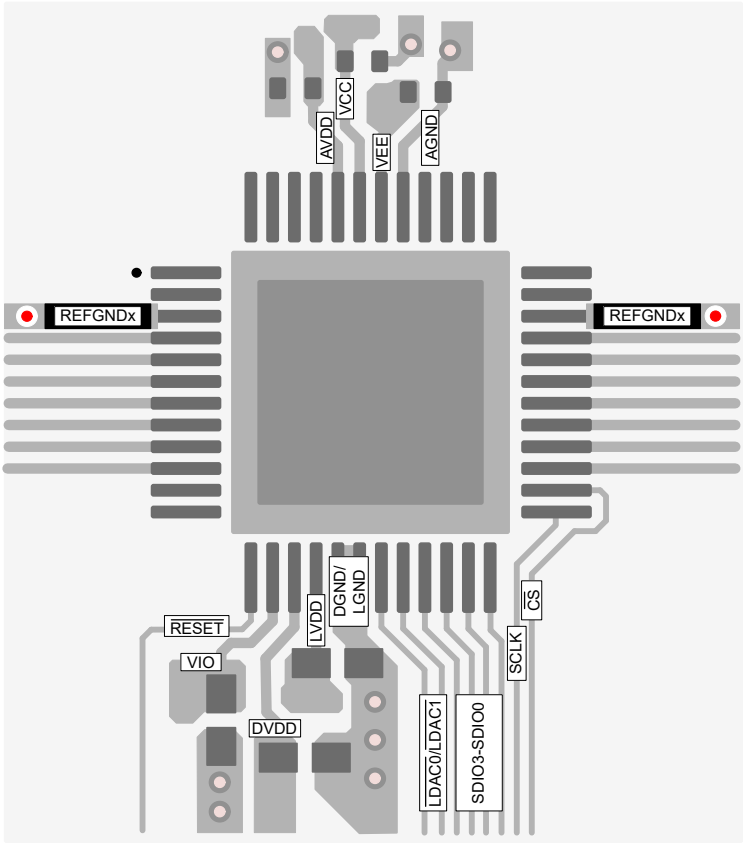

Figure 8-8. DAC90802 Layout Example

9 Device and Documentation Support

9.1 Related Documentation

For related documentation see the following:

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

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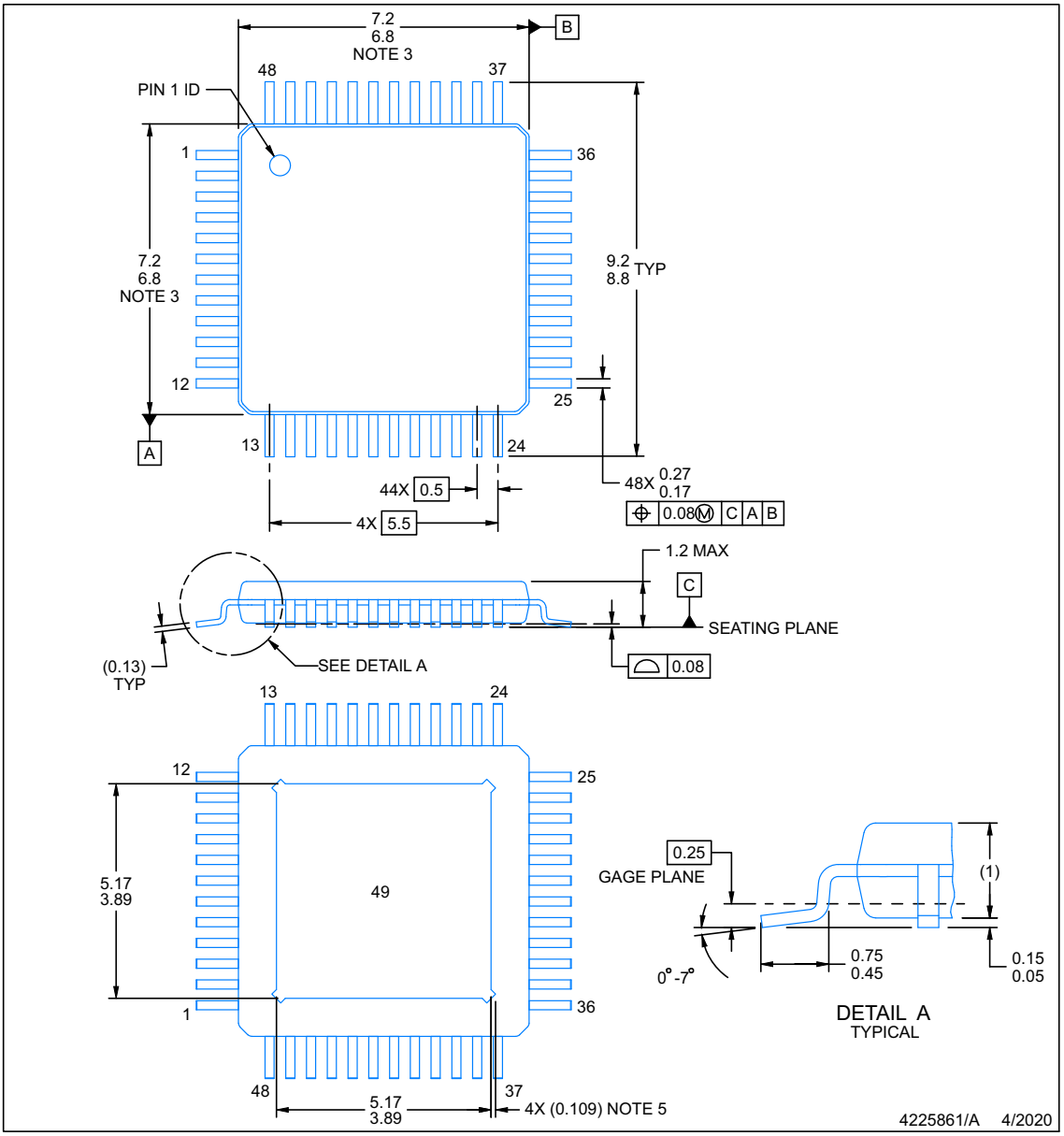
PACKAGE OUTLINE

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

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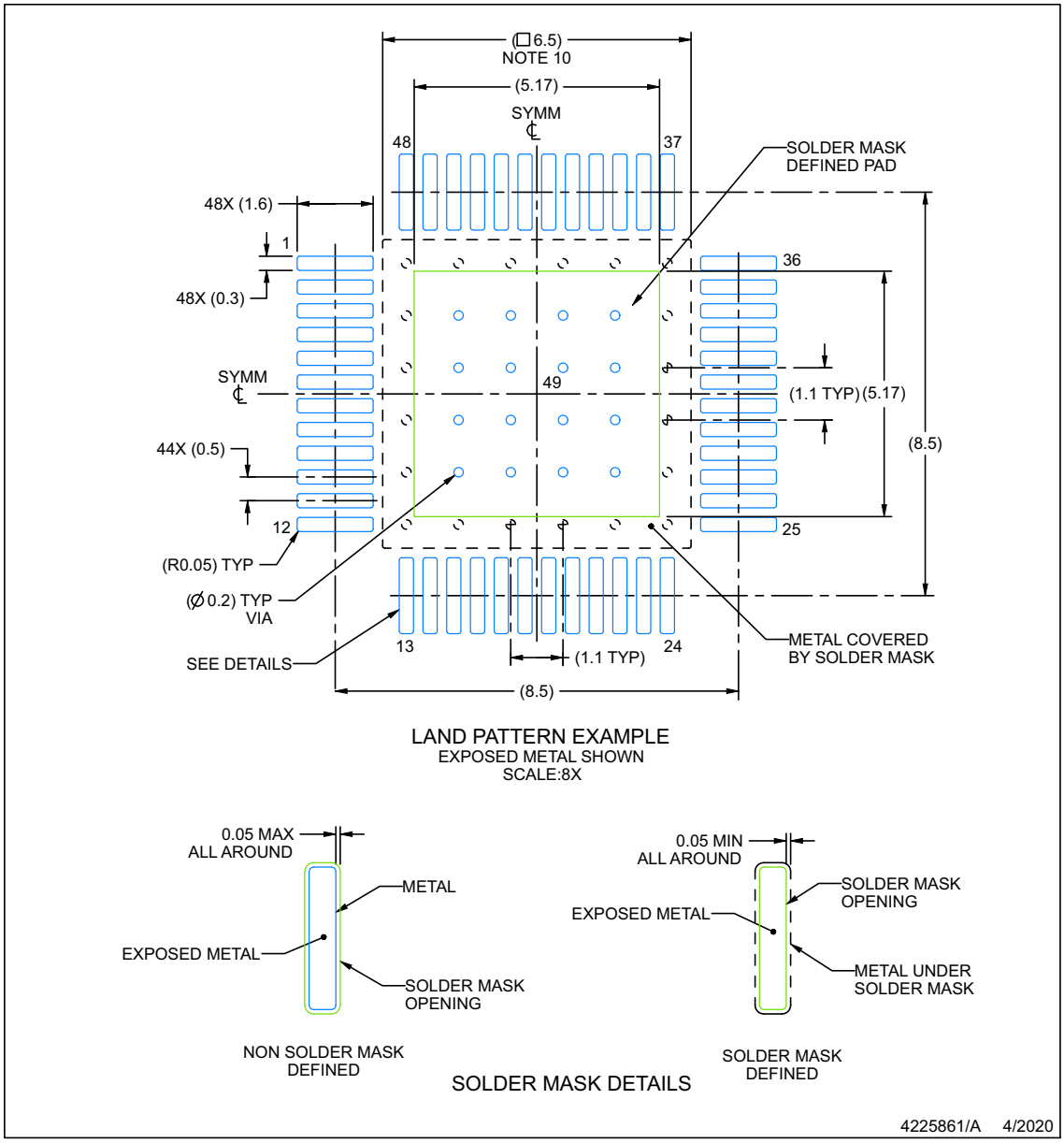
EXAMPLE BOARD LAYOUT

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

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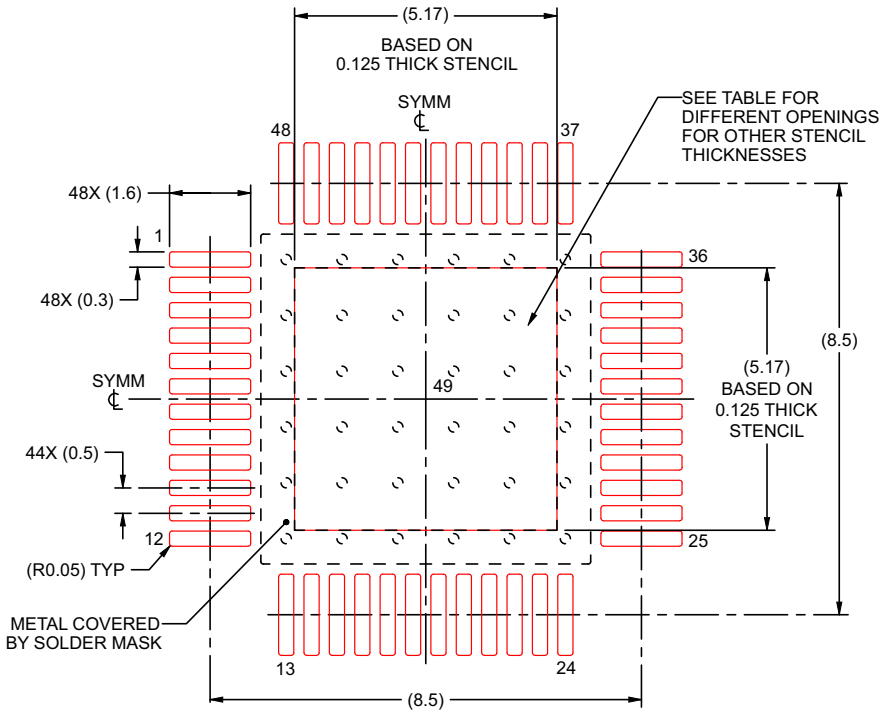
EXAMPLE STENCIL DESIGN

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4225861/A 4/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC90802PHPR	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	DAC90802

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

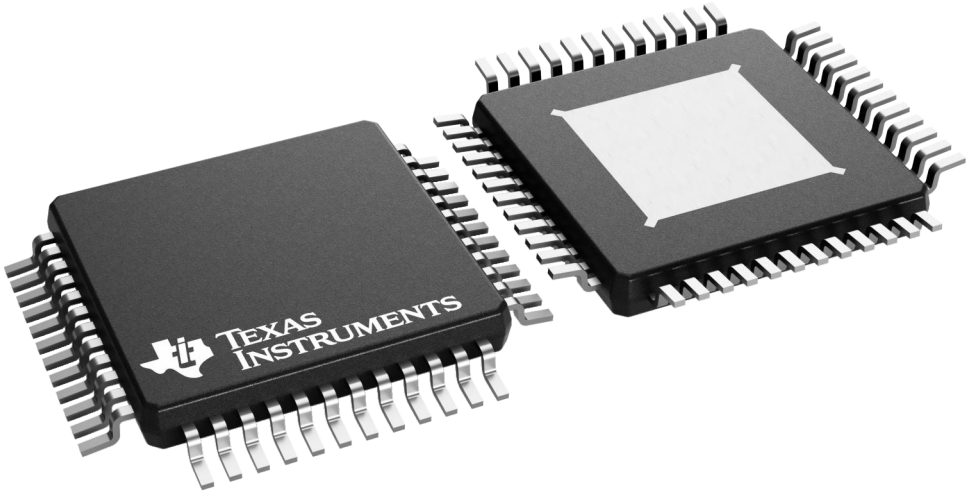
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

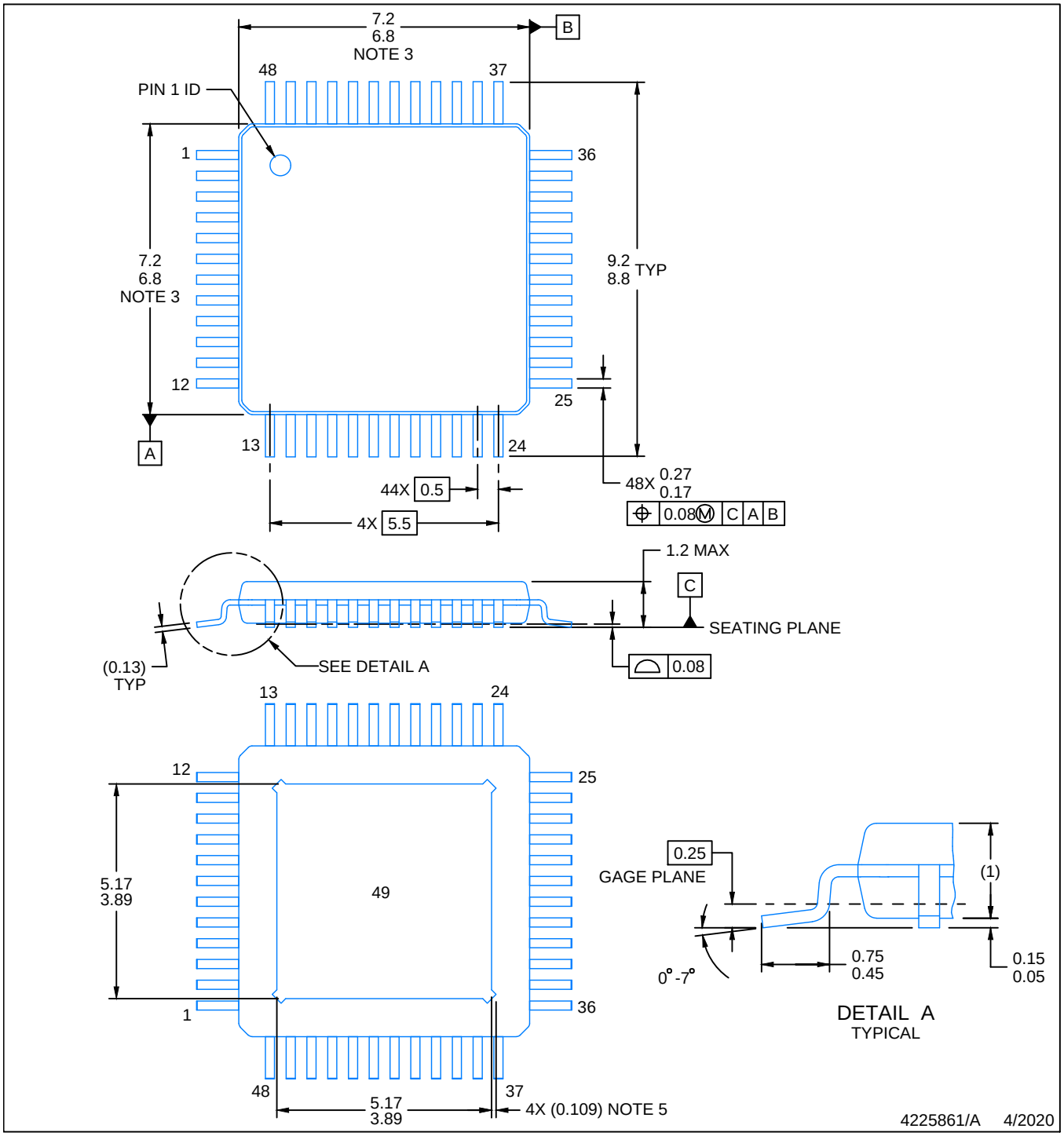


4226443/A

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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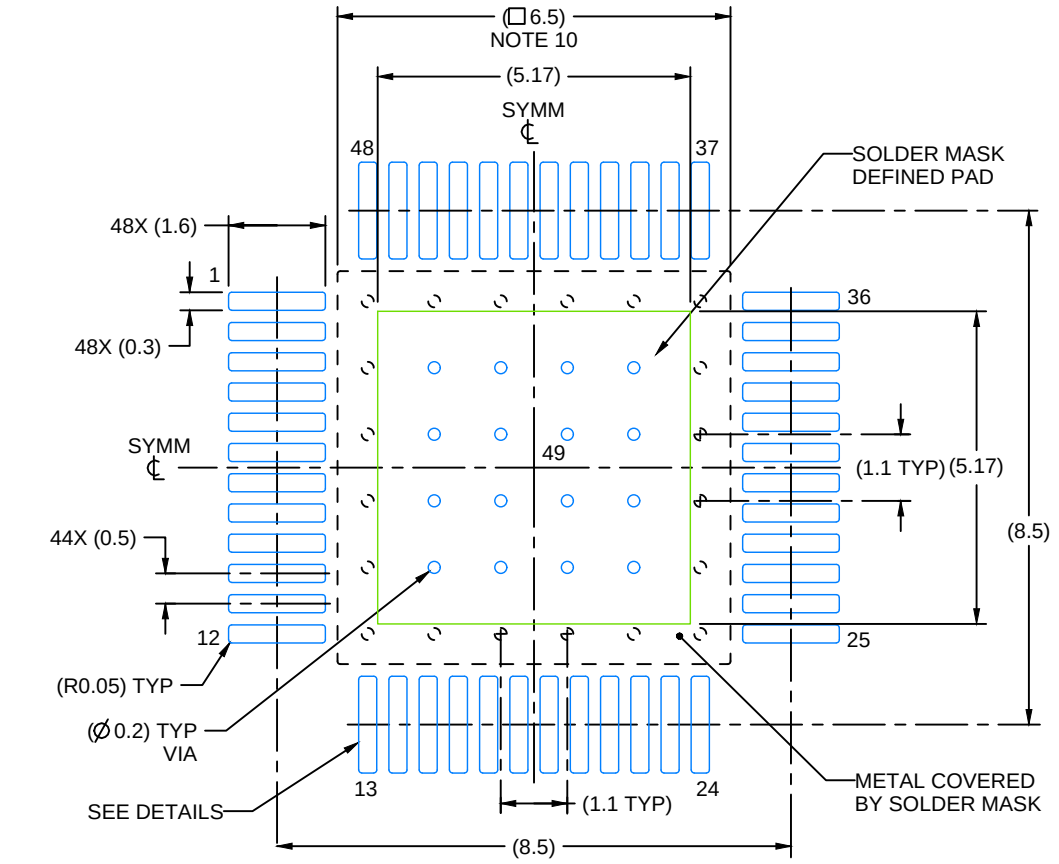
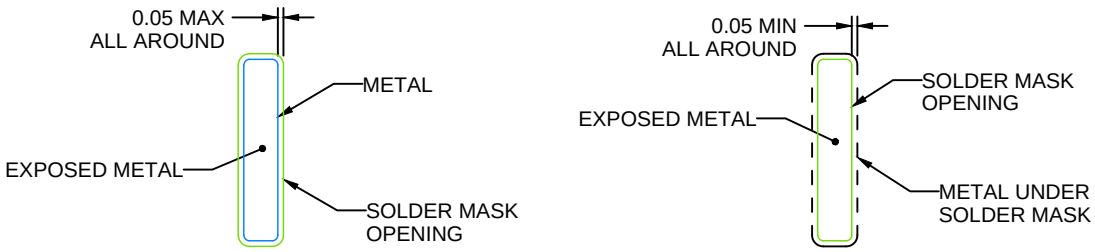
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

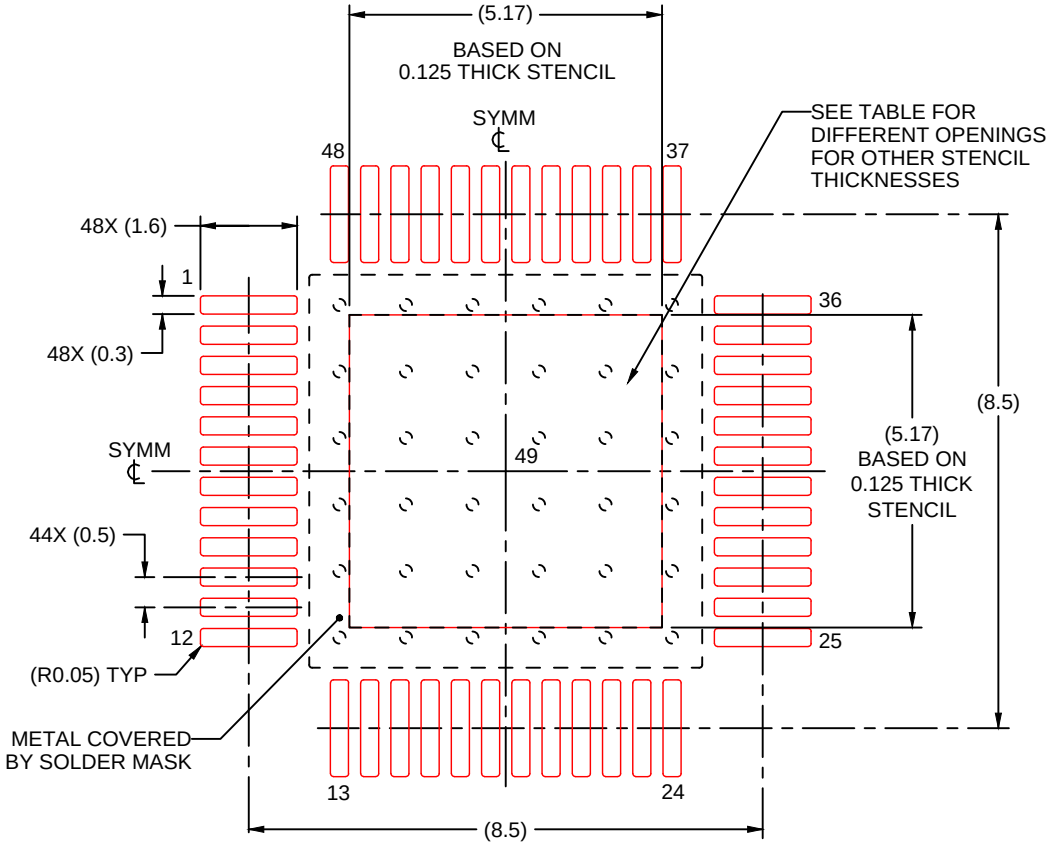
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225861/A 4/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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