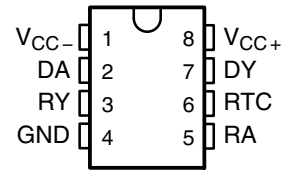


# SN75155 LINE DRIVER AND RECEIVER

SLLS017C – JULY 1986 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28
- 10-mA Current Limited Output
- Wide Range of Supply Voltage  
 $V_{CC} = 4.5 \text{ V to } 15 \text{ V}$
- Low Power . . . 130 mW
- Built-In 5-V Regulator
- Response Control Provides:  
Input Threshold Shifting  
Input Noise Filtering
- Power-Off Output Resistance . . . 300  $\Omega$  Typ
- Driver Input TTL Compatible

D OR P PACKAGE  
TOP VIEW

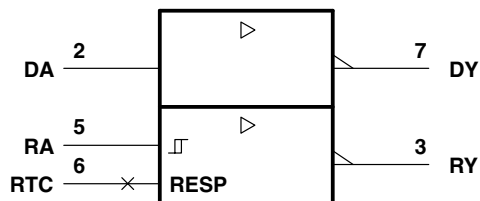


## description

The SN75155 monolithic line driver and receiver is designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI EIA/TIA-232-E. A response control input is provided for the receiver. A resistor or a resistor and a bias voltage can be connected between the response control input and ground to provide noise filtering. The driver used is similar to the SN75188. The receiver used is similar to the SN75189A.

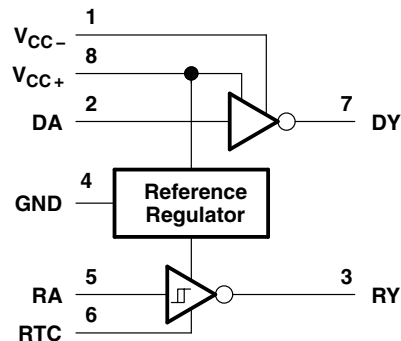
The SN75155 is characterized for operation from 0°C to 70°C.

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

## logic diagram



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

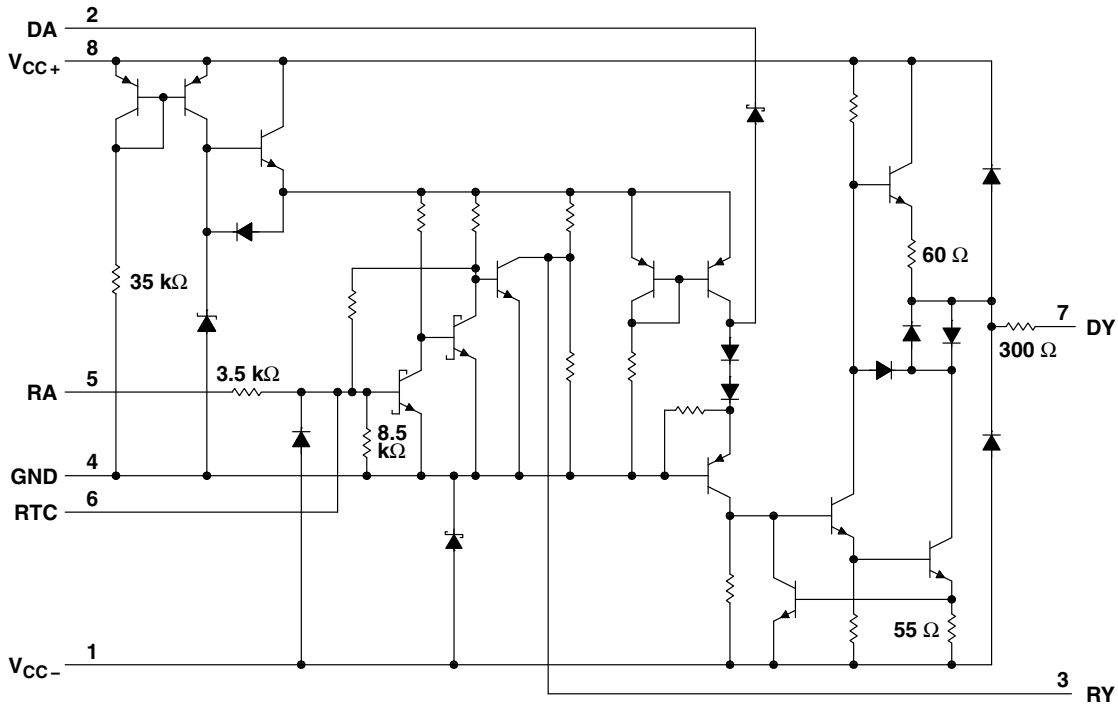
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# SN75155 LINE DRIVER AND RECEIVER

SLLS017C – JULY 1986 – REVISED MAY 1995

## schematic



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ (see Note 1)	15 V
Supply voltage, $V_{CC-}$ (see Note 1)	-15 V
Input voltage range, $V_i$ : Driver	-15 V to 15 V
Receiver	-30 V to 30 V
Output voltage range (driver), $V_o$	-15 V to 15 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$
	POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW



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**recommended operating conditions**

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC+}$	4.5	12	15	V
Supply voltage, $V_{CC-}$	-4.5	-12	-15	V
Output voltage, driver, $V_{O(D)}$			$\pm 15$	V
Input voltage, receiver, $V_{I(R)}$	-25		25	V
High-level input voltage, driver, $V_{IH}$	2			V
Low-level input voltage, driver, $V_{IL}$			0.8	V
Response control current			$\pm 5.5$	mA
Output current, receiver, $I_{O(R)}$			24	mA
Operating free-air temperature, $T_A$	0		70	$^{\circ}\text{C}$

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

**total device**

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$I_{CCH+}$ High-level supply current	$V_{CC+} = 5\text{ V}, V_{CC-} = -5\text{ V}$		6.3	8.1	mA
	$V_{CC+} = 9\text{ V}, V_{CC-} = -9\text{ V}$		9.1	11.9	
	$V_{CC+} = 12\text{ V}, V_{CC-} = -12\text{ V}$		10.4	14	
$I_{CCL+}$ Low-level supply current	$V_{CC+} = 5\text{ V}, V_{CC-} = -5\text{ V}$		2.5	3.4	mA
	$V_{CC+} = 9\text{ V}, V_{CC-} = -9\text{ V}$		3.7	5.1	
	$V_{CC+} = 12\text{ V}, V_{CC-} = -12\text{ V}$		4.1	5.6	
$I_{CC+}$ Supply current	$V_{CC+} = 5\text{ V}, V_{CC-} = 0$		4.8	6.4	mA
	$V_{CC+} = 9\text{ V}, V_{CC-} = 0$		6.7	9.1	
$I_{CCH-}$ High-level supply current	$V_{CC+} = 5\text{ V}, V_{CC-} = -5\text{ V}$		-2.4	-3.1	mA
	$V_{CC+} = 9\text{ V}, V_{CC-} = -9\text{ V}$		-3.9	-4.9	
	$V_{CC+} = 12\text{ V}, V_{CC-} = -12\text{ V}$		-4.8	-6.1	
$I_{CCL-}$ Low-level supply current	$V_{CC+} = 5\text{ V}, V_{CC-} = -5\text{ V}$		-0.2	-0.35	mA
	$V_{CC+} = 9\text{ V}, V_{CC-} = -9\text{ V}$		-0.25	-0.4	
	$V_{CC+} = 12\text{ V}, V_{CC-} = -12\text{ V}$		-0.27	-0.45	

† All typical values are at  $T_A = 25^{\circ}\text{C}$ .

# SN75155 LINE DRIVER AND RECEIVER

SLLS017C – JULY 1986 – REVISED MAY 1995

electrical characteristics over recommended operating free-air temperature range,  $V_{CC+} = 12\text{ V}$ ,  $V_{CC-} = -12\text{ V}$  (unless otherwise noted)

## driver section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OH}$ High-level output voltage	$V_{IL} = 0.8\text{ V}$ , $R_L = 3\text{ k}\Omega$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$	3.2	3.7	V
		$V_{CC+} = 9\text{ V}$ , $V_{CC-} = -9\text{ V}$	6.5	7.2	
		$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$	8.9	9.8	
$V_{OL}$ Low-level output voltage (see Note 2)	$V_{IH} = 2\text{ V}$ , $R_L = 3\text{ k}\Omega$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$	-3.6	-3.2	V
		$V_{CC+} = 9\text{ V}$ , $V_{CC-} = -9\text{ V}$	-7.1	-6.4	
		$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$	-9.7	-8.8	
$I_{IH}$ High-level input current	$V_I = 7\text{ V}$			5	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_I = 0$		-0.73	-1.2	mA
$I_{OS(H)}$ High-level short-circuit output current	$V_I = 0.8\text{ V}$ , $V_O = 0$	-7	-12	-14.5	mA
$I_{OS(L)}$ Low-level short-circuit output current	$V_I = 2\text{ V}$ , $V_O = 0$	6.5	11.5	15	mA
$r_o$ Output resistance with power off	$V_O = -2\text{ V}$ to $2\text{ V}$		300		$\Omega$

## receiver section (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
$V_{IT+}$ Positive-going input threshold voltage		1.2	1.9	2.3	V	
$V_{IT-}$ Negative-going input threshold voltage		0.6	0.95	1.2	V	
$V_{hys}$ Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )		0.6			V	
$V_{O(H)}$ High-level output voltage	$V_I = 0.6\text{ V}$ , $I_{OH} = 10\text{ }\mu\text{A}$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$	3.7	4.1	4.5	V
		$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$	4.4	4.7	5.2	
	$V_I = 0.6\text{ V}$ , $I_{OH} = 0.4\text{ mA}$	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = -5\text{ V}$	3.1	3.4	3.8	
		$V_{CC+} = 12\text{ V}$ , $V_{CC-} = -12\text{ V}$	3.6	4	4.5	
$V_{O(L)}$ Low-level output voltage	$V_I = 2.3\text{ V}$ , $I_{OL} = 24\text{ mA}$		0.2	0.3	V	
$I_{IH}$ High-level input current	$V_I = 2.5\text{ V}$	3.6	6.7	10	mA	
	$V_I = 3\text{ V}$	0.43	0.67	1	mA	
$I_{IL}$ Low-level input current	$V_I = -25\text{ V}$	-3.6	-6.7	-10	mA	
	$V_I = -3\text{ V}$	-0.43	-0.67	-1	mA	
$I_{OS}$ Short-circuit output current	$V_I = 0.6\text{ V}$		-2.8	-3.7	mA	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

NOTE 2: The algebraic limit system, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic voltage levels only (e.g., if  $-8.8\text{ V}$  is the maximum, the typical value is a more negative value).



switching characteristics over recommended operating free-air temperature range,  $V_{CC+} = 5\text{ V}$ ,  $V_{CC-} = -5\text{ V}$ ,  $C_L = 50\text{ pF}$  (unless otherwise noted)

driver section (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high level output	$R_L = 3\text{ k}\Omega$		250	480	ns
$t_{PHL}$ Propagation delay time, high- to low level output			80	150	
$t_r$ Output rise time	$R_L = 3\text{ k}\Omega$		67	180	ns
	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $C_L = 2500\text{ pF}$		2.4	3	$\mu\text{s}$
$t_f$ Output fall time	$R_L = 3\text{ k}\Omega$		48	160	ns
	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $C_L = 2500\text{ pF}$		1.9	3	$\mu\text{s}$

receiver section (see Figure 3)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high level output	$R_L = 400\ \Omega$		175	245	ns
$t_{PHL}$ Propagation delay time, high- to low level output			37	100	
$t_r$ Output rise time	$R_L = 400\ \Omega$		255	360	ns
$t_f$ Output fall time	$R_L = 400\ \Omega$		23	50	ns

† All typical values are at  $T_A = 25^\circ\text{C}$ .

### PARAMETER MEASUREMENT INFORMATION

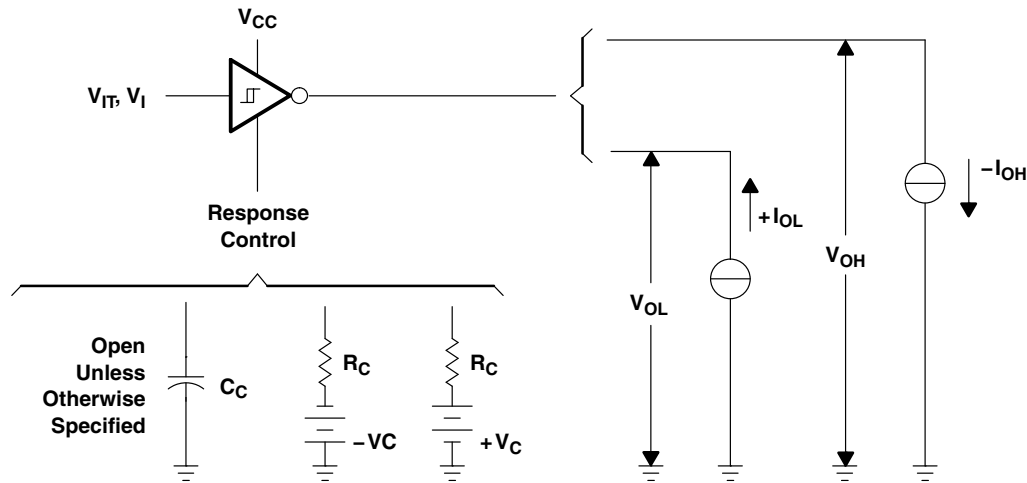
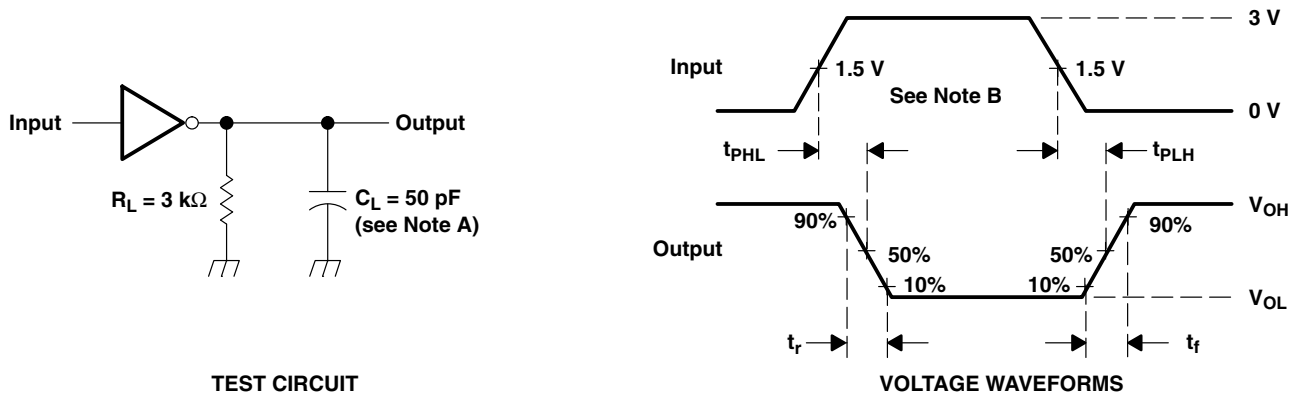


Figure 1. Receiver Section Test Circuit ( $V_{IT+}$ ,  $V_{IT-}$ ,  $V_{OH}$ ,  $V_{OL}$ )

# SN75155 LINE DRIVER AND RECEIVER

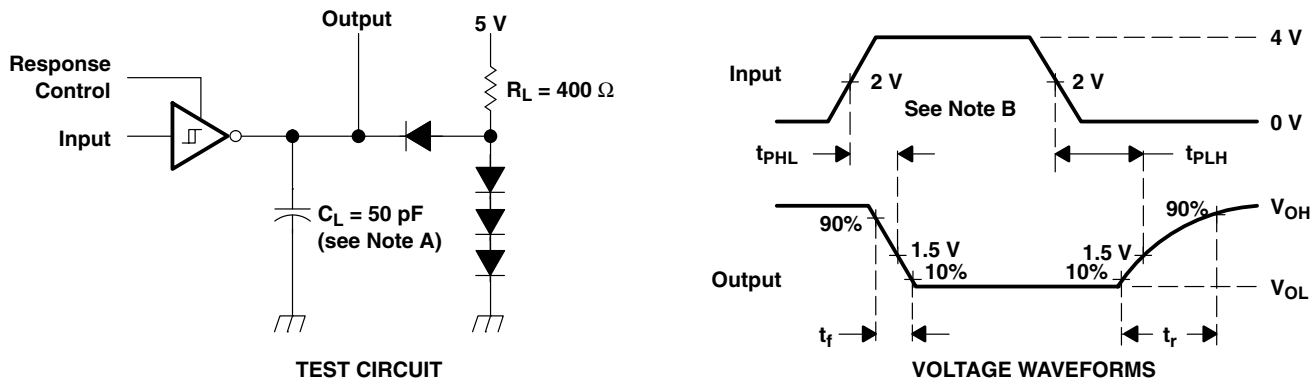
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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input waveform is supplied by a generator with the following characteristics:  $Z_O = 50 \Omega$ ,  $t_w = 1 \mu s$ ,  $t_r \leq 10 ns$ ,  $t_f \leq 10 ns$ .

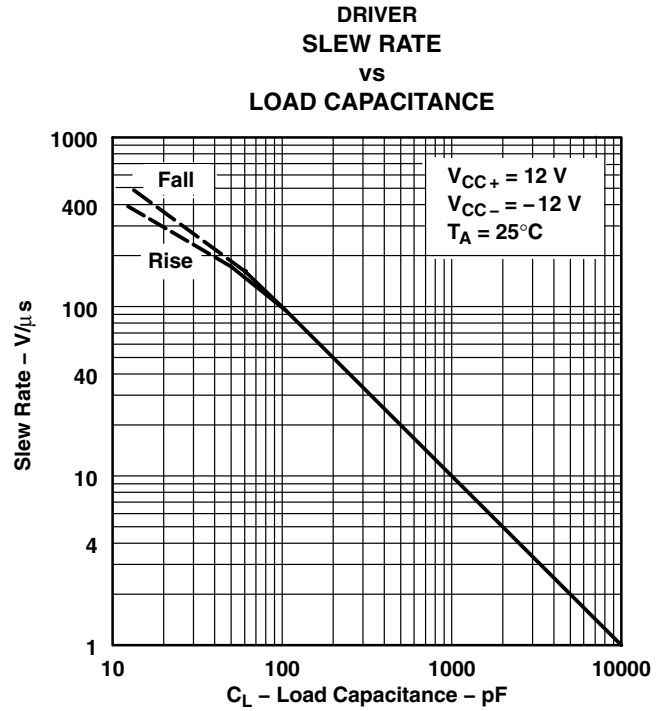
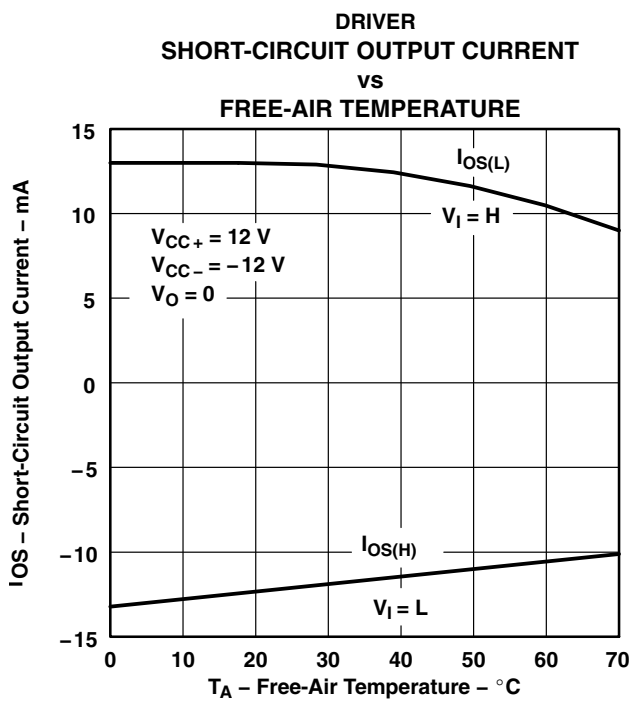
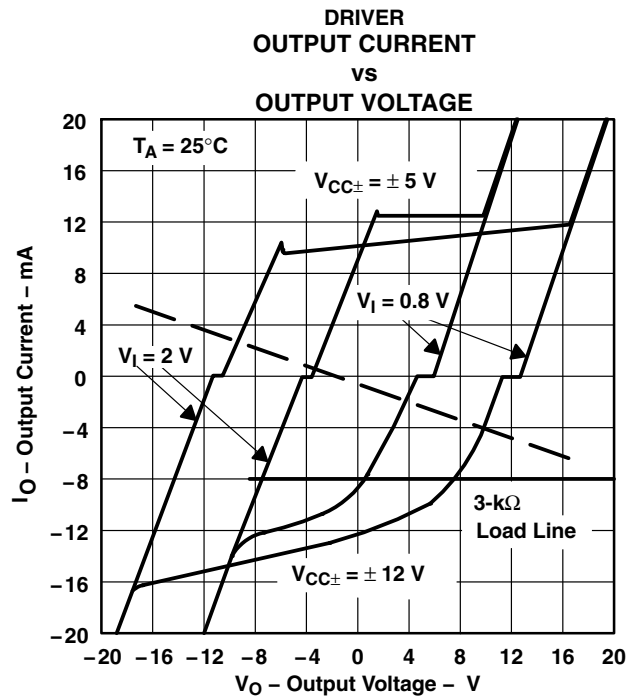
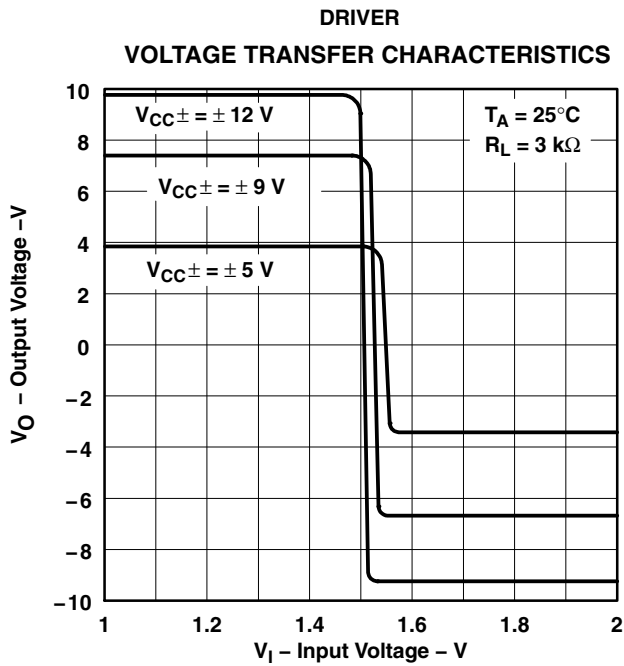
**Figure 2. Driver Section Switching Test Circuit and Voltage Waveforms**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input waveform is supplied by a generator with the following characteristics:  $Z_O = 50 \Omega$ ,  $t_w = 1 \mu s$ ,  $t_r \leq 10 ns$ ,  $t_f \leq 10 ns$ .

**Figure 3. Receiver Section Switching Test Circuit and Voltage Waveforms**

TYPICAL CHARACTERISTICS



# SN75155 LINE DRIVER AND RECEIVER

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## TYPICAL CHARACTERISTICS

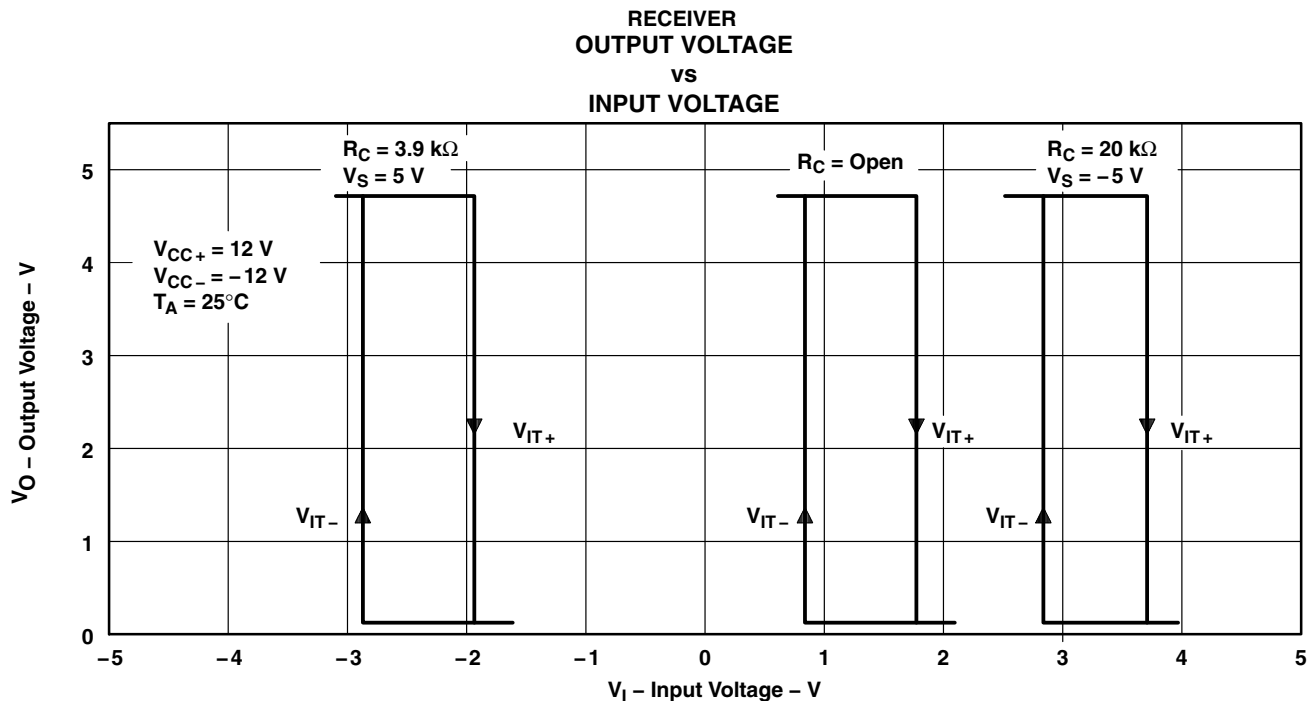


Figure 8

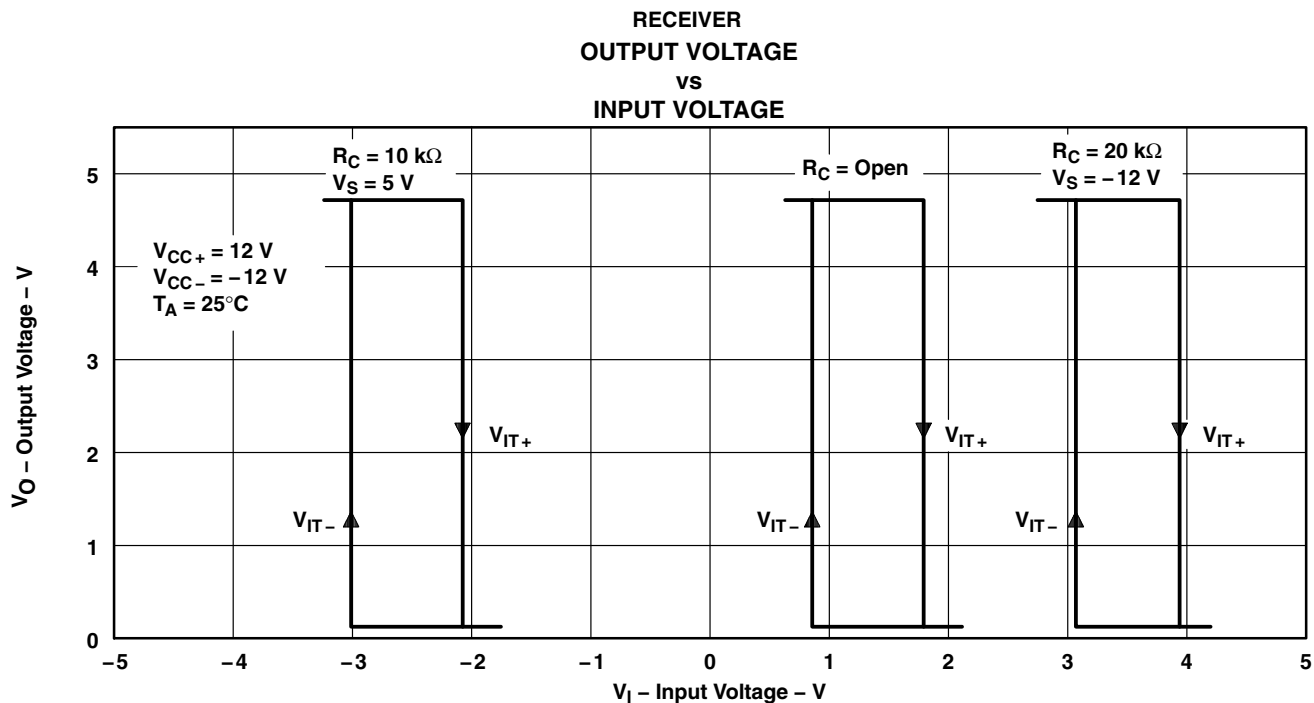


Figure 9



TYPICAL CHARACTERISTICS

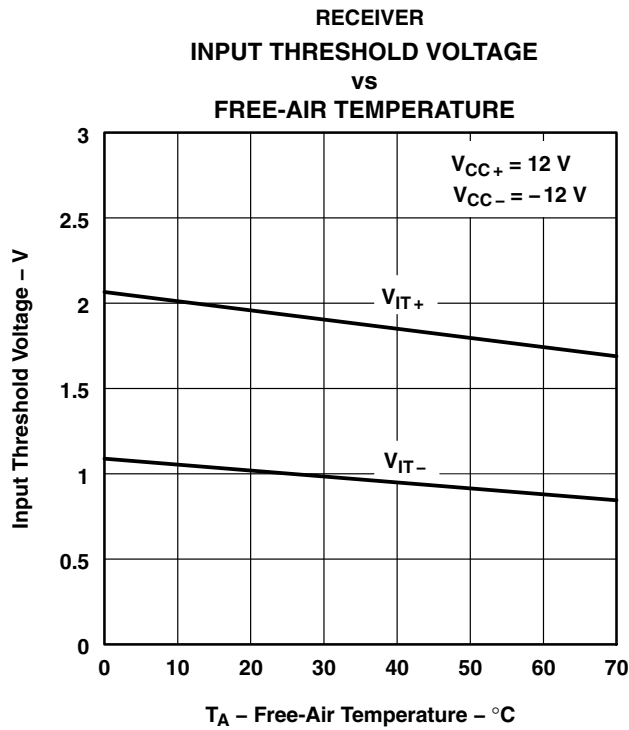


Figure 10

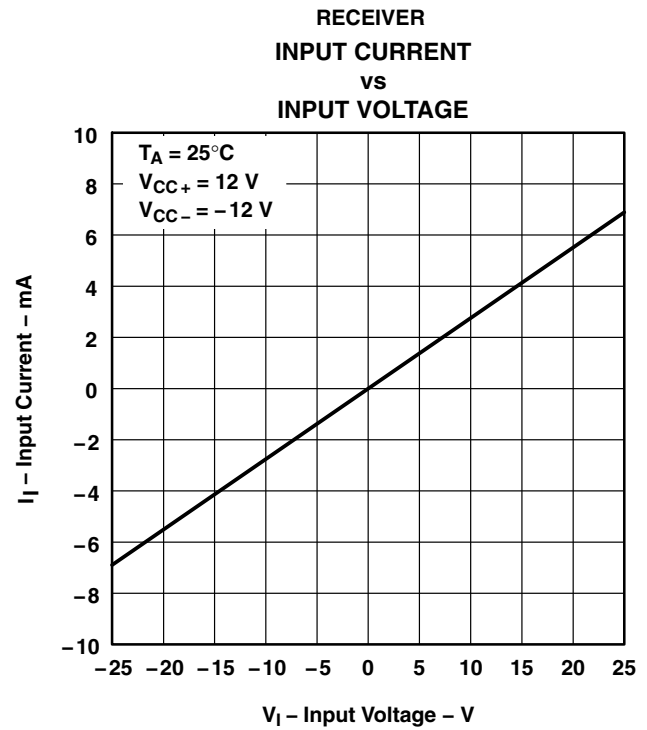


Figure 11

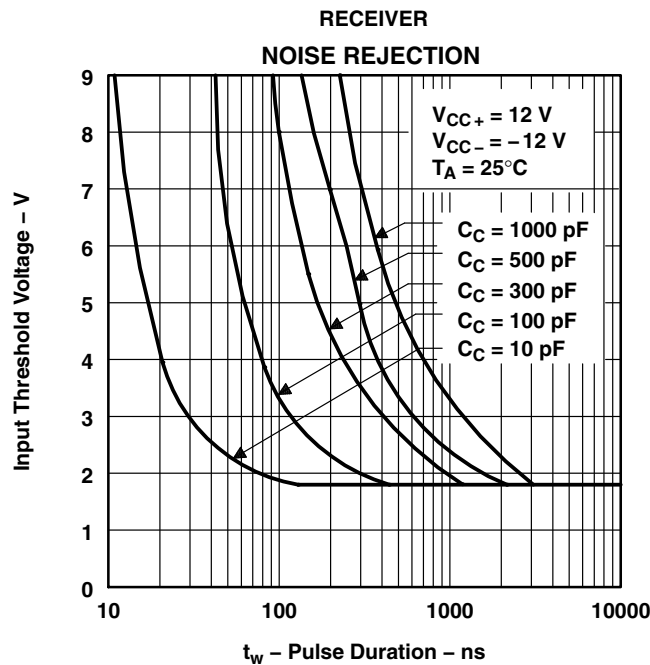


Figure 12

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75155D	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75155	
SN75155DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75155	Samples
SN75155DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75155	Samples
SN75155P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75155P	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

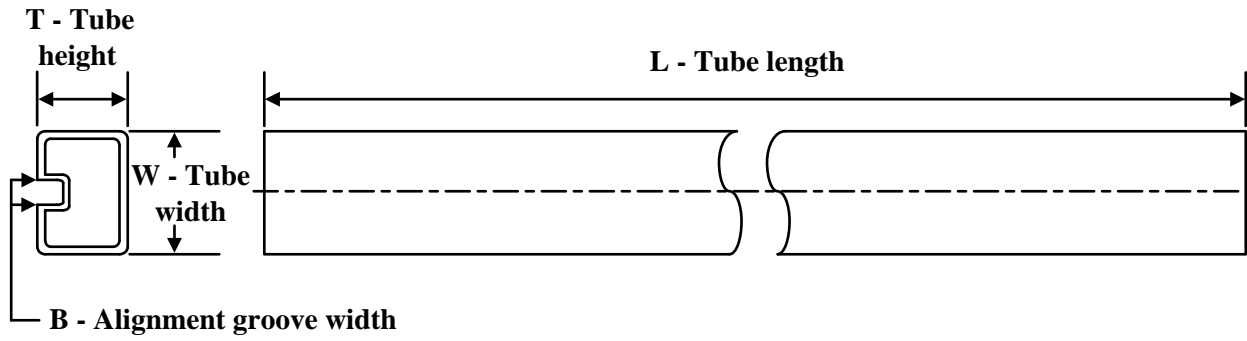
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75155DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



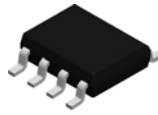
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75155DR	SOIC	D	8	2500	340.5	336.1	25.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75155D	D	SOIC	8	75	507	8	3940	4.32
SN75155P	P	PDIP	8	50	506	13.97	11230	4.32

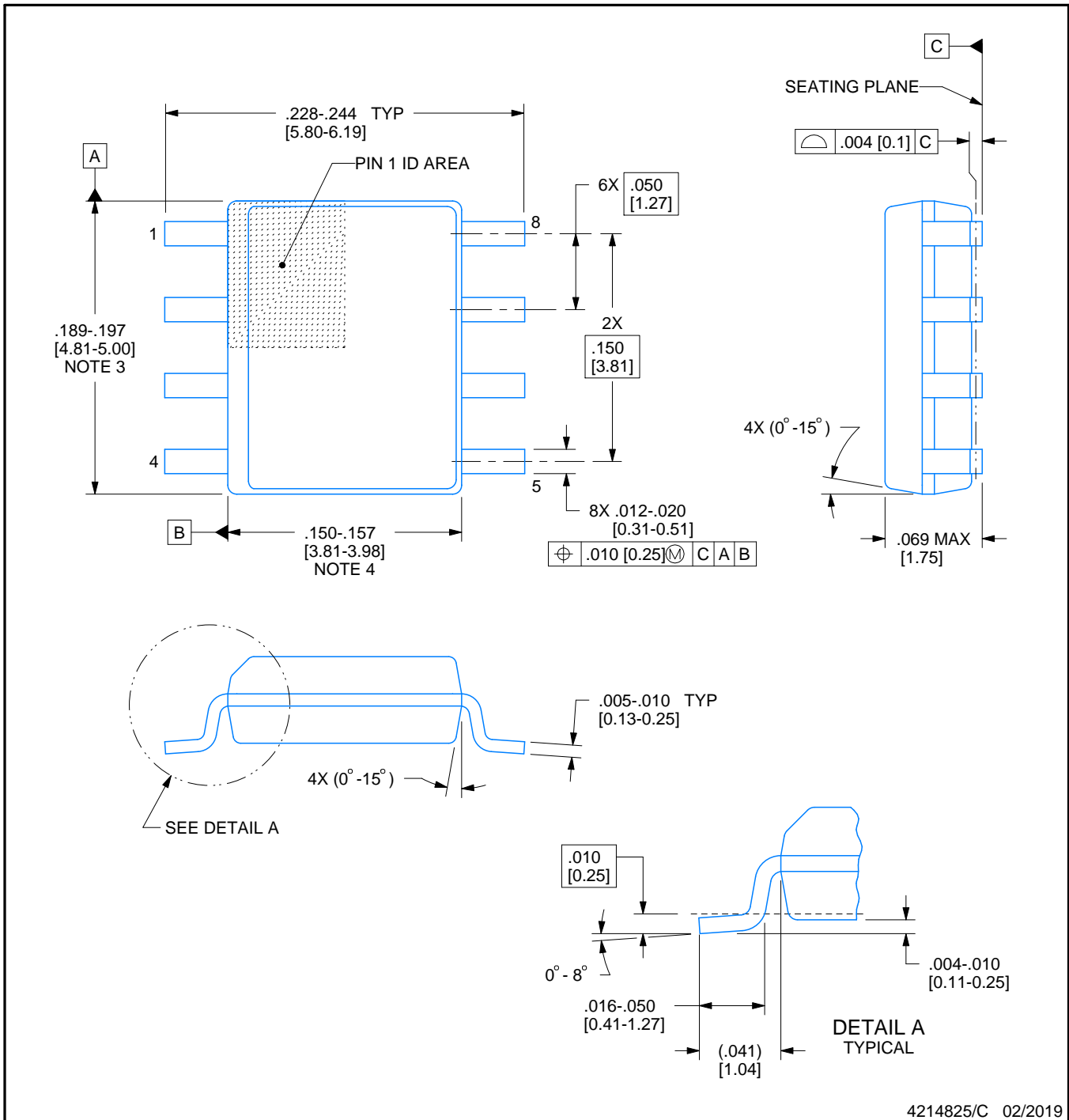


D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

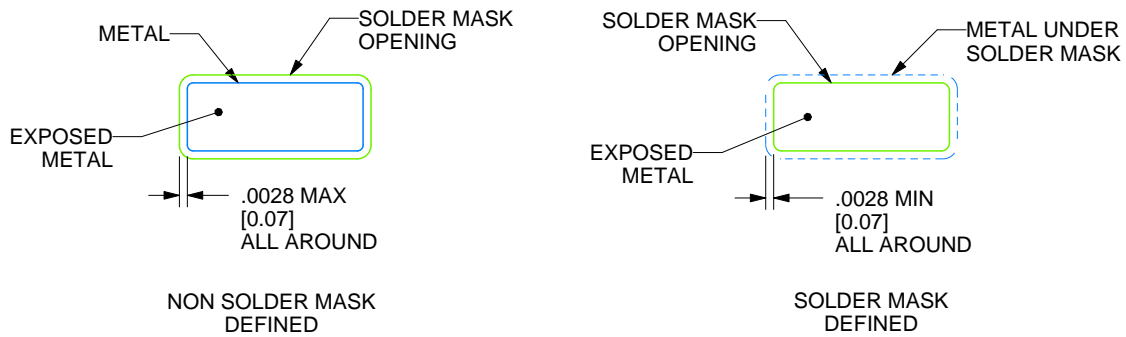
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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