1 TO 2.6 GBPS TRANSCEIVER

Check for Samples: TLK2541

FEATURES

- **1 to 2.6 Gigabits Per Second (Gbps) Serializer/Deserializer**
- **Independent Transmit/Receive Channels for Asynchronous Data Rate Operation**
- **Fast Relock at 1.25 Gbps and 2.5 Gbps for EPON OLT Applications**
- **Hot-Plug Protection**
- **High-Performance 80-Pin TQFP Package (PFP)**
- **2.5-V Power Supply for Low Power Operation**
- **Programmable Preemphasis Levels on Serial Output**
- **Interfaces to Backplane, Copper Cables, or Optical Converters**
- **On-Chip 8-bit/10-bit Encoding/Decoding**
- **On-Chip PLL Provides Clock Synthesis From Low-Speed Reference**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **3 V Tolerance on Parallel Data Input Signals**
- **Selectable 10 or 20 bit Parallel TTL Compatible Data Interface**
- **Industrial Temperature Range –40°C to 85°C**
- **Integrated 50-Ω Termination Resistors on RX**
- **Transmit FIFO Decouples Transmit Clock From Reference Clock**

APPLICATIONS

- **Next Generation EPON OLT Systems**
- **Ideal for use with EPON OLT MAC Solutions such as TK3723 from Teknovus**
- **Gigabit Ethernet and Fibre Channel Links**

DESCRIPTION

The TLK2541 is a member of the *WizardLink* transceiver family of multigigabit transceivers, intended for use in high-speed bidirectional point-to-point data transmission systems. The TLK2541 supports an effective serial interface speed of 1 Gbps to 1.3 Gbps or 2 to 2.6 Gbps, providing over 2 Gbps of data bandwidth.

The primary application of this chip is to provide high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50Ω. The transmission media can be printed-circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment. The TLK2541 allows for independent transmit and receive data rate operation for applications that need asymmetrical data rates such as Passive Optical Networking.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector terminals, and transmit/receive terminals. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. It is then reconstructed into its original parallel format. It offers significant power and cost savings over parallel solutions, as well as scalability for higher data rates.

At full rate, the TLK2541 performs data conversion parallel-to-serial and serial-to-parallel. The clock extraction functions as a physical layer interface device. The serial transceiver interface operates at a maximum speed of 2.6 Gbps. The transmitter latches 20 parallel data at a rate based on the supplied transmit clock (TX_CLK).. The 20-bit word is then transmitted differentially at 20 times the reference clock (REFCLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the recovered clock (RX_CLK). It then outputs the 20 bit recovered word on the receive data terminals RXD[0:19]. If the internal 8B/10B coding and decoding logic is enabled, 16 bits of data and two bits of control are latched on TX_CLK and the data is encoded into a 20 bit data word to be serialized. Likewise the 20 bit received data word is decoded into a 16 bit data word plus two bits of decode status.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

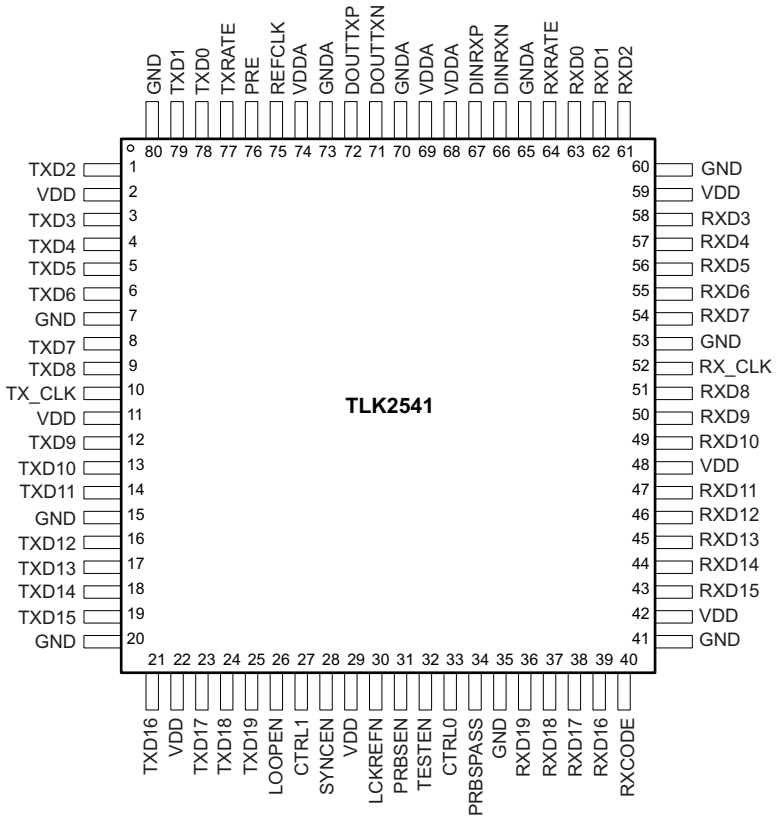
DESCRIPTION (CONTINUED)

At half rate, the TLK2541 only uses half of the parallel transmit and receive data busses. 10 bits of data on TXD[0:9] are latched by TX_CLK and serialized. If 8B/10B coding is enabled, 8 bits of data plus 1 bit of control is latched and the resulting 10 bit code word is serialized. The 10 bit received data word is output on RXD[0:9]. If 8B/10B decoding is enabled, the 10 bit received word is decoded and the 8 bit data plus 1 bit status is output.

The TLK2541 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer, providing the protocol device with a functional self-check of the physical interface.

The TLK2541 uses a 2.5-V supply. The I/O section is 3 V compatible. With the 2.5-V supply the chipset is very power efficient, consuming less than 625 mW typically. The TLK2541 is characterized for operation from –40°C to 85°C.

The TLK2541 is designed to be hot-plug capable. An on-chip power-on reset circuit holds the RX_CLK low and goes to high impedance on the parallel side output signal terminals as well as TXP and TXN during power up.



BLOCK DIAGRAM

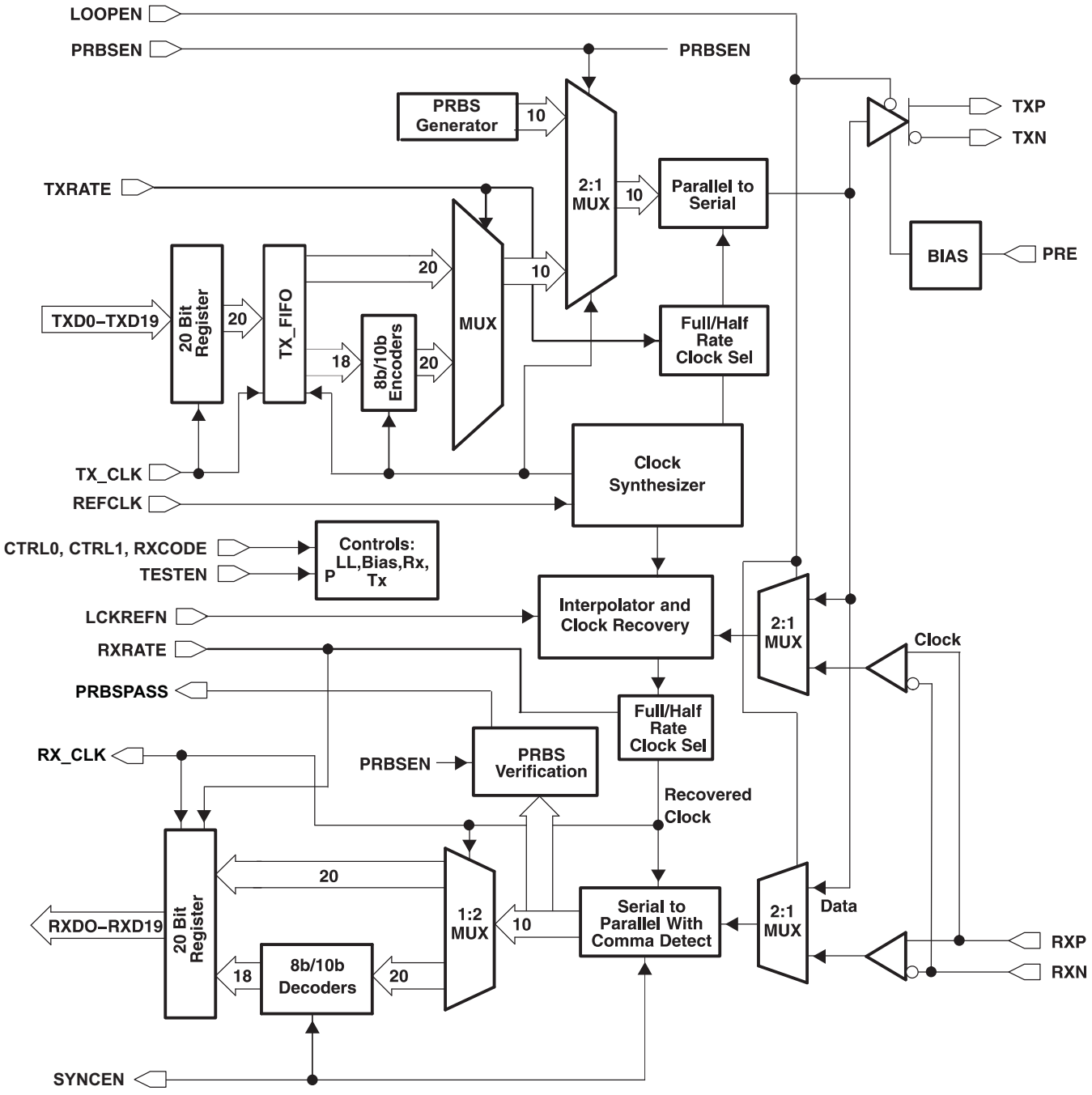


Figure 1. TLK2541 Block Diagram

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
DOUTTXP DOUTTXN	72 71	Output (Hi-Z power-up)	**Serial Transmit Outputs.** DOUTTXP and DOUTTXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 10 or 20 times the TX_CLK value. DOUTTXP and DOUTTXN are put in a high impedance state when LOOPEN is high and are active when LOOPEN is low. When Disabled or during power-on-reset these pins are high impedance.
DINRXP DINRXN	67 66	Input	**Serial Receive Inputs.** DINRXP and DINRXN together are the differential serial input interface from a copper or an optical I/F module.
TX_CLK	10	Input	**Transmit Clock.** TX_CLK is a continuous external input clock that synchronizes the transmitter parallel interface signals TXD[0:19]. The frequency range of TX_CLK is 100 MHz to 130 MHz. The transmitter uses the rising edge of this clock to register the input data (TXD) for serialization.
REFCLK	75	Input	**Reference Clock.** REFCLK is a clean reference clock for input to the phase lock loop. REFCLK must be the same frequency as TX_CLK.
TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7 TXD8 TXD9 TXD10 TXD11 TXD12 TXD13 TXD14 TXD15 TXD16 TXD17 TXD18 TXD19	78 79 1 3 4 5 6 8 9 12 13 14 16 17 18 19 21 23 24 25	Input	**Transmit Data Bus.** These inputs carry the 20-bit parallel data output from a protocol device to the transceiver for serialization and transmission. This 20-bit parallel data is clocked into the transceiver on the rising edge of TX_CLK. When the transmitter is operating at 20 times REFCLK rate, the full width of the transmit parallel bus is latched on the rising edge of TX_CLK and serialized. When the transmitter is operating at 10 times REFCLK rate, only the lower half of the transmit parallel bus is latched and serialized. When the on-chip encode/decode logic is bypassed, the full 20 bit data bus is serialized at full data rate. At half data rate only bits TXD0 through TXD9 are serialized. When the on-chip encode/decode logic is utilized, bits TXD[0:7] make up the lower order data byte and bit TXD[16] becomes the K control bit for the lower order byte. Bits TXD[8:15] make up the higher order byte and bit TXD[17] becomes the K control bit for the higher order byte. Bits TXD[18] and TXD[19] are ignored. At full data rate both lower and higher order bytes are latched, coded, and serialized. At half data rate, only the lower order byte is latched, coded and serialized. The lower order byte is always serialized first, and the lower order bit in a byte is always serialized first.
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7 RXD8 RXD9 RXD10 RXD11 RXD12 RXD13 RXD14 RXD15 RXD16 RXD17 RXD18 RXD19	63 62 61 58 57 56 55 54 51 50 49 47 46 45 44 43 39 38 37 36	Output (Hi-Z on power- up)	**Receive Data Bus.** These outputs carry 20-bit parallel data output from the transceiver to the protocol device, synchronized to RX_CLK. The data is valid on the rising edge of RX_CLK. These pins are high impedance during power-on reset. When the receiver is operating at 20 times REFCLK rate, the full width of the receive parallel bus is valid on the rising edge of RX_CLK. When the receiver is operating at 10 times REFCLK rate, only the lower half of the receive parallel bus is valid on the rising edge of RX_CLK. When the on-chip encode/decode logic is bypassed, raw coded data is presented on the receive parallel bus. At full data rate, data is presented on bits RXD0 through RXD19. At half data rate only bits RXD0 through RXD9 are valid When the on-chip encode/decode logic is utilized, bits RXD[0:7] make up the lower order data byte and bit RXD[16] becomes the K status bit for the lower order byte. Bits RXD[8:15] make up the higher order byte and bit RXD[17] becomes the K status bit for the higher order byte. Bits RXD[18] and RXD[19] are high impedance. At full data rate both lower and higher order bytes are de-serialized, decoded and output. At half data rate, only the lower order byte is de-serialized, decoded and output. The first received byte is always output on the lower order byte, and the first bit to be received is always presented in the lower order bit of a byte.
RX_CLK	52	Output (low on power-up)	**Recovered Clock.** Output clock that is synchronized to RXD[0:19]. RX_CLK is the recovered serial data rate clock divided by 10 or 20 depending on rate selection. RX_CLK is low during power-on reset.
TXRATE	77	Input (w/Pull-up)	**Transmit Rate Select.** When pulled high or left unconnected, the transmit path operates at a data rate of 20 times REFCLK. This provides a data rate range of 2.0 to 2.6 Gbps. In this mode, the width of the transmit parallel bus is 2 Bytes, either 20 bit coded data or 16 bit date plus two K-control bits for uncoded data. When pulled low, the transmit path operates at a data rate of 10 times REFCLK. This provides a data rate range of 1.0 to 1.3 Gbps. In this mode, the width of the transmit parallel bus is 1 Byte, either 10 bit coded data or 8 bit date plus one K-control bit for uncoded data.

TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
RXRATE	64	Input (w/Pull-up)	**Receive Rate Select.** When pulled high or left unconnected, the receive path expects to operate at a data rate of approximately 20 times REFCLK. This provides a data rate range of 2.0 to 2.6 Gbps. In this mode, the width of the receive parallel bus is 2 Bytes, either 20 bit coded data or 16 bit date plus two K-status bits of un-coded data.
			When pulled low, the receive path expects to operate at a data rate of approximately 10 times REFCLK. This provides a data rate range of 1.0 to 1.3 Gbps. In this mode, the width of the receive parallel bus is 1 Byte, either 10 bit coded data or 8 bit date plus one K-status bit of uncoded data.
PRBSPASS /FIFO_ERR	34	Output (low on power-up)	**PRBS PASS Output.** When PRBSEN is enabled, this pin reflects the result of the on-chip PRBS verifier. When the PRBS verifier is detects that the de-serialized data stream matches the PRBS data pattern then this output goes high. If the PRBS verifier detects one or more bits in a received word that do not match the PRBS pattern then this output goes low for that clock cycle. When PRBSEN is enabled, the PRBSPASS output my be latched or unlatched. If the PRBSPASS is not latched, then the PRBSPASS output will go low for only the clock cycle in which there is an error detected in the PRBS pattern. If the PRBSPASS is latched, then the PRBSPASS will go low and remain low when an error is detected. While PRBSEN is active, SYNCEN controls whether the PRBSPASS is latched or not latched. When SYNCEN is high, the PRBSPASS is latched. When SYNCEN is low, the PRBSPASS is not latched. When used in latched mode, toggling SYNCEN is used to clear a latched PRBSPASS output. When PRBSEN is not enabled, then this pin becomes FIFO_ERR. FIFO_ERR will go active whenever the internal transmit FIFO overflows or underflows and remain active until the FIFO reinitializes itself, which typically takes a few clock cycles. FIFO_ERR should never go active unless there is excessive wander on the TXCLK relative to REFCLK, or there is a frequency mismatch between the TX_CLK and REFCLK clock domains. The TX_CLK may accept as much as ±1 byte of phase wander relative to REFCLK, but the TX_CLK must be frequency locked to REFCLK and have 0-ppm frequency mismatch between TX_CLK and REFCLK. The transmit FIFO automatically reinitializes itself upon power-up reset or upon detection of an overflow or underflow.
PRE	76	Input (w/pull down)	**Pre-emphasis Control.** Selects the amount of pre-emphasis to be added to the high-speed serial output drivers. Left low or unconnected, 5% pre-emphasis is added. Pulled high, 20% pre-emphasis is added.
CTRL0 CTRL1	33 27	Input (w/pull down)	**Mode Select.** These control pins control the format of the data on the transmit parallel bus. The parallel data may be in the form of 10-bit coded 8B/10B data in which case the data bypasses the on-chip 8b/10b encode logic on the TLK2541. The data may also be un-coded data in the form of 8 bits data plus a K-control bit in which case the data path makes use of the on-chip 8b/10b encode logic on the TLK2541.
			When the on-chip 8b/10b encode logic is utilized, there are additional modes available where the TLK2541 can properly maintain the Gigabit Ethernet IEEE802.3 IDLE patterns or properly maintain the ANSI FibreChannel EOF End Of Frame patterns.
			CTRL0 = 0, CTRL1 = 0: Raw 10 bit or 20 bit coded data CTRL0 = 0, CTRL1 = 1: 8 bit or 16 bit un-coded data GigEther mode CTRL0 = 1, CTRL1 = 0: 8 bit or 16 bit un-coded data FibreChannel Mode CTRL0 = 1, CTRL1 = 1: 8 bit or 16 bit un-coded data
RXCODE	40	Input (w/pull down)	**RXCODE.** This control pin controls the format of the data on the receive parallel bus. When RXCODE is low, the parallel data will be in the form of 10-bit coded 8B/10B data in which case the data bypasses the on-chip 8b/10b decode logic on the TLK2541. When RXCODE is high, the data will be un-coded data in the form of 8 bits data plus a K-status bit in which case the data path makes use of the on-chip 8b/10b decoder.
SYNCEN	28	Input (w/Pull-up)	**SYNCEN Enable.** When high, this pin enables the coma detect logic to byte-align the receiver to the location of the comma.

Table 1. Test Pin Descriptions

SIGNAL	PIN #	TYPE	DESCRIPTION
LCKREFN	30	Input (w/Pull-up)	**Lock to Reference.** When the LCKREFN pin is asserted active low, the tracking circuitry on the receiver Clock/Data Recovery (CDR) circuit is disabled and the recovered byte clock will become a buffered version of REFCLK.
LOOPEN	26	Input (w/Pull-down)	**Loop Enable**. When LOOPEN is active high, the internal loop-back path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUTTXP and DOUTTXN outputs are held in a high impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active.
PRBSEN	31	Input (w/Pull-down	**PRBS Test Enable.** When asserted high results of Pseudo Random Bit Stream (PRBS) tests can be monitored on the PRBSPASS pin. A high on PRBSPASS indicates that valid PRBS is being received.
TESTEN	32	Input (w/Pull-down)	**Test Mode Enable.** This pin should be left unconnected or tied low.

Table 2. Power Pin Descriptions

POWER	PIN#	TYPE	DESCRIPTION
VDD	2, 11, 22, 29, 42, 48, 59	Supply	**Digital logic power.** Provides power for all digital circuitry and Digital I/O Buffers.
VDDA	68, 69, 74	Supply	**Analog Power.** VDDA provides a supply reference for the high-speed analog circuits, receiver and transmitter
GROUND			
GNDA	65, 70, 73	Ground	**Analog Ground.** GNDA provides a ground reference for the high-speed analog circuits, RX and TX.
GND	7, 15, 20, 35, 41, 53, 60, 80	Ground	**Digital Logic Ground.** Provides a ground for the logic circuits and digital I/O buffers.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

			VALUE	UNIT
V_{DD}	Supply voltage(2)		–0.3 to 3	V
	Voltage range at TXD[0:19], ENABLE, TX_CLK, LOOPEN, PRBSEN, PRE, CTRL0, CTRL1, TXRATE, RXRATE, REFCLK, LCKREFN, TESTEN,RXCODE		–0.3 to 4	V
	Voltage range at any other terminal except above		–0.3 to V_{DD}+ 0.3	V
P_D	Package power dissipation		See Dissipation Rating Table	
T_{stg}	Storage temperature		–65 to 150	°C
	Electrostatic discharge	HBM	2	kV
		CDM	1.5	kV
T_A	Characterized free-air operating temperature range	PFP	–40 to 85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are stated with respect to network ground.

DISSIPATION RATINGS(1)

PACKAGE(2)	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PFP80(3)	5.01 W	42.9 mW/°C	2.69 W

(1) This data was taken using 2 oz trace and copper pad that is soldered directly to a JEDEC standard 4 layer 3 in × 3 in PCB.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) Standard JEDEC High-K board.

For more information, refer to TI application note PowerPAD™ Thermally Enhanced package, TI literature number SLMA002.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.3	2.5	2.7	V
I_{CC}	Supply current	Frequency = 1.25 Gbps, PRBS pattern		280		mA
		Frequency = 2.5 Gbps, PRBS pattern		310		
P_D	Power dissipation	Frequency = 1.25 Gbps, PRBS pattern		700		mW
		Frequency = 2.5 Gbps, PRBS pattern		775		
		Frequency = 2.6 Gbps, worst case pattern(1)			825	
	Low Power Mode current	TX_CLK Static, V_{DDA} and V_{DD} = Max			1	mA
	PLL startup lock time	V_{DD}, V_{DDC} = 2.3 V		0.1	0.4	ms
	Data acquisition time	Frequency = 1.25 Gbps or 2.5 Gbps, K28.5 D16.2 pattern (3 sigma values)			256	ns
T_A	Operating free-air temperature		–40		85	°C

(1) Worst case pattern is a pattern that creates a maximum transition density on the serial transceiver.

REFERENCE CLOCK (REFCLK)TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Minimum data rate	Typ–0.01%	100	Typ+0.01%	MHz
Frequency	Maximum data rate	Typ–0.01%	130	Typ+0.01%	MHz
Frequency tolerance		–100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Peak-to-peak			40	ps

TTL INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted), TTL signals: TXD[0:19], TX_CLK, LOOPEN, ENABLE, PRBS_EN, PRE , CTRL0, CTRL1, TXRATE, RXRATE, REFCLK, LCKREFN, TESTEN, RXCODE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	See Figure 2	1.7		3.6	V
V_{IL}	Low-level input voltage	See Figure 2			0.8	V
I_{IH}	Input high current	V_{DD} = MAX, V_{IN} = 2 V			40	µA
I_{IL}	Input low current	V_{DD} = MAX, V_{IN} = 0.4 V	–40			µA
C_I	Receiver input capacitance				4.5	pF
t_r	Rise time, TXD[0..19]	0.8 V to 1.7 V, C = 5 pF, See Figure 2		1		ns
t_f	Fall time, TX_CLK, TXD[0..19]	1.7 V to 0.8 V, C = 5 pF, See Figure 2		1		ns
t_{su}	TXD[0:19], setup to ↑ TX_CLK	See Figure 2	1.5			ns
t_h	TXD[0:19], hold to ↑ TX_CLK	See Figure 2	0.5			ns

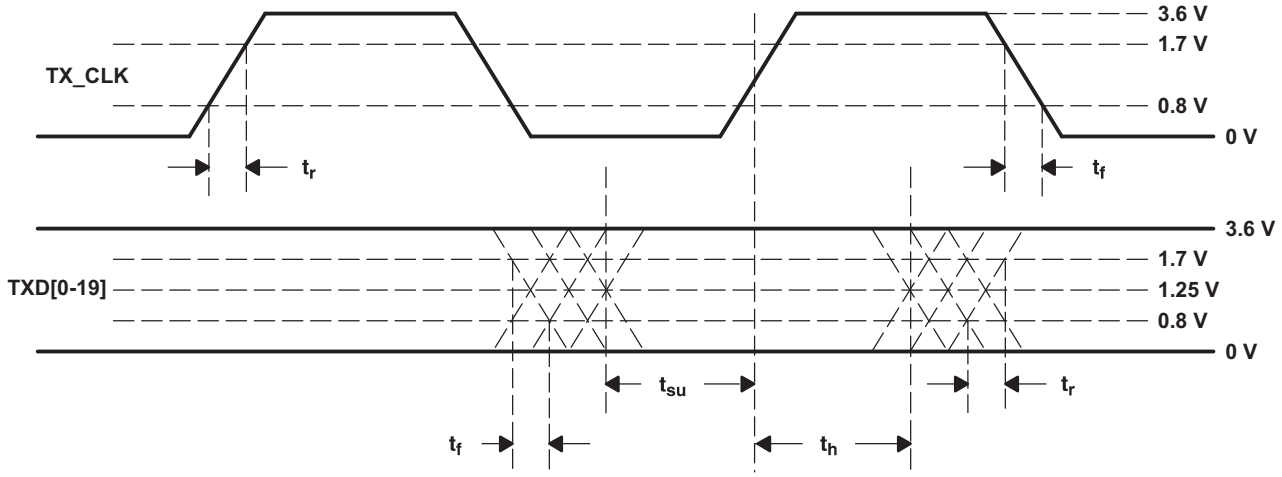


Figure 2. TTL Data Input Valid Levels for AC Measurements

TTL OUTPUT SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA, V_{DD} = MIN	2.10	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, V_{DD} = MIN	GND	0.25	0.5	V
$t_{r(slew)}$	Slew rate (rising), magnitude of RX_CLK, RXD[0:19]	0.8 V to 2 V, C = 5 pF, See Figure 3	0.5			V/ns
$t_{f(slew)}$	Slew rate (falling), magnitude of RX_CLK, RXD[0:19]	0.8 V to 2 V, C = 5 pF, See Figure 3	0.5			V/ns
t_{su}	RXD[0:19] setup to ↑ RX_CLK	50% voltage swing, TX_CLK = 100 MHz, See Figure 3	2.5			ns
		50% voltage swing, TX_CLK = 130 MHz, See Figure 3	2.5			
t_h	RXD[0:19] hold to ↑ RX_CLK	50% voltage swing, TX_CLK = 100 MHz, See Figure 3	1.5			ns
		50% voltage swing, TX_CLK = 130 MHz, See Figure 3	1.5			
	Duty Cycle, RX_CLK	See Figure 3	45%	50%	55%	

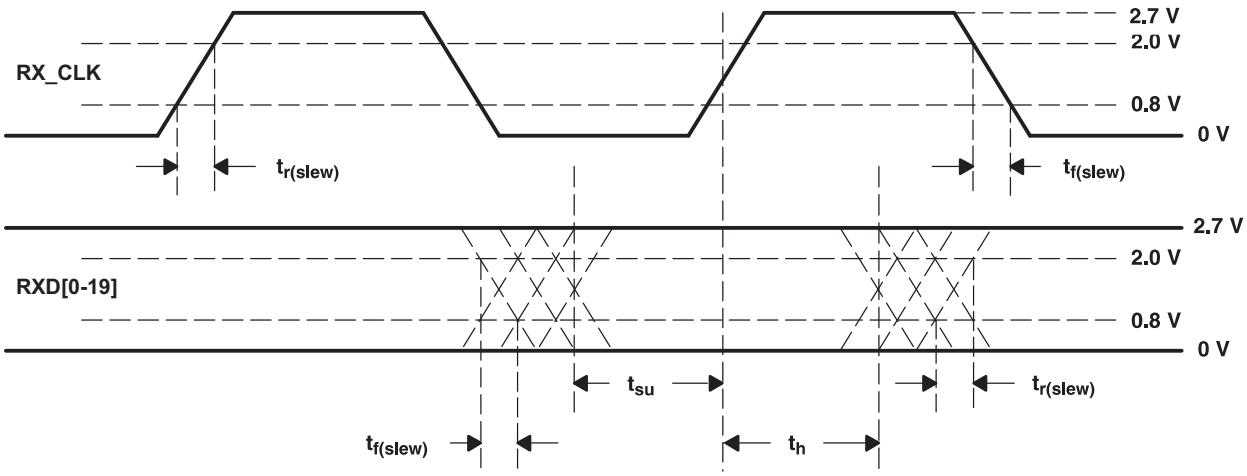


Figure 3. TTL Data Output Valid Levels for AC Measurements

TRANSMITTER/RECEIVER CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{OD(p)}$	Preemphasis V_{OD}, direct, $V_{OD(p)}$ = |VTXP – VTXN|	R_t = 50Ω, PREM = high, dc-coupled, See Figure 4	750	913	1075	mV
		Rt = 50Ω, PREM = low, dc-coupled, See Figure 4	700	850	1000	
$V_{OD(pp\_p)}$	Differential peak-to-peak output voltage with preemphasis	R_t = 50Ω, PREM = high, dc-coupled, See Figure 4	1500	1825	2150	mV_{PP}
		Rt = 50Ω, PREM = low, dc-coupled, See Figure 4	1400	1700	2000	
$V_{OD(d)}$	Deemphais output voltage, |VTXP–VTXN|	R_t = 50Ω, dc-coupled, See Figure 4	500	600	800	mV
$V_{OD(pp\_d)}$	Differential, peak-to-peak output voltage with deemphasis	R_t = 50Ω, dc-coupled, See Figure 4	1000	1300	1600	mV_{PP}
$V_{(cmt)}$	Transmit common mode voltage range, (VTXP + VTXN)/2	R_t = 50Ω, See Figure 4	1000	1250	1400	mV
V_{ID}	Receiver input voltage differential, |VRXP – VRXN|		200		1600	mV
$V_{(cmr)}$	Receiver common mode voltage range, (VRXP + VRXN)/2		1000	1250	2250	mV
	Ci Receiver input capacitance				2	pF
	Serial data total jitter (peak-to-peak)	Differential output jitter at 2.5 Gbps, Random *12 + deterministic, Based on K28.5/K28.5 pattern			.32	UI(1)
		Differential output jitter at 1.25 Gbps, Random*12 + deterministic, PRBS Pattern			0.19	
	Serial data total jitter (Random)	Random Jitter (RMS)			.016	UI
t_t, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50Ω, C_L = 5 pF, See Figure 4		150		ps
	Jitter tolerance, Total jitter at serial input	Differential input jitter, random + deterministic, PRBS pattern at zero crossing at 1.25 Gbps			.75	UI
	Jitter tolerance, Deterministic jitter at serial input	Differential input jitter, deterministic, PRBS pattern at zero crossing at 1.25 Gbps			.462	UI
	Jitter tolerance, Total jitter at serial input	Differential input jitter, random + deterministic, PRBS pattern at zero crossing at 2.5 Gbps			.60	UI
	Jitter tolerance, Deterministic jitter at serial input	Differential input jitter, deterministic, PRBS pattern at zero crossing at 2.5 Gbps			.37	UI
$t_{d(Tx\ latency)}$	Tx latency with Coding Off	See Figure 6	50		106	bits
	Tx latency with Coding On		70		126	
$t_{d(Rx\ latency)}$	Rx latency for Full Rate	See Figure 9	81		100	bits
	Rx latency for Half Rate		69		83	

(1) UI is the time interval of one serialized bit.

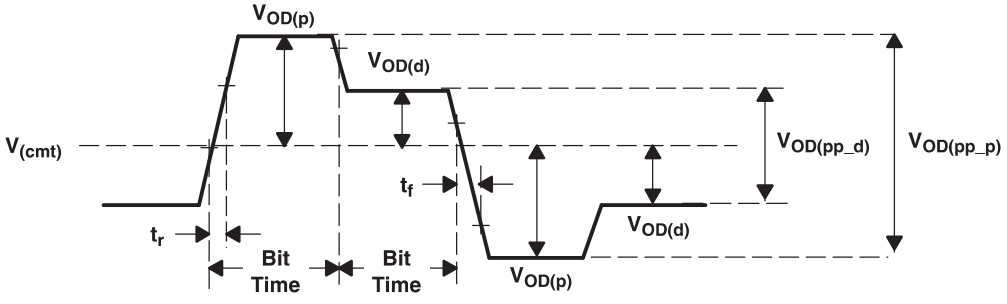


Figure 4. Differential and Common-Mode Output Voltage Definitions

DETAILED DESCRIPTION

TRANSMIT INTERFACE

The TLK2541 offers four modes of operation for the transmit data path. The TLK2541 can operate as a 10 bit SERDES at 10 times the rate of REFCLK or as a 20 bit SERDES at 20 times the rate of REFCLK. At either rate, the data may be serialized exactly as presented on the parallel bus or it may be coded into 8B/10B data codes by way on an integrated 8B/10B encoder.

TRANSMIT DATA BUS

At full data rate, The transmitter portion registers valid incoming 20-bit wide data (TXD[0:19]) on the rising edge of the TX_CLK. The data is then serialized and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (REFCLK) by a factor of 10 times, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register which transmits data on both the rising and falling edges of the internal bit clock, providing a serial data rate that is 20 times the input clock. Data is transmitted LSB TXD[0] first. If the 8B/10B encoder is enabled, the data is latched as 16 bits of data plus two bits of control. The lower order byte is latched on TXD[0:7] and the higher order byte is latched on TXD[8:15]. Bit TXD[16] controls whether the lower order byte is coded as a Dx.y data word or a Kx.y control word. Bit TXD[17] controls whether the higher order byte is coded as a Dx.y data word or a Kx.y control word. Bits TXD[18] and TXD[19] are ignored.

At half data rate, The transmitter portion registers valid incoming 10-bit wide data (TXD[0:9]) on the rising edge of the TX_CLK. The data is then serialized and transmitted sequentially over the differential high-speed I/O channel. Bits TXD[10:19] are ignored. The clock multiplier multiplies the reference clock (REFCLK) by a factor of 5 times, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register which transmits data on both the rising and falling edges of the bit clock, providing a serial data rate that is 10 times the input clock. Data is transmitted LSB (TXD[0]) first. If the 8B/10B encoder is enabled, the data is latched as 8 bits of data plus one bit of control. The lower order byte is latched on TXD[0:7]. Bit TXD[16] controls whether the lower order byte is coded as a Dx.y data word or a Kx.y control word. Bits TXD[8:15] and TXD[17:19] are ignored. The data and clock signals must be properly aligned as shown in Figure 5. Detailed timing information can be found in the electrical characteristics table.

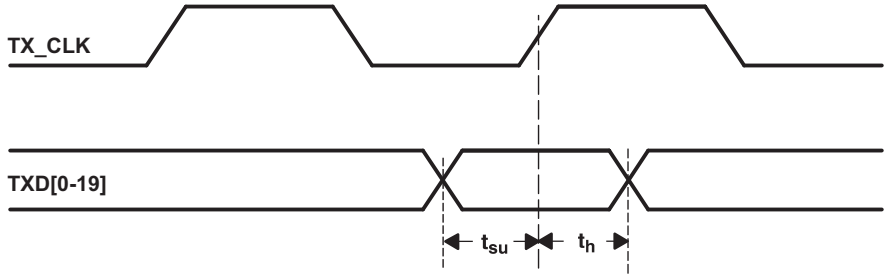


Figure 5. Transmit Timing Waveform

Transmit Rate Select

The TLK2541 has two ranges of operation. The TLK2541 may be used to serialize 20 bits of data at a data rate of 20 times the reference clock, or the TLK2541 may be used to serialize 10 bits of data at a rate of 10 times the reference clock. In either case, the reference clock must be in the range of 100 to 130 MHz, allowing the TLK2541 to be used as a 10-bit serializer at a rate of 1 to 1.3 Gbps or as a 20-bit serializer at a rate of 2 to 2.6 Gbps. The control pin TXRATE selects the range of operation for the TLK2541 serializer.

When TXRATE is low, the TLK2541 serializes the 10 bit data on TXD[0:9] at a rate of 10 times the reference clock. Bits TXD[10:19] is ignored. If the 8B/10B encoder is enabled, then bits TXD[0:7] is encoded into a 10 bit code word and bit TXD[16] controls whether the code is a Dx.y code if TXD[16] is low or a Kx.y code if TXD[16] is high. Bit TXD[9] is ignored.

When TXRATE is high, the TLK2541 serializes the 20 bit data on TXD[0:19] at a rate of 20 times the reference clock. Bit TXD[0] is the first bit serialized. If the 8B/10B encoders are enabled, then bits TXD[0:7] is encoded into the lower order 10 bit code word and bits TXD[8:15] is encoded into the higher order 10 bit code word. The lower order code word is serialized first. Bit TXD[16] controls whether the lower order code is a Dx.y code if TXD[16] is low or a Kx.y code if TXD[16] is high. Bit TXD[17] controls whether the higher order code is a Dx.y code if TXD[17] is low or a Kx.y code if TXD[17] is high. Bits TXD[18] and TXD[19] is ignored.

When TXRATE is high, it is expected (but not required) that a K28.5 code such as that used in a Gigabit Ethernet IDLE or a FibreChannel ordered set be present on the lower order byte. This is because at the higher data rate the parallel bus is two bytes wide, and if the receiver is also a TLK2541 with a two-byte wide parallel bus then the receiver must determine which byte to output on the lower order byte of the receive parallel bus. The TLK2541 receiver expects the K28.5 code to be present on the lower order byte and thus the receiver chooses a 20 bit deserialization boundary such that the K28.5 is present on the lower order byte.

TRANSMISSION LATENCY

The data transmission latency of the TLK2541 is defined as the delay from the initial 20-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies. The minimum transmit latency $t_{d(Tx\ latency)}$ is 50 bit times; the maximum is 86 bit times when 8b/10b coding is off. The minimum transmit latency $t_{d(Tx\ latency)}$ is 70 bit times; the maximum is 106 bit times when 8b/10b coding is on. Figure 6 illustrates the timing relationship between the transmit data bus, the TX_CLK, and the serial transmit terminals.

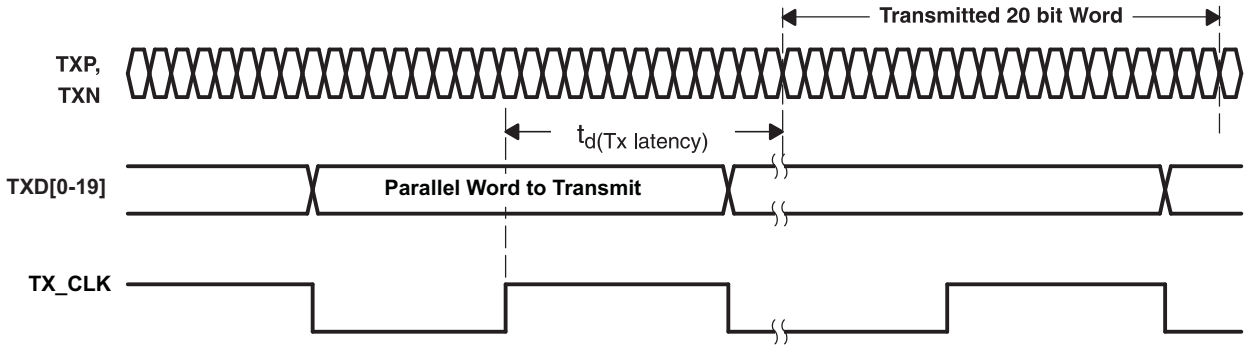


Figure 6. Transmission Latency

Optional 8-BIT/10-BIT ENCODER

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiving PLL has a minimal number of transitions to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The TLK2541 uses the 8-bit/10-bit encoding algorithm that is used by fibre channel and gigabit ethernet. This is transparent to the user, as the TLK2541 internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

The 8-bit/10-bit encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transmission characteristics. Since the TLK2541 is a 16-bit wide interface, the data is split into two 8-bit wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependent upon two additional input signals are presented on pins TXD[16] and TXD[17]. See Table 3.

Table 3. Transmit Data Controls

TXD[16]	TXD[17]	16 BIT PARALLEL INPUT FULL RATE WITH 8B/10B CODING	
0	0	Valid data on TXD[0:7],	Valid data TXD[8:15]
0	1	Valid data on TXD[0:7],	K code on TXD[8:15]
1	0	K code on TXD[0:7],	Valid data on TXD[8:15]
1	1	K code on TXD[0:7],	K code on TXD[8:15]

TXD[16]	8 BIT PARALLEL INPUT HALF RATE WITH 8B/10B CODING
0	Valid data on TXD[0:7]
1	K code on TXD[0:7]

8B/10B Bypass Mode

When control pin CTRL0 and CTRL1 are both held low, the TLK2541 will bypass the integrated 8B/10B encode logic and will serialize the parallel data as it is presented to the parallel bus without coding or modification. Data is serialized least-significant bit first, so bit TXD[0] is the first bit to be transmitted and bit TXD[19] is the last bit transmitted. For all other combinations of CTRL0 and CTRL1, the data path includes the integrated 8B/10B encode logic. In this mode, bits TXD[0:7] are presented to the lower order encoder, and bit TXD[16] controls whether this byte is coded as Dx.y or as Kx.y. If TXD[16] is low, then the data is coded as Dx.y. If TXD[16] is high, then the data is coded as Kx.y. Bits TXD[8:15] are presented to the higher order encoder, and bit TXD[17] controls whether the data is coded as Dx.y or Kx.y. When TXD[16] or TXD[17] are used to generate Dx.y codes, all possible combinations of the data codes are valid. However, there are only 12 valid Kx.y codes defined by the 8B/10B coding definition. To generate one of these valid K codes, the proper data bit combination must be presented on the data bus. For example, to generate a K28.5 on the lower order byte, bit TXD[16] is set to logic '1' and bits TXD[0:7] are set to '10111100'. If the K control bit is set while the data bus is set for an undefined Kx.y code (such as K0.9), then the output of the encoder is undefined and not specified to be valid. When either CTRL0 or CTRL1 are set to logic '1', data presented on the parallel bus TDX[0:17] is presented to the 8B/10B encoders. TXD[18] and TXD[19] are ignored. When both CTRL0 and CTL1 are set to logic '1' the data presented on the TXD[0:17] bus is encoded and serialized, allowing the use of the TLK2541 for proprietary protocols built around the 8B/10B coding standard. For Ethernet or FibreChannel protocols, the Gigabit Ethernet or FibreChannel modes may be better suited for the application.

Gigabit Ethernet IDLE Correction Mode

The IDLE pattern described in the IEEE802.3 clause 36 specification requires the IDLE pattern to be generated as either K28.5 D5.6 or as K28.5 D16.2 depending on the state of the 8B/10B current running disparity at the time that the IDLE pattern is sent. If the integrated 8B/10B encoders are used, then there is no way for the host device controlling the TLK2541 TXD[0:19] bus to know whether to send the D5.6 code or the D16.2 code on the upper order byte. If the TLK2541 is to be used to generate valid Ethernet IDLE patterns while using the on board 8b/10b encoder, then the Gigabit Ethernet IDLE Correction mode should be enabled. In this mode, a K28.5 D16.2 idle may be presented to the transmit parallel bus for all idles, and the TLK2541 substitutes a D5.6 in place of the D16.2 on those occasions where the current running disparity requires that a K28.5 D5.6 is the proper IDLE to be generated. This mode is enabled when CTRL0 is 0 and CTRL1 is high.

FibreChannel End Of Frame Correction Mode

The EOF pattern described in the ANSI FC-PH FibreChannel specification requires the EOF pattern to be generated as either K28.5 D21.4 D21.x D21.x or as K28.5 D21.5 D21.× D21.x depending on the state of the 8B/10B current running disparity at the time that the EOF pattern is sent. If the integrated 8B/10B encoders are used, then there is no way for the host device controlling the TLK2541 TXD[0:19] bus to know whether to send one EOF code or the other EOF code. If the TLK2541 is to be used to generate valid FibreChannel EOF patterns while using the on board 8b/10b encoder then the FibreChannel EOF correction mode should be enabled. In this mode, a K28.5 D21.4 D21.x D21.x EOF is presented to the transmit parallel bus for all EOF ordered sets, and the TLK2541 substitutes a D21.5 in place of the D21.4 on those occasions where a K28.5 D21.5 D21.× D21.× is the proper EOF to be generated. This mode is enabled when CTRL0 is 1 and CTRL1 is 0. The EOF correction mode also corrects the EOF-invalid ordered sets by correcting a K28.5 D10.5 D21.× D21.× ordered set to be a K28.5 D10.4 D21.× D21.× ordered set when necessary.

PRBS Generator

The TLK2541 has a built-in 2^7-1 PRBS (pseudo random bit stream) function. When the PRBSEN terminal is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (bit error rate tester), the receiver of another TLK2541, or looped back to the receive input. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

Parallel-to-Serial

The parallel-to-serial shift register takes in the 20-bit wide data word multiplexed from the two parallel 8-bit/10-bit encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the REFCLK input frequency. The LSB (TXD[0]) is transmitted first.

High-Speed Data Output

The high-speed data output driver consists of a voltage mode logic (VML) differential pair optimized for a 50-Ω impedance environment. The magnitude of the differential pair signal swing is compatible with pseudo emitter coupled logic (PECL) levels when ac-coupled. The line can be directly-coupled or ac-coupled. See Figure 11 and Figure 12 for termination details. The outputs also provide preemphasis to compensate for ac loss when driving a cable or PCB backplane trace over a long distance (see Figure 7). The level of pre-emphasis is controlled by PRE as shown in Table 4.

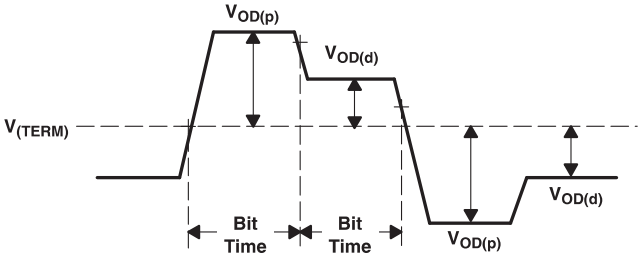


Figure 7. Output Voltage Under Pre-emphasis (|VTXP–VTXN|)

Table 4. Programmable Pre-emphasis

PRE	PRE-EMPHASIS LEVEL(%) $V_{OD(P)}$, $V_{OD(D)}$ (1)
0	5%
1	20%

(1) $V_{OD(p)}$: Voltage swing when there is a transition in the data stream
$V_{OD(d)}$: Voltage swing when there is no transition in the data stream.

RECEIVE INTERFACE

The receiver portion of the TLK2541 accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit locks to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream. The recovered clock is divided down to output a receive word clock that is output on RX_CLK. The parallel data is presented on the parallel output bus according to four modes of operation. The TLK2541 can operate as a 10 bit SERDES at 10 times the rate of REFCLK or as a 20 bit SERDES at 20 times the rate of REFCLK. At either rate, the data may be deserialized, byte aligned and output exactly as it is captured from the serial inputs or it may be decoded into data bytes by way on an integrated 8B/10B decoder.

Receive Data Bus

At full data rate, the receiver portion locks to an incoming serial data stream and deserializes the data into 20-bit wide data words and outputs them on RXD[0:19] along with the RX_CLK. RX_CLK is aligned with the rising edge in the center of the output data word. The first data bit received is output on RXD[0]. If the 8B/10B decoder is enabled, the data is output as 16 bits of data plus two bits of status. The lower order byte is output on RXD[0:7] and the higher order byte is output on RXD[8:15]. Bit RXD[16] indicates whether the lower order byte was decoded as a Dx.y data word or a Kx.y control word. Bit RXD[17] indicates whether the higher order byte was decoded as a Dx.y data word or a Kx.y control word. Bits RXD[18] and RTXD[19] are high impedance.

At half data rate, the receiver portion locks to an incoming serial data stream and deserializes the data into 10-bit wide data words and outputs them on RXD[0:9] along with the RX_CLK. RX_CLK is aligned with the rising edge

in the center of the output data word. The first data bit received is output on RXD[0]. If the 8B/10B encoder is enabled, the data is output as 8 bits of data plus one bit of status. The lower order byte is output on RXD[0:7]. Bit RXD[16] indicates whether the lower order byte was decoded as a Dx.y data word or a Kx.y control word. Bits RXD[8:15] and RXD[17:19] and are high impedance The data and clock signals are aligned as shown in Figure 8. Detailed timing information can be found in the switching characteristics table.

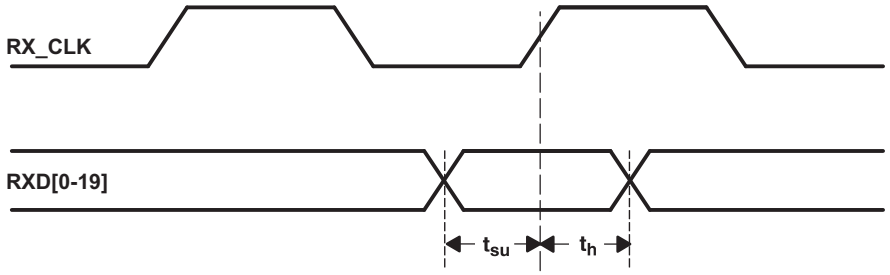


Figure 8. Receive Timing Waveform

Data Reception Latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies. The minimum receive latency $t_{d(Rx\ latency)}$ is 81 bit times; the maximum is 93 bit times for full rate operation. The minimum receive latency $t_{d(Rx\ latency)}$ is 69 bit times; the maximum is 81 bit times for half rate operation. Figure 9 illustrates the timing relationship between the serial receive terminals, the recovered word clock (RX_CLK), and the receive data bus.

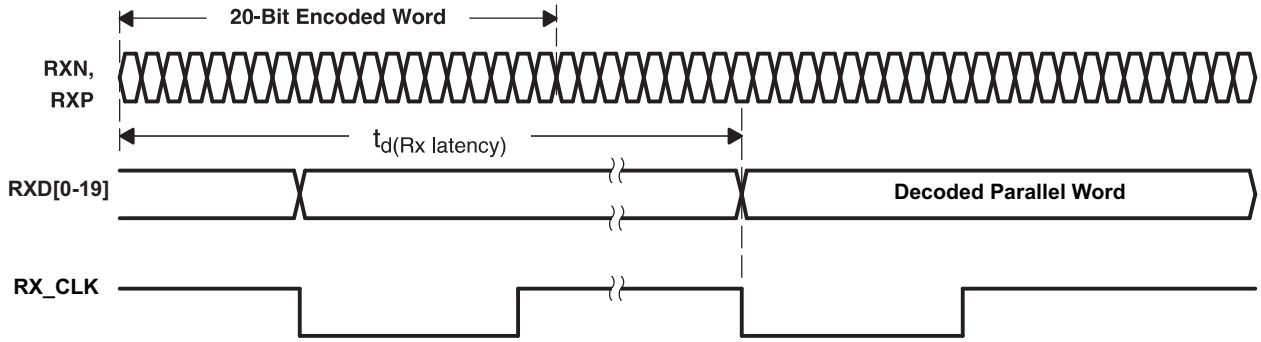


Figure 9. Receiver Latency

Serial-to-Parallel

Serial data is received on the RXP and RXN terminals. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within 200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10-bit wide parallel data is then multiplexed and fed into two separate 8-bit/10-bit decoders where the data is then synchronized to the incoming data stream word boundary by detection of the comma 8-bit/10-bit synchronization pattern.

Comma Detect and Optional 8-Bit/10-Bit Decoding

The TLK2541 has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10 bit encoded data (half of the 20-bit received word) back into 8 bits. The comma detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a method is needed to recognize the byte boundary. This is accomplished through the use of a synchronization pattern. This is a unique pattern of 1's and 0's that either cannot occur as part of valid data, or is a pattern that repeats at defined intervals. The

8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma detect circuit on the TLK2541 to align the received serial data back to its original byte boundary. The decoder detects the comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding; the comma is mapped into the LSB. The decoder then converts the data back into 8-bit data. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RX_CLK) and output valid on the rising edge of the RX_CLK.

Since the TLK2541 must determine which byte of data belongs on the lower order byte of the parallel output bus, the K code that contains a comma pattern is chosen to be output on the lower order byte. Protocols such as Gigabit Ethernet or Fibre Channel are defined such that the K28.5 is only present on 20 or 40 bit boundaries.

NOTE

The TLK2541 only achieves byte alignment on the 0011111 comma.

Decoding provides two additional status signals, RXD[16] and pin RXD[17]. When RXD[16] is high , an 8-bit/10-bit K code was received and the specific K code is presented on the data bits RXD[0:7]; otherwise, an 8-bit/10-bit D code was received. When RXD[17] is high, an 8-bit/10-bit K code was received and the specific K-code is presented on data bits RXD[8:15]; otherwise, an 8-bit/10-bit D code was received (see Table 5). The valid K codes the TLK2541 decodes are provided in Table 6. An error detected on either byte, including K codes not in Table 6, causes that byte only to indicate a K0.0 code on the RXD[16] or RXD[17] and associated data pins, where K0.0 is known to be an invalid 8-bit/10-bit code.

8B/10B Decode Bypass

When control pin RXCODE is held low, the TLK2541 will bypass the integrated 8B/10B decode logic and will present the raw 20 bit deserialized data on the output pins RXD[0:19]. If RXCODE is high, then the deserialized data will be decoded by the integrated 8B/10B decoder and the decoded data will be output on the output pins RXD[0:19].

RX Rate Select

The TLK2541 receiver has two ranges of operation. The TLK2541 may be used to deserialize 20 bits of data at a data rate of 20 times the reference clock, or the TLK2541 may be used to deserialize 10 bits of data at a rate of 10 times the reference clock. In either case, the reference clock must be in the range of 100 to 130 MHz, allowing the TLK2541 to be used as a 10-bit deserializer at a rate of 1 to 1.3 Gbps or as a 20-bit deserializer at a rate of 2 to 2.6 Gbps. The control pin RXRATE selects the range of operation for the TLK2541 deserializer. The recovered byte clock is always in the range of 100 to 130 MHz. The data rate range for the TLK2541 receiver may be selected independently of the TLK2541 transmitter. The TLK2541 may receive a data stream that is half the rate of the transmitted data stream, or twice that of the transmitted data stream, or the same as the transmitted data stream. At whatever data rate is chosen for the receiver, the Clock/Data Recovery (CDR) function in the TLK2541 receiver may lock to and track an incoming data stream that is as much as ± 200 ppm away from the nominal data rate as referenced by the REFCLK to the TLK2541.

When RXRATE is low, the TLK2541 deserializes the data stream into a 10 bit data byte and output it on RXD[0:9]. Bits RXD[10:19] are high-impedance. If the 8B/10B decoder is enabled, then the 10 bit deserialized data is decoded and output on bits RXD[0:7], and bit RXD[16] indicates whether the code is a Dx.y code if RXD[16] is low or a Kx.y code if RXD[16] is high. Bits RXD[8:15] and RXD[17:19] are high-impedance.

When RXRATE is high, the TLK2541 deserializes the data stream into a 20 bit data word and output it on bits RXD[0:19]. Bit RXD[0] is the first bit received. If the 8B/10B decoders are enabled, then bits RXD[0:7] outputs the lower order 10 bit deserialized code word and bits RXD[8:15] output the higher order 10 bit deserialized code word. The lower order code word is the first byte received. Bit RXD[16] indicates whether the lower order code is a Dx.y code if RXD[16] is low or a Kx.y code if RXD[16] is high. Bit RXD[17] indicates whether the higher order code is a Dx.y code if RXD[17] is low or a Kx.y code if RXD[17] is high. Bits RXD[18] and RXD[19] are high impedance.

When RXRATE is high, a K28.5 code such as that used in a Gigabit Ethernet IDLE or a FibreChannel ordered set is output on the lower order byte. This is because at the higher data rate the parallel bus is two bytes wide, and the receiver must determine which byte to output on the lower order byte of the receive parallel bus. The TLK2541 receiver expects the K28.5 code to be present on the lower order byte and thus the receiver chooses a 20 bit deserialization boundary such that the K28.5 is present on the lower order byte.

Table 5. Receive Status Signals

RXD[16]	RXD[17]	DECODED 20 BIT OUTPUT FULL RATE WITH 8B/10B CODING
0	0	Valid data on RXD[0:7], Valid data RXD[8:15]
0	1	Valid data on RXD[0:7], K code on RXD[8:15]
1	0	K code on RXD[0:7], Valid data on RXD[8:15]
1	1	K code on RXD[0:7], K code on RXD[8:15]

RXD[16]	DECODED 20 BIT OUTPUT HALF RATE WITH 8B/10B CODING
0	Valid data on RXD[0:7]
1	K code on RXD[0:7]

Table 6. Valid K Characters

K CHARACTER	RECEIVE DATA BUS (RXD[0:7]) OR (RXD[8:15])
K28.0	000 11100
K28.1(1)	001 11100
K28.2	010 111000
K28.3	011 111000
K28.4	100 11100
K28.5(1)	101 11100
K28.6	110 111001
K28.7(1)	111 11100
K23.7	111 101111
K27.7	111 110111
K29.7	111 111011
K30.7	111 111101

(1) Should only be present on RXD[7–0] when in running disparity < 0.

Lock to Reference

When the LCKREFN pin is asserted (active low), the tracking circuitry on the receiver Clock/Data Recovery (CDR) circuit is disabled, and the recovered byte clock becomes a buffered version of REFCLK. If there is not a valid serial data stream while the receiver is attempting to lock onto and track a serial data stream, then it is possible for the recovered byte clock to drift to a frequency above or below the desired data rate by as much as 2000 ppm depending on noise components of the invalid input serial data stream. The assertion of LCKREFN, while there is no valid incoming serial data, would ensure that the recovered byte clock does not drift away from REFCLK. The use of LCKREFN is not required to help the receiver lock onto incoming serial data, and the use of LCKREFN does not speed the process of locking onto data once LCKREFN is released.

Power Down Mode

When the reference clock (REFCLK) is held static, the TLK2541 goes into power-down mode. In power-down mode, the serial transmit pins (TXN and TXP) , and the receive data bus pins (RXD[0:19]) go into a high-impedance state. When the reference clock begins to toggle at a rate approaching its minimum recommended operating frequency then the TLK2541 will go through its power-on reset procedure.

PRBS Verification

The TLK2541 also has a built-in BERT function in the receiver side that is enabled by the PRBSEN. It can check for errors and report the errors by forcing the PRBSPASS terminal low.

Reference Clock Input

The reference clock (REFCLK) is an external input clock that sets the rate of the transmitted serial data stream. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. In full rate mode, the internal serialization bit clock is frequency-locked to the input clock and used to clock out the serial transmit data on both its rising and falling edges, providing a serial data rate that is 20 times the input clock.

Operating Frequency Range

The TLK2541 can operate at a serial data rate from 1.0 Gbps to 1.3 Gbps or 2.0 to 2.6 Gbps. To achieve these serial rates, REFCLK must be within 100 MHz to 130 MHz. The frequency accuracy of REFCLK is expected to be within 100 PPM of the desired rate. The transmit path data rate will be set by REFCLK and the receive path data rate is expected to be within 200 PPM of the transmit path data rate.

Testability

The TLK2541 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable terminal allows for all circuitry to be disabled so that a quiescent current test can be performed. The PRBS function allows for BIST (built-in self-test).

Loopback Testing

The transceiver can provide a self-test function by enabling (LOOPEN) the internal loop-back path. Enabling this terminal causes serial-transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high impedance state during the loopback testing.)

Built-In Self-Test (BIST)

The TLK2541 has a BIST function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the PRBSPASS terminal. The PRBS generation and verification can operate at either full rate or half rate, but both PRBS generation and verification must be at the same rate or PRBSPASS will report an error condition.

Power-On Reset

Upon application of minimum valid power or upon application of a minimum toggling reference clock, the TLK2541 generates a power-on reset. During the power-on reset the RXD[0:19] and serial output signal terminals go to a high impedance state. The RX_CLK is held low. The length of the power-on reset cycle is dependent upon the input frequency, but is less than 1 ms.

APPLICATION INFORMATION

Figure 10. External Component Interconnection

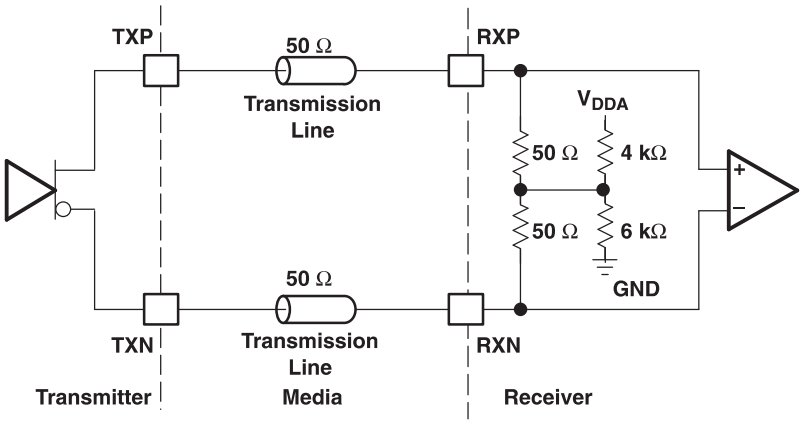


Figure 11. High-Speed I/O Directly-Coupled Mode

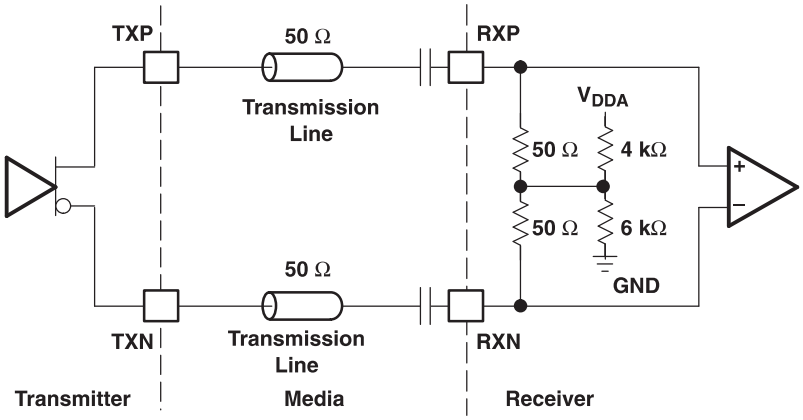


Figure 12. High-Speed I/O AC-Coupled Mode

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK2541PFP	LIFEBUY	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK2541	
TLK2541PFPG4	LIFEBUY	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK2541	
TLK2541PFPR	LIFEBUY	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK2541	
TLK2541PFPRG4	LIFEBUY	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLK2541	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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