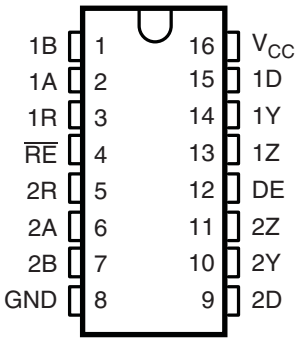
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

Check for Samples: SN7534050, SN7534051

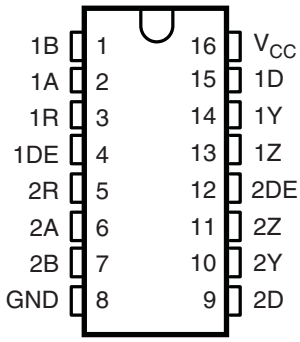
FEATURES

- **Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11**
- **Operate From Single 5-V Power Supply**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Sensitivity: ±200mV**
- **Receiver Input Impedance: 12 kΩ Min**
- **Driver 3-State Outputs**
- **Receiver 3-State Outputs (SN7534050 Only)**

SN7534050...N OR NS PACKAGE
(TOP VIEW)



SN7534051...N OR NS PACKAGE
(TOP VIEW)



DESCRIPTION

The SN7534050 and SN7534051 dual differential drivers and receivers are monolithic integrated circuits designed to meet the requirements of ANSI standards TIA/EIA-422-B and ITU Recommendations V.11.

The driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on transmission bus line.

The SN7534050 combines dual 3-state differential drivers and dual 3-state differential input receivers. The drivers and receivers have active-high and active-low enables, respectively which can be externally connected together to function as direction control. SN7534051 drivers each have an individual active-high enable.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–20°C to 85°C	PDIP – N	Tube of 25	SN7534050N	SN7534050N
	SOP – NS	Tube of 50	SN7534050NS	SN7534050
		Reel of 2000	SN7534050NSR	SN7534050
	PDIP – N	Tube of 25	SN7534051N	SN7534051N
	SOP – NS	Tube of 50	SN7534051NS	SN7534051
		Reel of 2000	SN7534051NSR	SN7534051

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Table 1. SN7534050, SN7534051 Each Driver(1)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

Table 2. SN7534050 Each Receiver(1)

DIFFERENTIAL INPUTS, A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

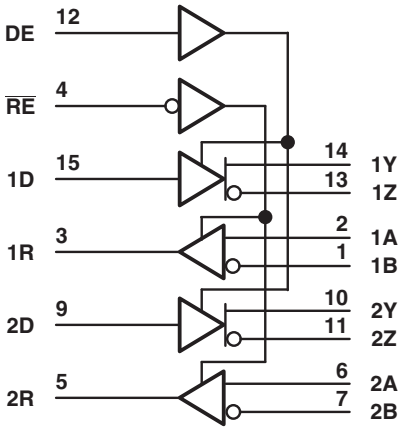
Table 3. SN7534051 Each Receiver(1)

DIFFERENTIAL INPUTS, A–B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

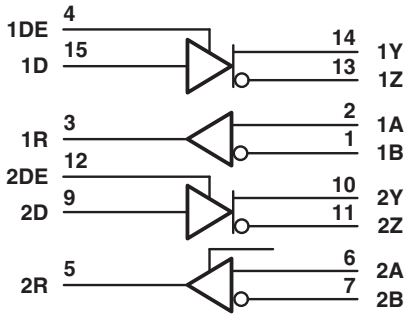
(1) H = high level, L = low level, ? = indeterminate

LOGIC DIAGRAMS

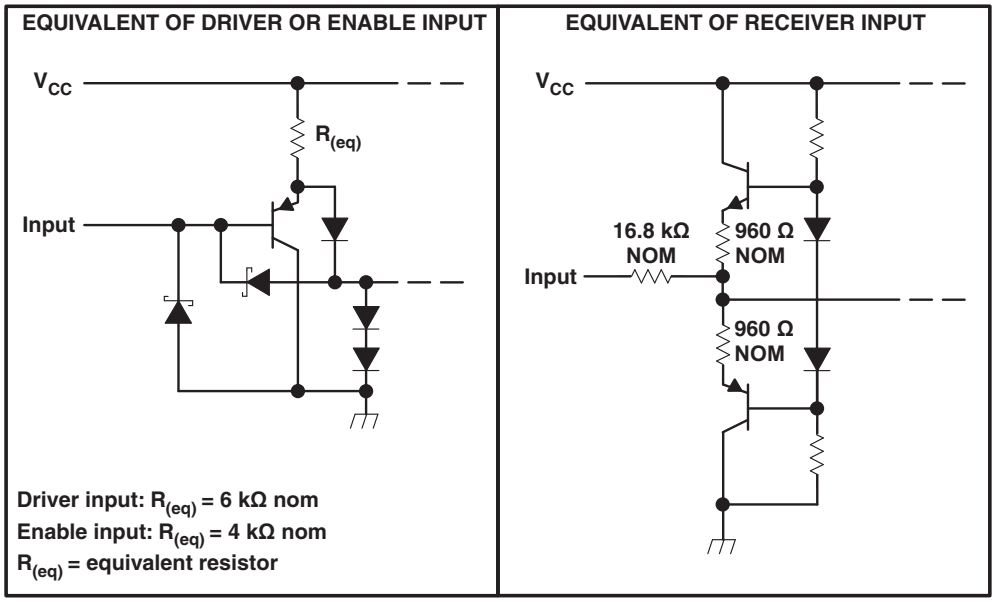
SN7534050



SN7534051

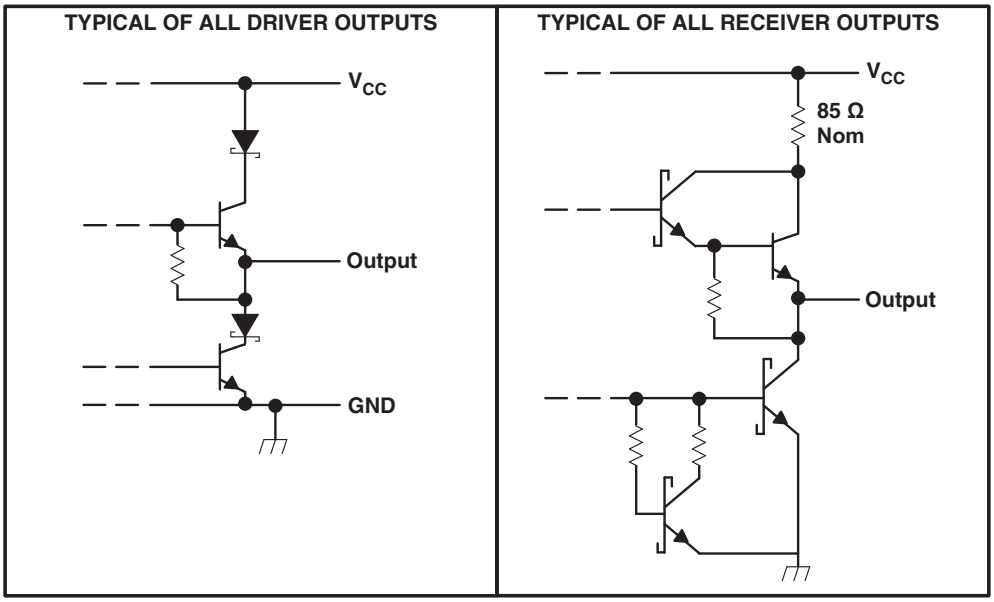


SCHEMATIC OF INPUTS



All resistor values are nominal.

SCHEMATIC OF OUTPUTS



All resistor values are nominal.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			7	V
V_I	Input voltage	DE, $\overline{RE}$, D inputs		7	V
V_i	Receiver input voltage	A or B inputs		±25	V
V_{ID}	Receiver differential output voltage(3)			±25	V
V_O	Driver output voltage range		–10	15	V
I_{OL}	Receiver low-level output current			50	mA
θ_{JA}	Package thermal impedance(4)	N package		66	°C/W
		NS package		68	
	Operating free-air temperature range		–20	85	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature, 1.6 mm (1/16 in) from case for 10 s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages, except differential input voltage, are with respect to the network GND.
(3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.
(4) The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	DE, $\overline{RE}$, D	2			V
V_{IL}	Low-level input voltage	DE, $\overline{RE}$, D			0.8	V
V_{IC}	Common-mode input voltage(1)	Receiver			±7	V
V_{ID}	Differential input voltage	Receiver			±12	V
I_{OH}	High-level output current	Driver			40	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			–40	mA
		Receiver			16	mA
T_A	Operating free-air temperature		–20		85	°C

(1) Refer to TIA/EIA-422-B for exact conditions.

DRIVER SECTION

Electrical Characteristics

over recommended supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –20 mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			1.1		V
V_{OD1}	Differential output voltage	I_O = 0 mA		1.5		6	V
V_{OD2}	Differential output voltage(2)	R_L = 100 Ω,	See Figure 1	2			V
ΔV_{OD}	Change in magnitude of differential output voltage(2)	R_L = 100 Ω,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage(2)	R_L = 100 Ω,	See Figure 1			±3	V
ΔV_{OC}	Change in magnitude of differential common-mode voltage(2)	R_L = 100 Ω,	See Figure 1			±0.4	V
I_{off}	Output current with power off(2)	V_{CC} = 0 V	V_O = 6 V			100	µA
		V_{CC} = 0 V	V_O = –0.25 V			–100	µA
I_{OZ}	High-impedance-state output current	V_O = –0.25 V to 6 V				±100	µA
I_{IH}	High-level input current	V_I = 2.7 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–100	µA
I_{OS}	Short-circuit output current(2) (3)	V_O = V_{CC} or GND		–30		–150	mA
I_{CC}	Supply current (total package)	No load	Output enabled		80	110	mA
		No load	Output disabled		50	80	mA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Refer to TIA-EIA-422-B for exact conditions.
(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Switching Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 100 Ω, C_L = 50 pF, See Figure 3		20	25	ns
$t_{t(OD)}$	Differential output transition time	R_L = 100 Ω, C_L = 50 pF, See Figure 3		27	35	ns
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 27 Ω, See Figure 4		20	25	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 27 Ω, See Figure 4		20	25	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 5		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 6		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 5		90	120	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 6		30	45	ns

RECEIVER SECTION

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input						0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input				–0.2(2)			V
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})					50		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	SN7534050	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –400 µA,	See Figure 2	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, See Figure 2	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	SN7534050	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current		Other input at 0 V	V_I = 10 V			1.5	mA
				V_I = –10 V			–2.5	
I_{IH}	High-level enable input current, $\overline{RE}$	SN7534050	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable input current, $\overline{RE}$	SN7534050	V_{IL} = 0.4 V				–100	µA
r_i	Input resistance				12			kΩ
I_{OS}	Short circuit output current				–15		–85	mA
I_{CC}	Supply current (total package)		No load, enabled			80	110	mA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels.

Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		V_{ID} = 1.5 V, C_L = 15 pF, See Figure 7		20	35	ns
t_{PHL}	Propagation delay time, high- to low-level output		V_{ID} = 1.5 V, C_L = 15 pF, See Figure 7		22	35	ns
t_{PZH}	Output enable time to high level	SN7534050	C_L = 15 pF, see Figure 8		17	25	ns
t_{PZL}	Output enable time to low level	SN7534050	C_L = 15 pF, See Figure 8		20	27	ns
t_{PHZ}	Output disable time from high level	SN7534050	C_L = 15 pF, See Figure 8		25	40	ns
t_{PLZ}	Output disable time from low level	SN7534050	C_L = 15 pF, See Figure 8		30	40	ns

PARAMETER MEASUREMENT INFORMATION

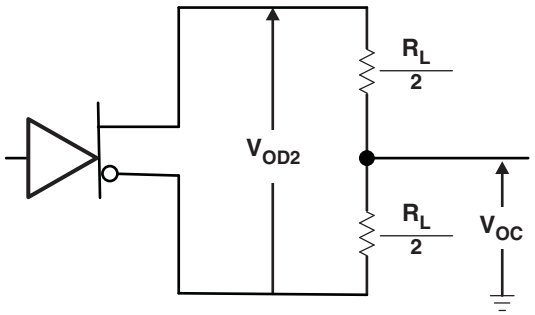


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

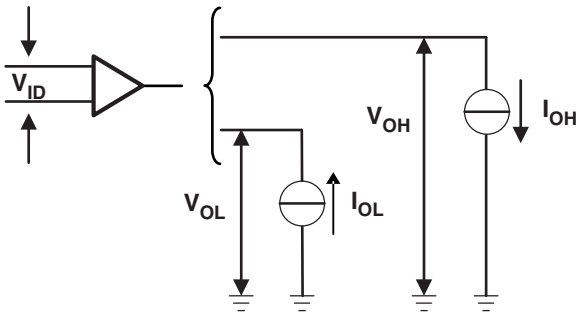


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

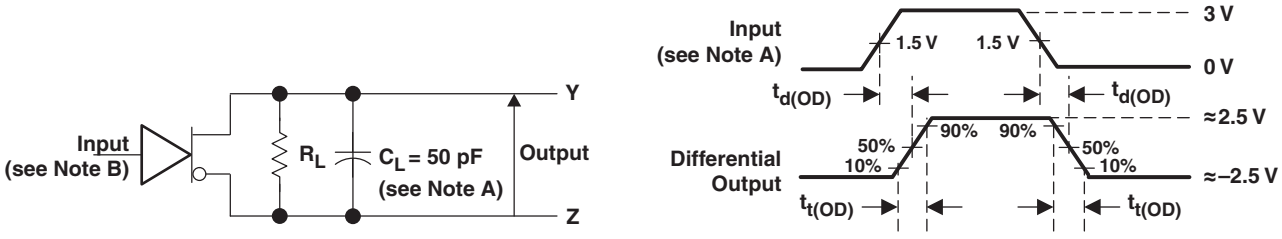


Figure 3. Driver Test Circuit and Voltage Waveforms, $t_{d(OD)}$ and $t_{t(OD)}$

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

PARAMETER MEASUREMENT INFORMATION (continued)

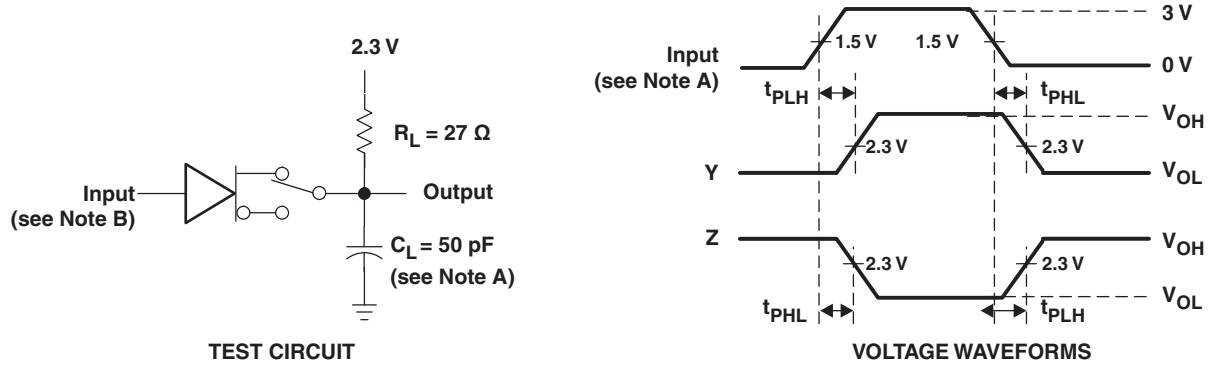


Figure 4. Driver Test Circuit and Voltage Waveforms, t_{PLH} and t_{PHL}

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

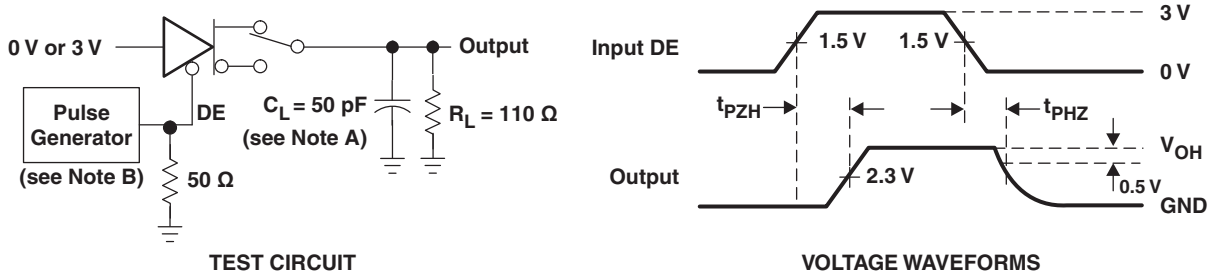


Figure 5. Driver Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

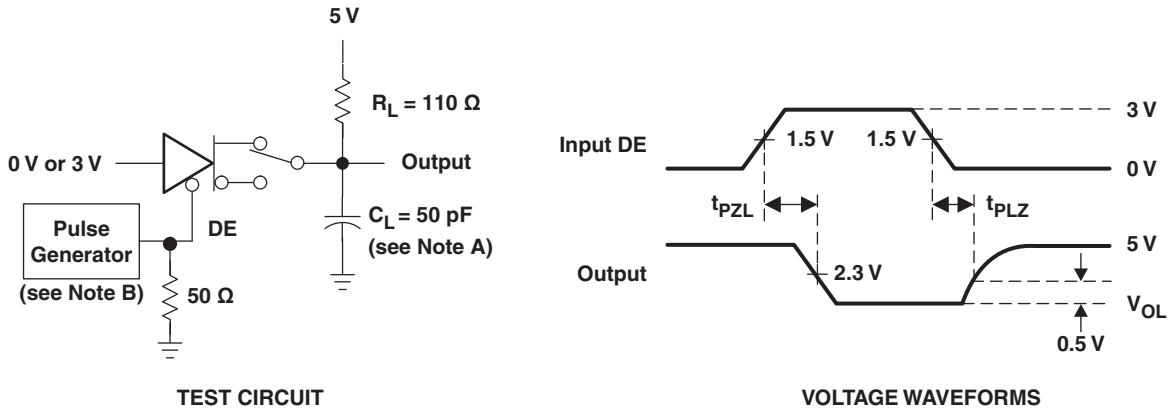


Figure 6. Driver Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

PARAMETER MEASUREMENT INFORMATION (continued)

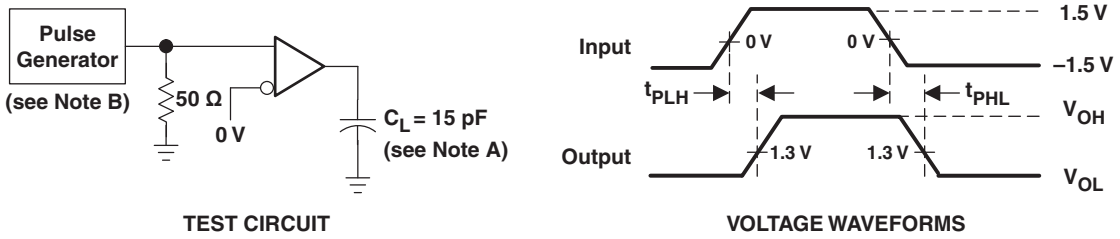


Figure 7. Receiver Test Circuit and Voltage Waveforms, t_{PLH} and t_{PHL}

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f$ ≤ 6 ns.

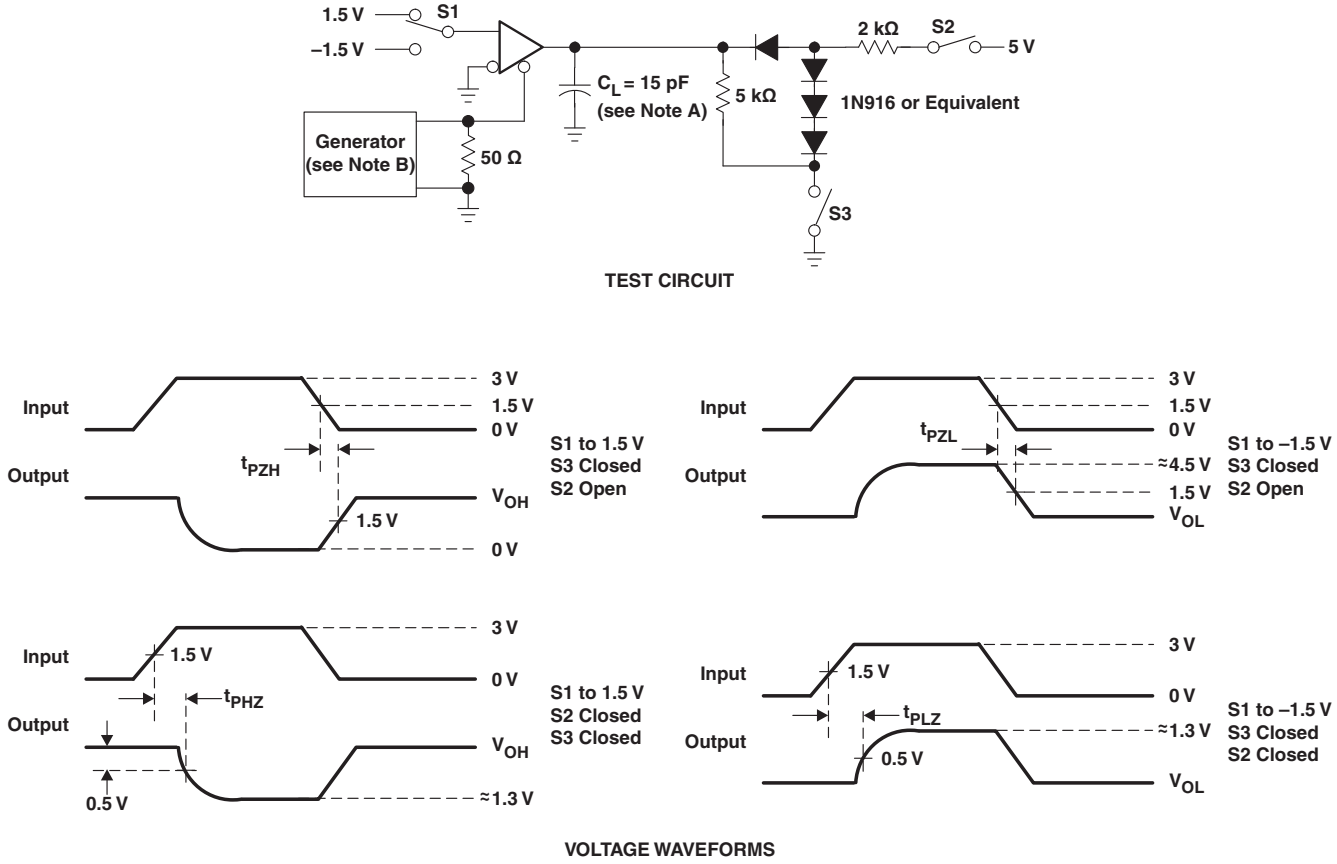


Figure 8. Receiver Test Circuit and Voltage Waveforms, t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ} (SN7534050)

REVISION HISTORY

Changes from Original (May 2007) to Revision A	Page
• Updated document format from QS to DocZone.	1
• Updated ORDERING INFORMATION table.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN7534050N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 85	SN7534050N	Samples
SN7534050NS	ACTIVE	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	SN7534050	Samples
SN7534050NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN7534050	Samples
SN7534051N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 85	SN7534051N	Samples
SN7534051NS	ACTIVE	SO	NS	16	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN7534051	Samples
SN7534051NSR	LIFEBUY	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN7534051	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

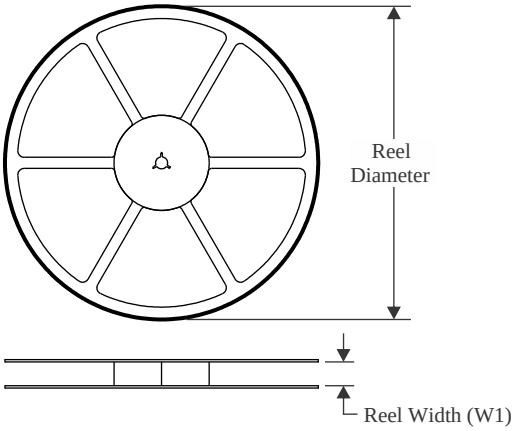
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

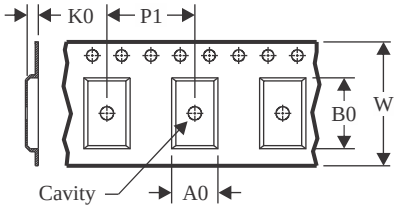
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

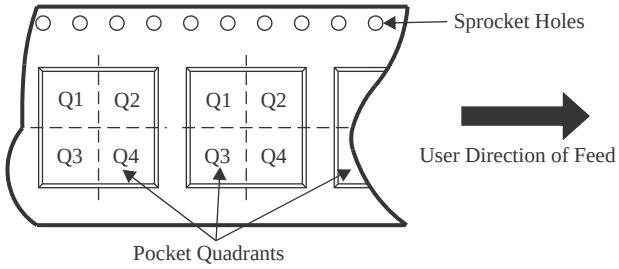


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

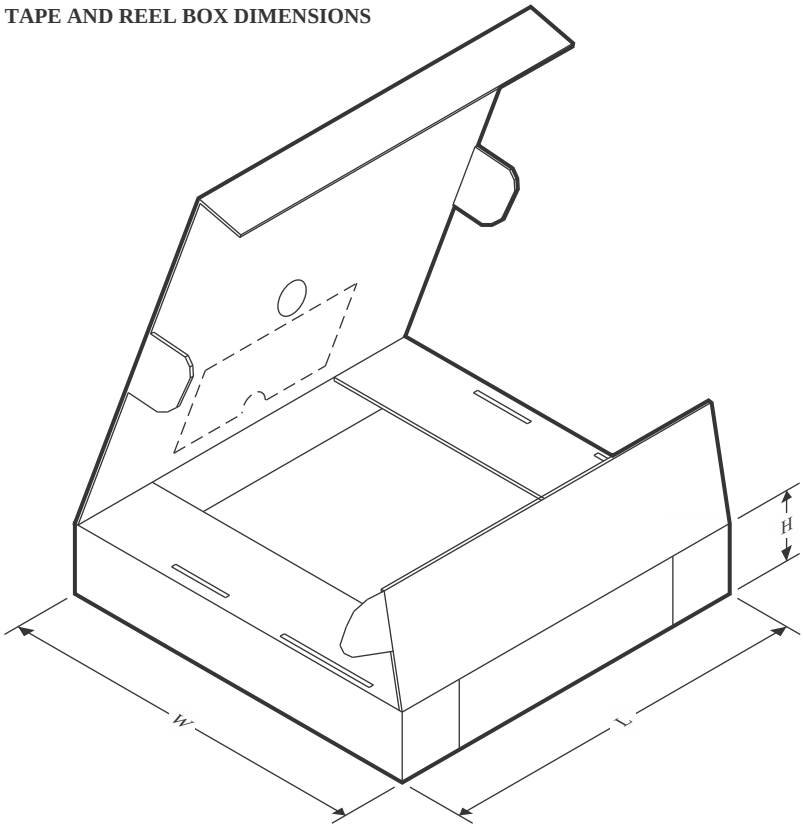
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN7534050NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN7534051NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

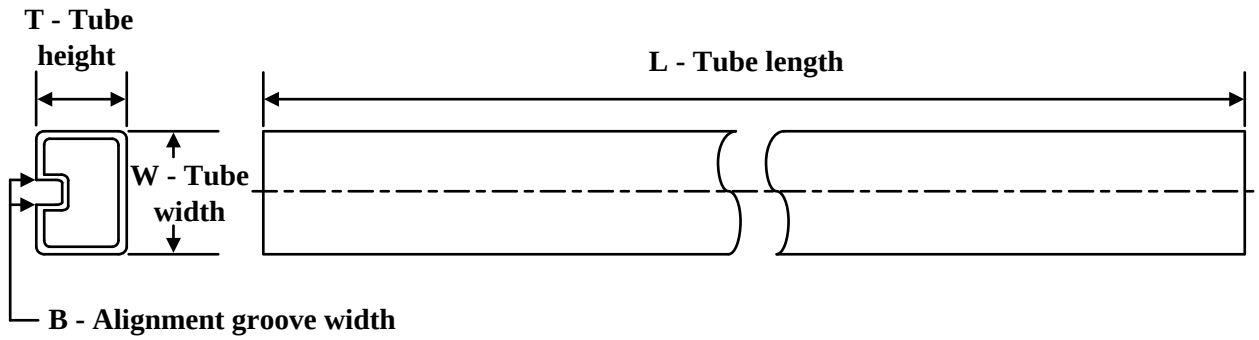
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

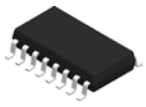
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN7534050NSR	SO	NS	16	2000	356.0	356.0	35.0
SN7534051NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN7534050N	N	PDIP	16	25	506	13.97	11230	4.32
SN7534050NS	NS	SOP	16	50	530	10.5	4000	4.1
SN7534051N	N	PDIP	16	25	506	13.97	11230	4.32
SN7534051NS	NS	SOP	16	50	530	10.5	4000	4.1

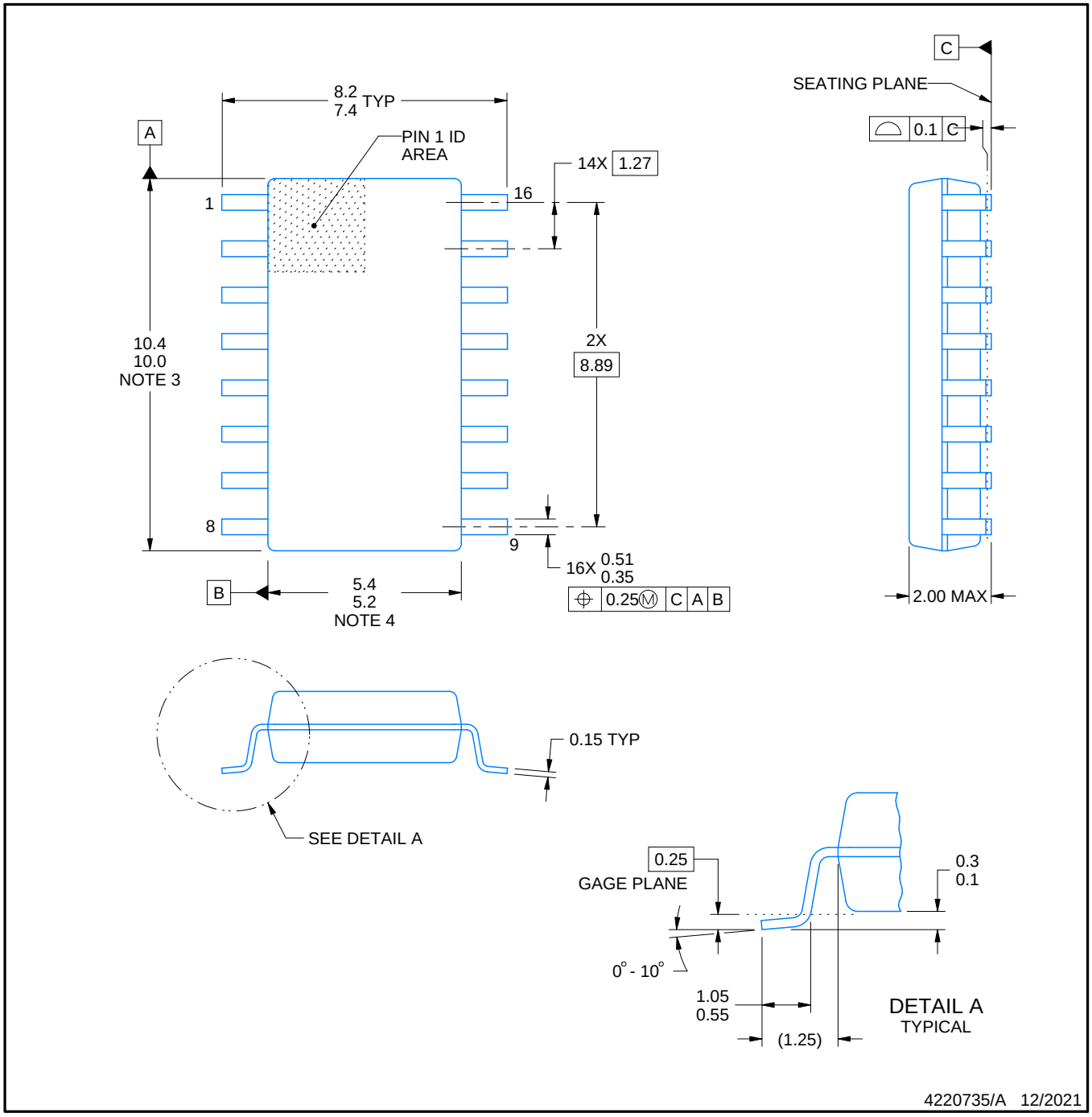


PACKAGE OUTLINE

NS0016A

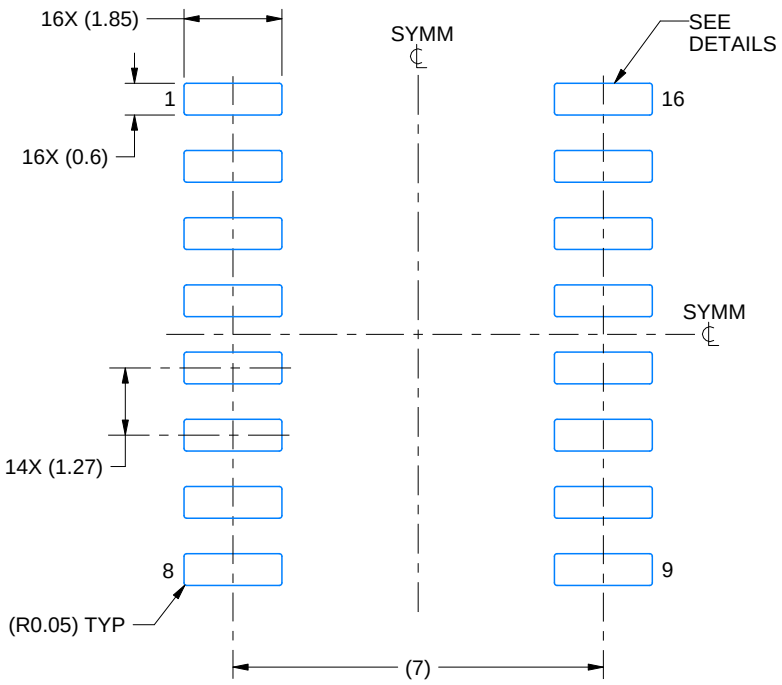
SOP - 2.00 mm max height

SOP

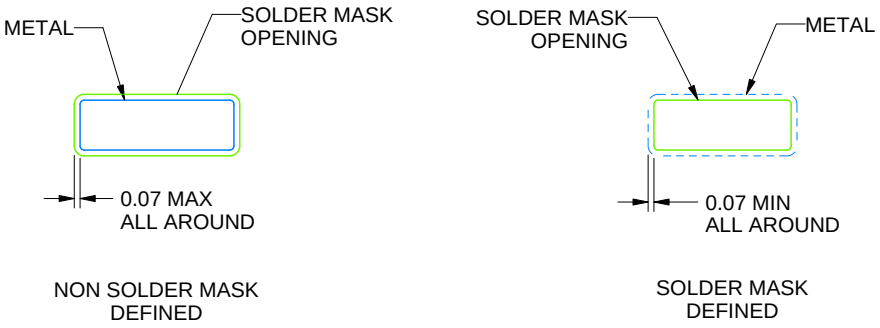


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

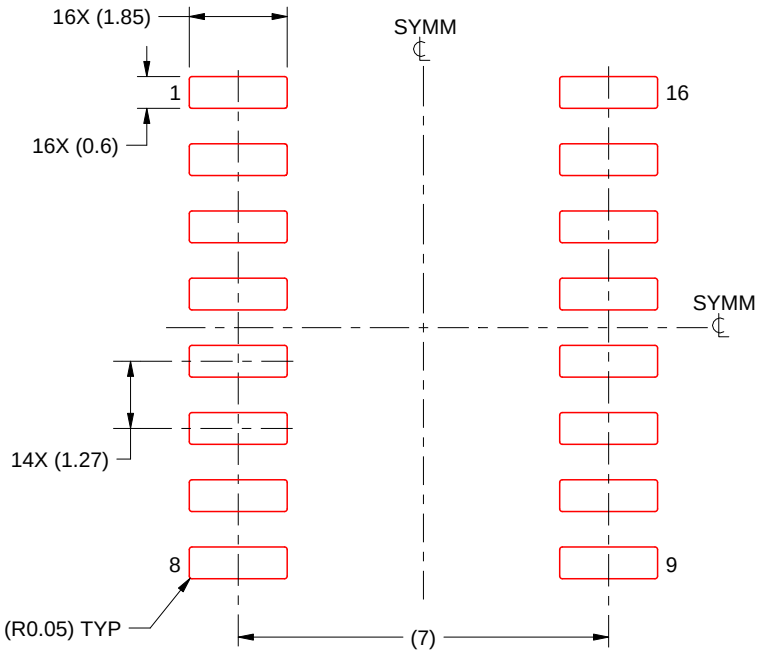
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

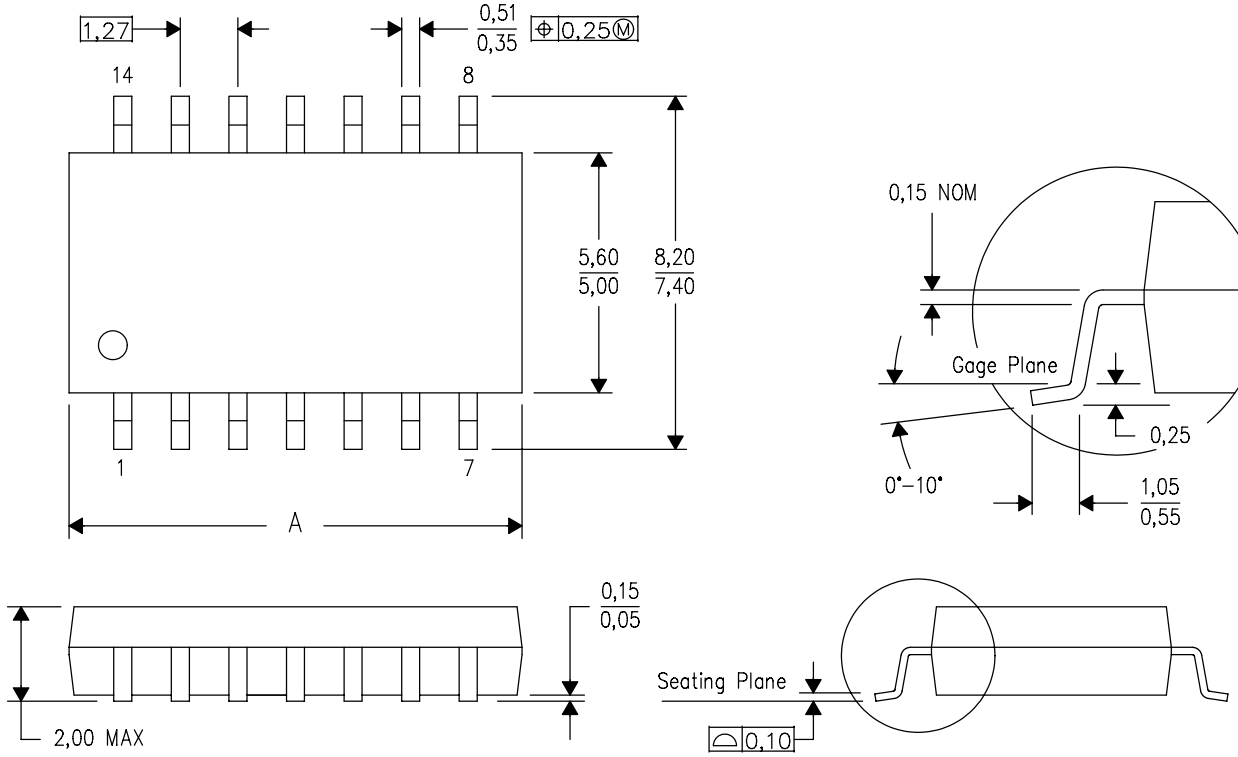
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

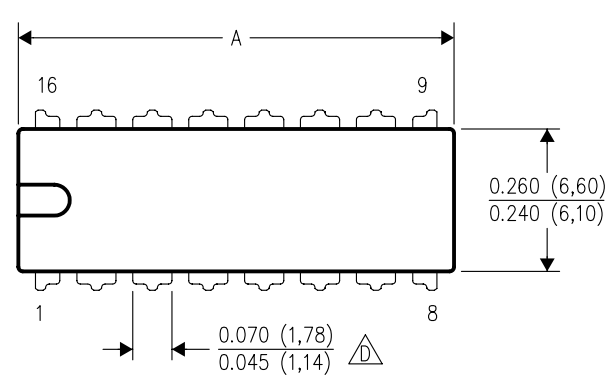
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

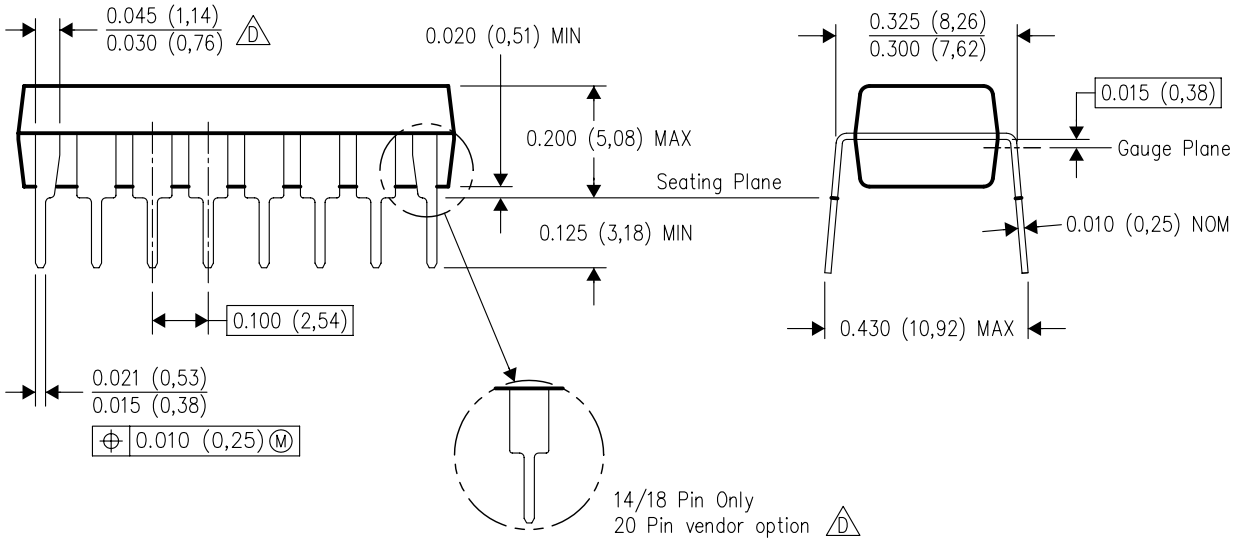
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265