

DisplayPort 1:2 Switch

FEATURES

- One Input Port to One of Two Output Ports
- Supports Data Rates up to 2.7Gbps
- Supports Dual-Mode DisplayPort
- Output Waveform Mimics Input Waveform Characteristics
- Enhanced ESD:
 - 12kV on all Main Link Pins
 - 10kV on all Auxiliary Pins
- Enhanced Commercial Temperature Range: 0°C to 85°C
- 56 Pin 8 × 8 QFN Package

APPLICATIONS

- Personal Computer Market
 - Desktop PC
 - Notebook PC
 - Docking Station
 - Standalone Video Card

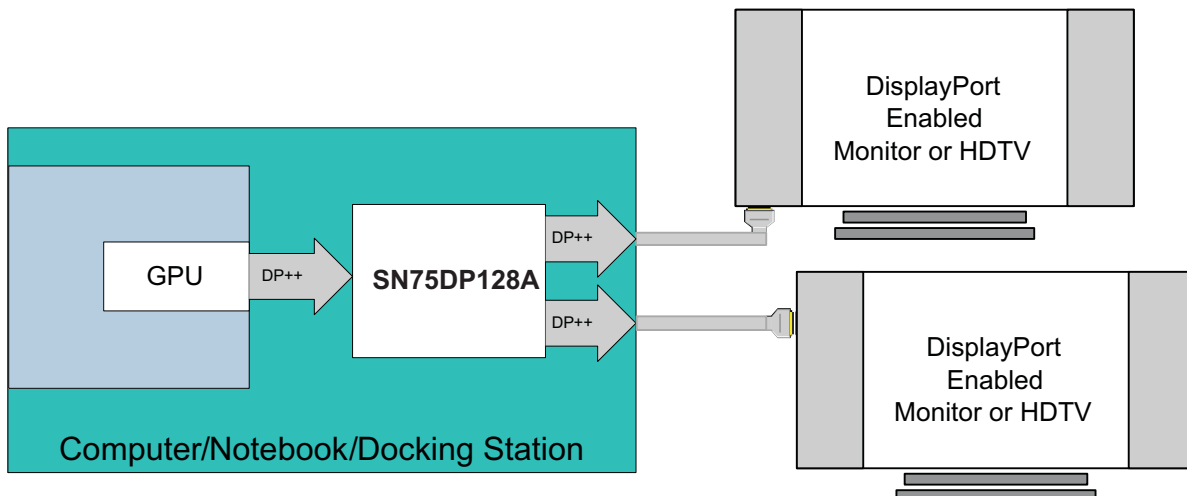
DESCRIPTION

The SN75DP128A is a one Dual-Mode DisplayPort input to one of two Dual-Mode DisplayPort outputs. The outputs will follow the input signal in a manner that provides the highest level of signal integrity while supporting the EMI benefits of spread spectrum clocking. Through the SN75DP128A data rates of up to 2.7Gbps through each link for a total throughput of up to 10.8Gbps can be realized. The SN75DP128A supports Display Port Spec 1.1a.

In addition to the switching of the DisplayPort high speed signal lines, the SN75DP128A also supports the switching of the bi-directional auxiliary (AUX), Hot Plug Detect (HPD), and Cable Adapter Detect (CAD) channels. The Auxiliary differential pair supports Dual-Mode DisplayPort operation with the ability to be configured as a bi-directional differential bus while in DisplayPort mode or an I2C™ bus while in TMDS mode.

The SN75DP128A is characterized for operation over ambient air temperature of 0°C to 85°C.

TYPICAL APPLICATION

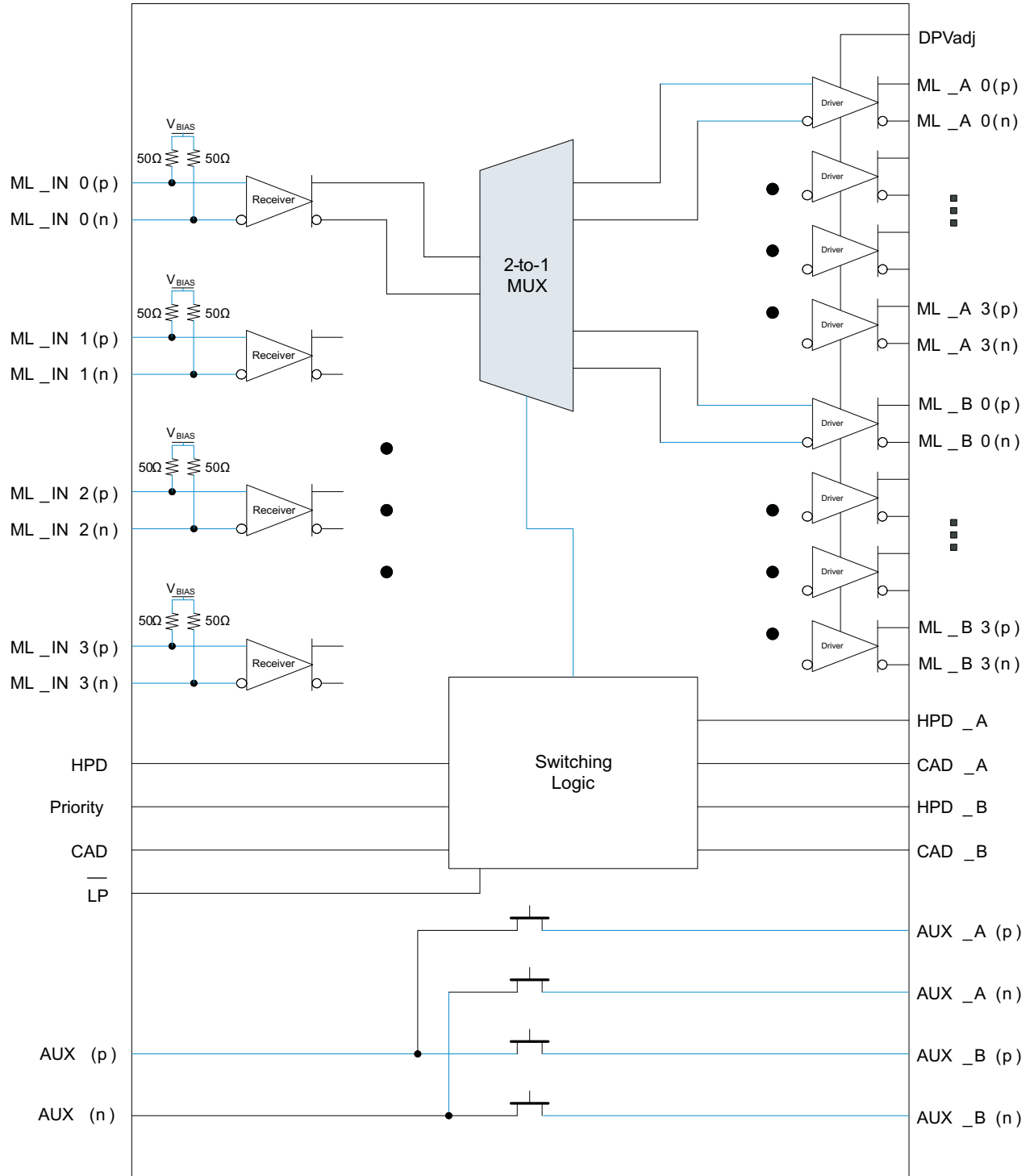


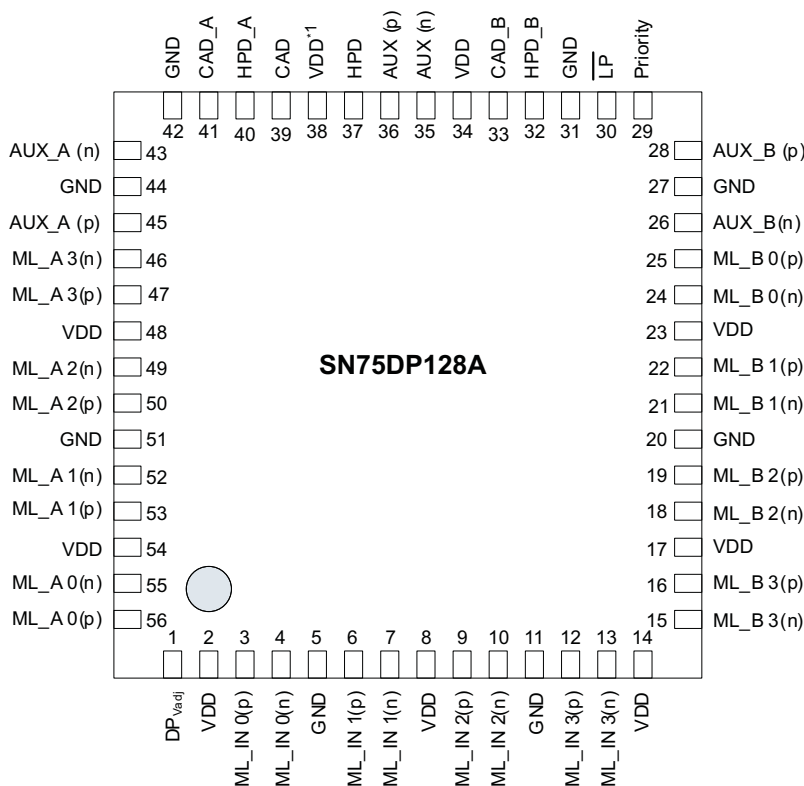
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DATA FLOW BLOCK DIAGRAM





TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
MAIN LINK INPUT PINS			
ML_IN 0	3, 4	I	DisplayPort Main Link Channel 0 Differential Input
ML_IN 1	6, 7	I	DisplayPort Main Link Channel 1 Differential Input
ML_IN 2	9, 10	I	DisplayPort Main Link Channel 2 Differential Input
ML_IN 3	12, 13	I	DisplayPort Main Link Channel 3 Differential Input
MAIN LINK PORT A OUTPUT PINS			
ML_A 0	56, 55	O	DisplayPort Main Link Port A Channel 0 Differential Output
ML_A 1	53, 52	O	DisplayPort Main Link Port A Channel 1 Differential Output
ML_A 2	50, 49	O	DisplayPort Main Link Port A Channel 2 Differential Output
ML_A 3	47, 46	O	DisplayPort Main Link Port A Channel 3 Differential Output
MAIN LINK PORT B OUTPUT PINS			
ML_B 0	25, 24	O	DisplayPort Main Link Port B Channel 0 Differential Output
ML_B 1	22, 21	O	DisplayPort Main Link Port B Channel 1 Differential Output
ML_B 2	19, 18	O	DisplayPort Main Link Port B Channel 2 Differential Output
ML_B 3	16, 15	O	DisplayPort Main Link Port B Channel 3 Differential Output
HOT PLUG DETECT PINS			
HPD	37	O	Hot Plug Detect Output to the DisplayPort Source
HDP_A	40	I	Port A Hot Plug Detect Input
HPD_B	32	I	Port B hot Plug Detect Input
AUXILIARY DATA PINS			
AUX	36, 35	I/O	Source Side Bidirectional DisplayPort Auxiliary Data Line
AUX_A	45, 43	I/O	Port A Bidirectional DisplayPort Auxiliary Data Line

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AUX_B	28, 26	I/O	Port B Bidirectional DisplayPort Auxiliary Data Line
CABLE ADAPTER DETECT PINS			
CAD	39	O	Cable Adapter Detect Output to the DisplayPort Source
CAD_A	41	I	Port A Cable Adapter Detect Input
CAD_B	33	I	Port B Cable Adapter Detect Input
CONTROL PINS			
$\overline{\text{LP}}$	30	I	Low Power Select Bar
Priority	29	I	Output Port Priority selection
DPVadj	1	I	DisplayPort Main Link Output Gain Adjustment
SUPPLY and GROUND PINS			
VDD	2, 8, 14, 17, 23, 34, 48, 54		Primary Supply Voltage
VDD ^{*1}	38		HPD and CAD Output Voltage
GND	5, 11, 20, 27, 42, 44, 51		Ground

Table 1. Control Pin Lookup Table

SIGNAL	LEVEL ⁽¹⁾	STATE	DESCRIPTION
$\overline{\text{LP}}$	H	Normal Mode	Normal operational mode for device
	L	Low Power Mode	Device is forced into a Low Power state causing the outputs to go to a high impedance state. All other inputs are ignored
Priority	H	Port B has Priority	If both HPD_A and HPD_B are high, Port B will be selected
	L	Port A has Priority	If both HPD_A and HPD_B are high, Port A will be selected
DP _{Vadj}	4.53 k Ω	Increased Gain	Main Link DisplayPort Output will have an increased voltage swing
	6.49 k Ω	Normal Gain	Main Link DisplayPort Output will have a nominal voltage swing
	10 k Ω	Decreased Gain	Main Link DisplayPort Output will have a decreased voltage swing

(1) (H) Logic High; (L) Logic Low

Explanation of the internal switching logic of the SN75DP128A is located in the Application Information section at the end of the data sheet.

ORDERING INFORMATION⁽¹⁾

PART NUMBER	PART MARKING	PACKAGE
SN75DP128ARTQR	DP128A	56-pin QFN Reel (large)
SN75DP128ARTQT	DP128A	56-pin QFN Reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE	UNIT	
Supply Voltage Range ⁽²⁾	V_{DD}, V_{DD}^{*1}	-0.3 to 5.25	V	
Voltage Range	Main Link I/O (ML_IN x, ML_A x, ML_B x) Differential Voltage	1.5	V	
	HPD and CAD I/O	-0.3 to $V_{DD} + 0.3$	V	
	Auxiliary I/O	-0.3 to $V_{DD} + 0.3$	V	
	Control I/O	-0.3 to $V_{DD} + 0.3$	V	
Electrostatic discharge	Human body model ⁽³⁾	Auxiliary I/O (AUX +/-, AUX_A +/-, & AUX_B +/-)	±10000	V
		All Other Pins	±12000	
	Charged-device model ⁽³⁾		±1000	V
	Machine model ⁽⁴⁾		±200	V
Continuous power dissipation		See Dissipation Rating Table		

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
- (4) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
56-pin QFN (RTQ)	Low-K	3623 mW	36.23 mW/°C	1449 mW
	High-K	1109 mW	11.03 mW/°C	443.9 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX ⁽¹⁾	UNIT
$R_{\theta JB}$ Junction-to-board thermal resistance	4x4 Thermal vias under powerpad		11.03		°C/W
$R_{\theta JC}$ Junction-to-case thermal resistance			20.4		= C/W
P_D Device power dissipation DisplayPort selected	$\overline{LP} = 5V$, ML: $V_{ID} = 600\text{ mV}$, 2.7 Gbps PRBS; AUX: $V_{ID} = 500\text{ mV}$, 1Mbps PRBS; HPD/CAD A and B = 5V; $V_{DD}^{*1} = V_{DD}$		300	340	mW
P_{SD} Device power dissipation under low power	$\overline{LP} = 0V$, HPD/CAD A and B = 5V; $V_{DD}^{*1} = V_{DD}$			85	μW

- (1) The maximum rating is simulated under 5.25 V VDD.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V_{DD} Supply Voltage	4.5	5	5.25	V
V_{DD}^{*1} HPD and CAD Output reference voltage	1.62		5.25	V
T_A Operating free-air temperature	0		85	°C
MAIN LINK DIFFERENTIAL PINS				
V_{ID} Peak-to-peak input differential voltage	0.15		1.4	V
d_R Data rate			2.7	Gbps
R_t Termination resistance	45	50	55	Ω
V_{Oterm} Output termination voltage	0		2	V
AUXILIARY PINS				

RECOMMENDED OPERATING CONDITIONS (continued)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	0		3.6	V
d_R	Data rate			1	MHz
HPD, CAD, AND CONTROL PINS					
V_{IH}	High-level input voltage	2		5.25	V
V_{IL}	Low-level input voltage	0		0.8	V

DEVICE POWER

The SN75DP128A is designed to operate off a single 5V supply.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current LP = 5V, $V_{DD}^{*1} = V_{DD}$ ML: $V_{ID} = 600$ mV, 2.7 Gbps PRBS AUX: $V_{ID} = 500$ mV, 1 Mbps PRBS HPD/CAD A and B = 5 V		60	65	mA
I_{DD}^{*1}	Supply current $V_{DD}^{*1} = 5.25$ V		0.1	4	mA
I_{SD}	Shutdown current $\overline{LP} = 0$ V		1	16	μ A

HOT PLUG AND CABLE ADAPTER DETECT

The SN75DP128A is designed to support the switching of the Hot Plug Detect and Cable adapter Detect signals. The SN75DP128A has a built in level shifter for the HPD and CAD outputs. The output voltage level of the HPD and CAD pins is defined by the voltage level of the V_{DD}^{*1} pin. Explanation of HPD and the internal logic of the SN75DP128A is located in the application section at the end of the data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH5}	High-level output voltage $I_{OH} = -100$ μ A, $V_{DD}^{*1} = 5$ V	4.5		5	V
$V_{OH3.3}$	High-level output voltage $I_{OH} = -100$ μ A, $V_{DD}^{*1} = 3.3$ V	3		3.3	V
$V_{OH2.5}$	High-level output voltage $I_{OH} = -100$ μ A, $V_{DD}^{*1} = 2.5$ V	2.25		2.5	V
$V_{OH1.8}$	High-level output voltage $I_{OH} = -100$ μ A, $V_{DD}^{*1} = 1.8$ V	1.62		1.8	V
V_{OL}	Low-level output voltage $I_{OH} = 100$ μ A	0		0.4	V
I_H	High-level input current $V_{IH} = 2.0$ V, $V_{DD} = 5.25$ V	-10		10	μ A
I_L	Low-level input current $V_{IL} = 0.8$ V, $V_{DD} = 5.25$ V	-10		10	μ A

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(CAD)}$	Propagation delay $V_{DD}^{*1} = 5$ V	5		30	ns
$t_{PD(HPD)}$	Propagation delay $V_{DD}^{*1} = 5$ V	30		110	ns
$t_{T1(HPD)}$	HPD logic switch pause time $V_{DD}^{*1} = 5$ V	2		4.7	ms
$t_{T2(HPD)}$	HPD logic switch time $V_{DD}^{*1} = 5$ V	170		400	ms
$t_{M(HPD)}$	Minimum output pulse duration $V_{DD}^{*1} = 5$ V	100			ns
$t_{Z(HPD)}$	Low Power to High-level propagation delay $V_{DD}^{*1} = 5$ V	30	50	110	ns

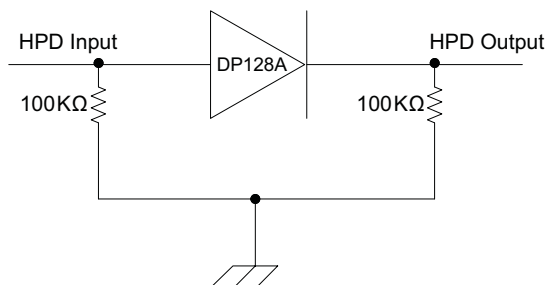


Figure 1. HPD Test Circuit

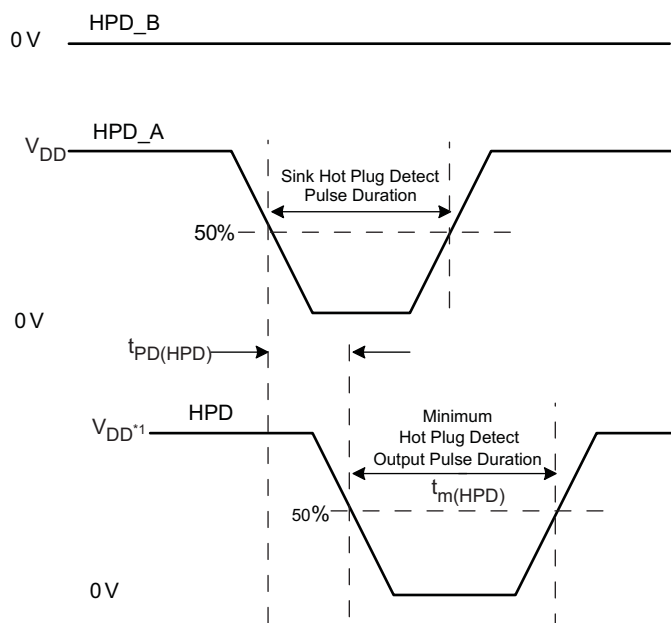


Figure 2. HPD Timing Diagram #1

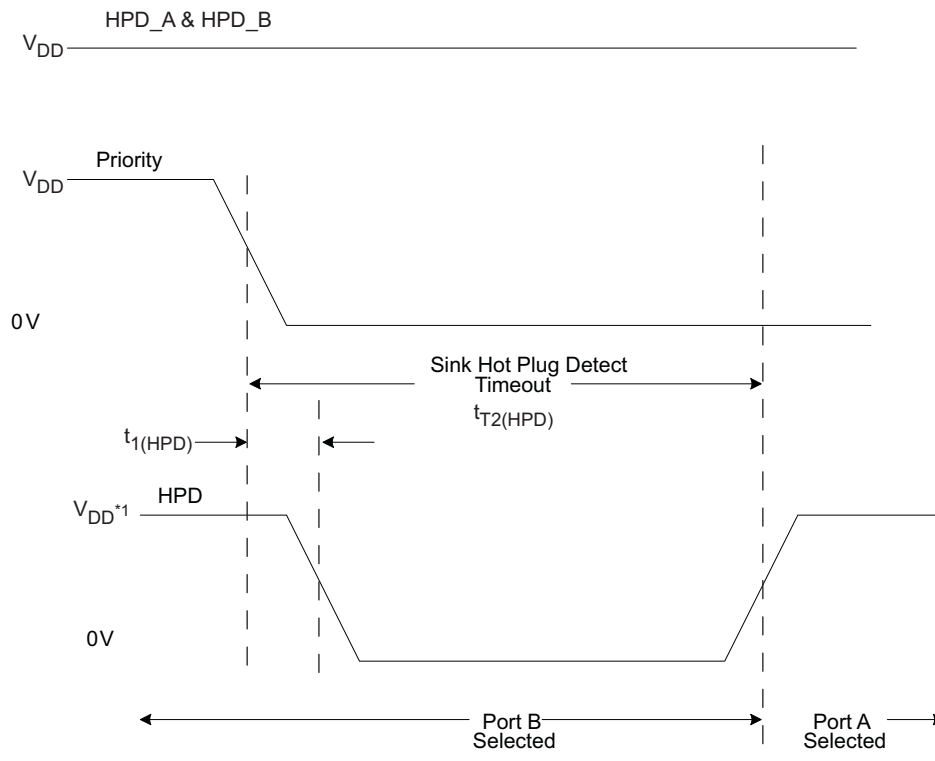


Figure 3. HPD Timing Diagram #2

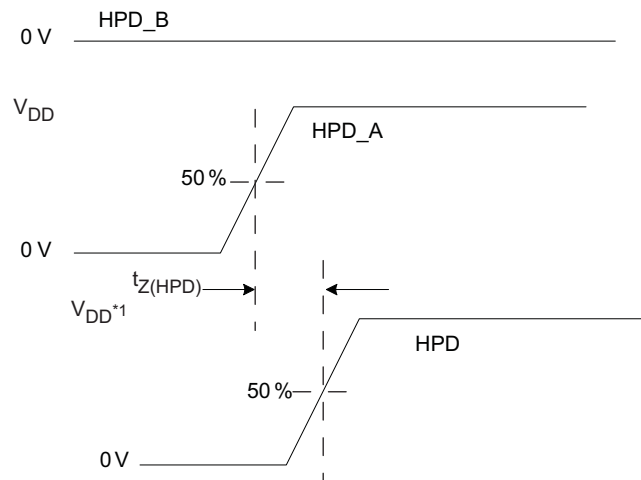


Figure 4. HPD Timing Diagram #3

Auxiliary Pins

The SN75DP128A is designed to support the 1:2 switching of the bidirectional auxiliary signals in both a differential (DisplayPort) mode and an I²C (DVI, HDMI) mode. The performance of the Auxiliary bus is optimized based on the status of the selected output port's CAD pin.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{Pass1}	Maximum passthrough voltage (CAD=1)	$V_{DD} = 4.5\text{ V}$, $V_I = 5\text{ V}$, $I_O = 100\ \mu\text{A}$	2.4		4.2	V
I_{OZ}	Output current from unselected output	$V_{DD} = 5.25\text{ V}$, $V_O = 0\text{--}3.6\text{ V}$, $V_I = 0\text{ V}$	–5		5	μA
$C_{IO(off)}$	I/O capacitance when in low power	DC bias = 1 V, AC = 1.4 Vp-p, F = 100 kHz,		9	12	pF
$C_{IO(on)}$	I/O capacitance when in normal operation	DC bias = 1 V, AC = 1.4 Vp-p, F = 100 kHz, CAD = High		18	25	pF
$r_{ON(C0-AUX+)}$	On resistance AUX+	$V_{DD} = 4.5\text{ V}$, $V_I = 0\text{ V}$, $I_O = 5\text{ mA}$, CAD = Low		3.5	10	Ω
$r_{ON(C0-AUX-)}$	On resistance AUX-	$V_{DD} = 4.5\text{ V}$, $V_I = 3.6\text{ V}$, $I_O = 5\text{ mA}$, CAD = Low		3.5	10	Ω
$r_{ON(C1)}$	On resistance	$V_{DD} = 4.5\text{ V}$, $V_I = 0.4\text{ V}$, $I_O = 3\text{ mA}$, CAD = High		10	18	Ω
V_{AUX+}	Voltage on the AUX+	$V_{DD} = 4.5\text{ V}$, 100k pullup on AUX+ to 3.3V $\pm 10\%$, HPD_SINK = Low	1.48		1.81	V
V_{AUX-}	Voltage on the AUX-	$V_{DD} = 4.5\text{ V}$, 100k pulldown on AUX- to GND, HPD_SINK = Low	1.48		1.81	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(AUX)}$	Intra-pair skew	$V_{ID} = 400\text{ mV}$, $V_{IC} = 2\text{ V}$		350	400	ps
$I_L(AUX)$	Single Line Insertion Loss	$V_{ID} = 500\text{ mV}$, $V_{IC} = 2\text{ V}$, F = 1 MHz, CAD = Low			0.4	dB
$t_{PLH(AUXC0)}$	Propagation delay time, low to high	CAD = Low, F = 1 MHz			3	ns
$t_{PHL(AUXC0)}$	Propagation delay time, high to low	CAD = Low, F = 1 MHz			3	ns
$t_{PLH(AUXC1)}$	Propagation delay time, low to high	CAD = High, F = 100 kHz			5	ns
$t_{PHL(AUXC1)}$	Propagation delay time, high to low	CAD = High, F = 100 kHz			5	ns

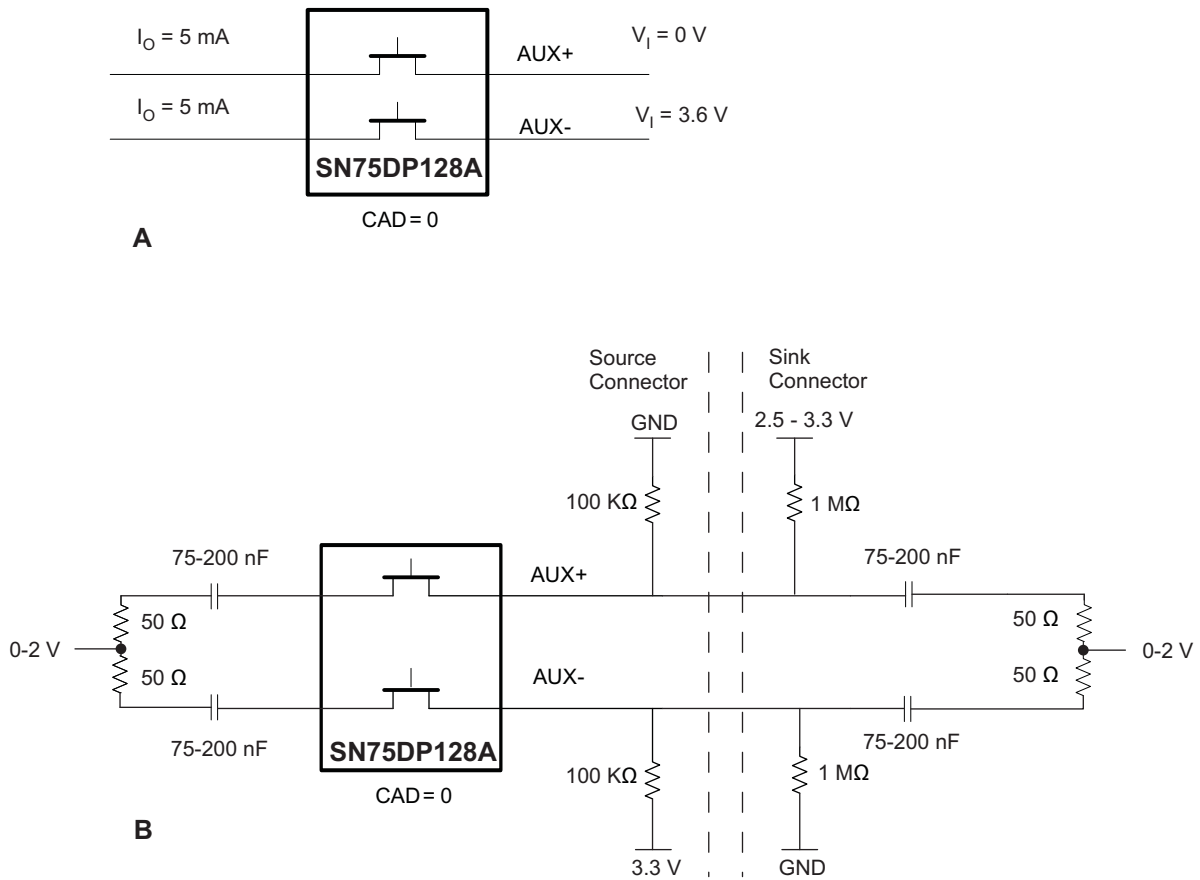


Figure 5. Auxiliary Channel Test Circuit (CAD = LOW)

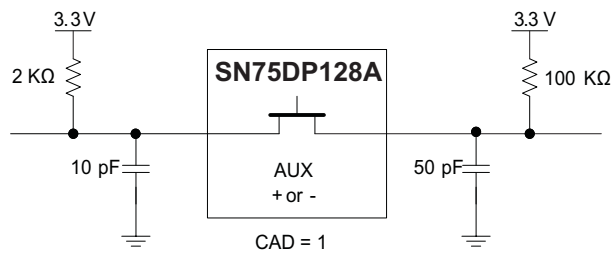


Figure 6. Auxiliary Channel Test Circuit (CAD = HIGH)

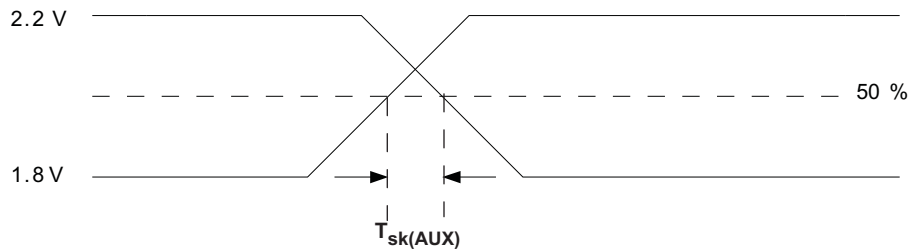


Figure 7. Auxiliary Channel Skew Measurement

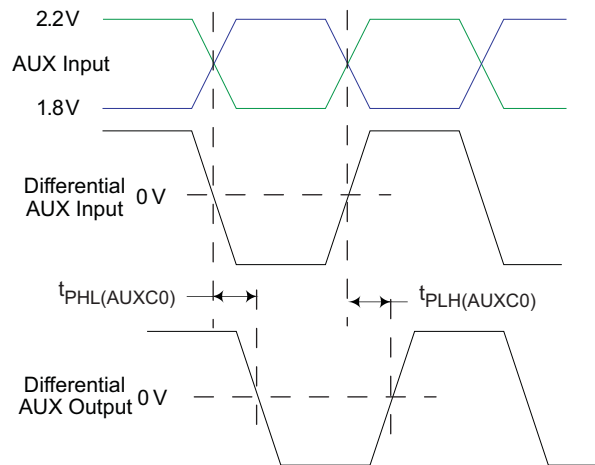


Figure 8. Auxiliary Channel Delay Measurement (CAD = LOW)

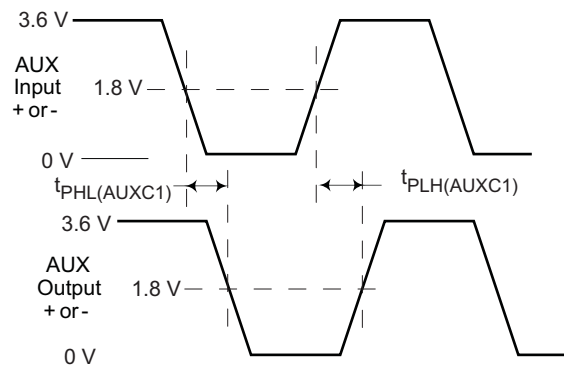


Figure 9. Auxiliary Channel Delay Measurement (CAD = HIGH)

Main Link Pins

The SN75DP128A is designed to support the 1:2 switching of DisplayPort's high speed differential main link. The main link I/O of the SN75DP128A are designed to track the magnitude and frequency characteristics of the input waveform and replicate them on the output. A feature has also been incorporated in the SN75DP128A to either increase or decrease the output amplitude via the resistor connected between the DPVADJ pin and ground.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{I/O(2)}$	Difference between input and output voltages ($V_{OD} - V_{ID}$)	$V_{ID} = 200 \text{ mV}$, $DPV_{adj} = 6.5 \text{ k}\Omega$	0	30	60	mV
$\Delta V_{I/O(3)}$		$V_{ID} = 300 \text{ mV}$, $DPV_{adj} = 6.5 \text{ k}\Omega$	-24	11	36	mV
$\Delta V_{I/O(4)}$		$V_{ID} = 400 \text{ mV}$, $DPV_{adj} = 6.5 \text{ k}\Omega$	-45	-15	15	mV
$\Delta V_{I/O(6)}$		$V_{ID} = 600 \text{ mV}$, $DPV_{adj} = 6.5 \text{ k}\Omega$	-87	-47	-22	mV
R_{INT}	Input termination impedance		45	50	55	Ω
V_{Iterm}	Input termination voltage		0		2	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R/F(DP)}$	Output edge rate (20%–80%)	Input edge rate = 80 ps (20%–80%)		115	160	ps
t_{PD}	Propagation delay time	F = 1 MHz, $V_{ID} = 400$ mV	200	240	280	ps
$t_{SK(1)}$	Intra-pair skew	F = 1 MHz, $V_{ID} = 400$ mV			20	ps
$t_{SK(2)}$	Inter-pair skew	F = 1 MHz, $V_{ID} = 400$ mV			40	ps
$t_{DPJIT(PP)}$	Peak-to-peak output residual jitter	$d_R = 2.7$ Gbps, $V_{ID} = 400$ mV, PRBS 27-1		25	35	ps

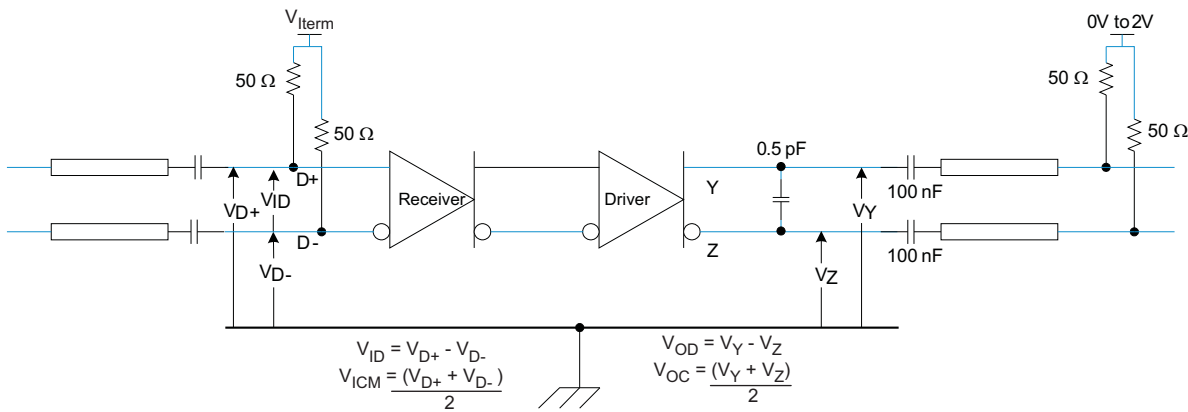


Figure 10. Main Link Test Circuit

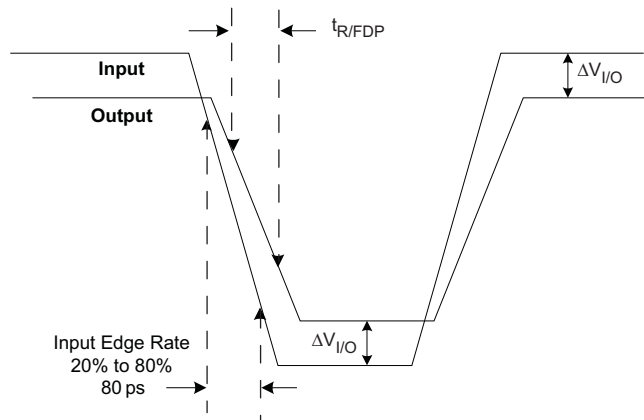


Figure 11. Main Link $\Delta V_{I/O}$ and Edge Rate Measurements

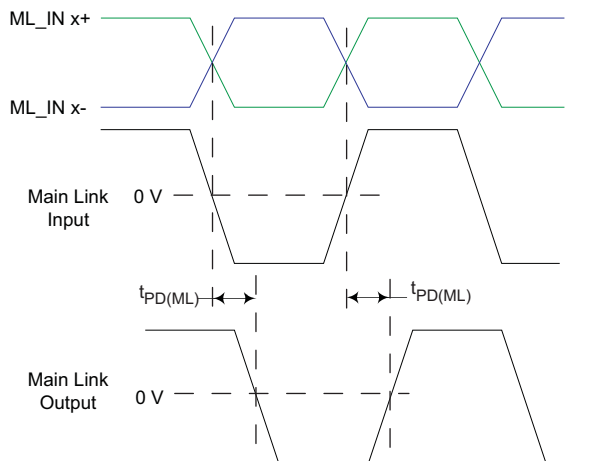


Figure 12. Main Link Delay Measurements

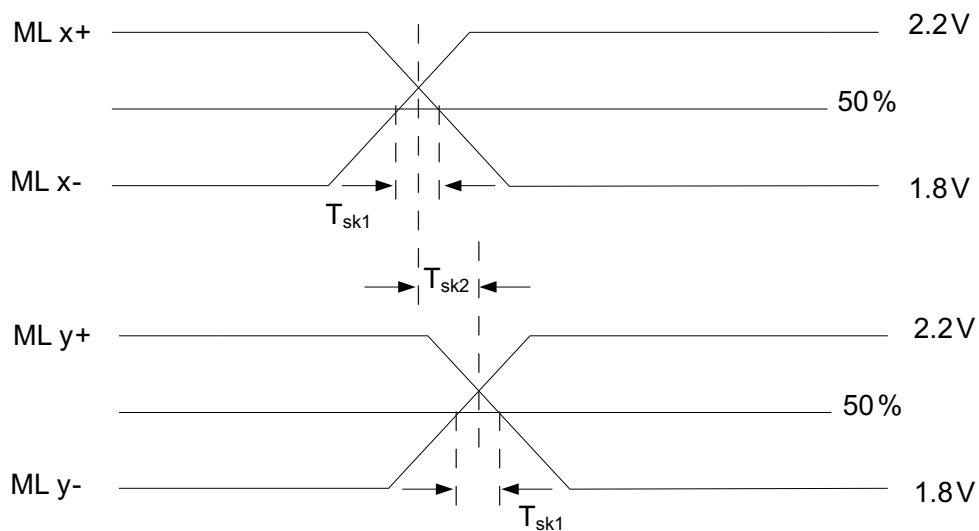


Figure 13. Main Link Skew Measurements

TYPICAL CHARACTERISTICS

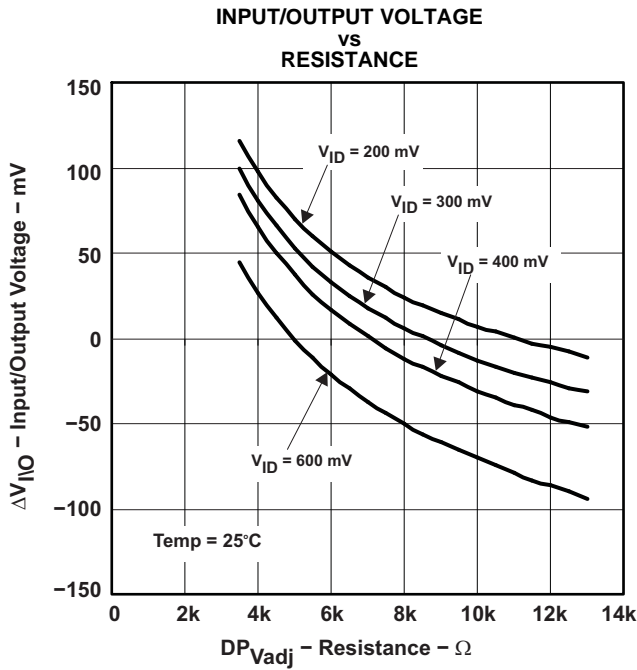


Figure 14.

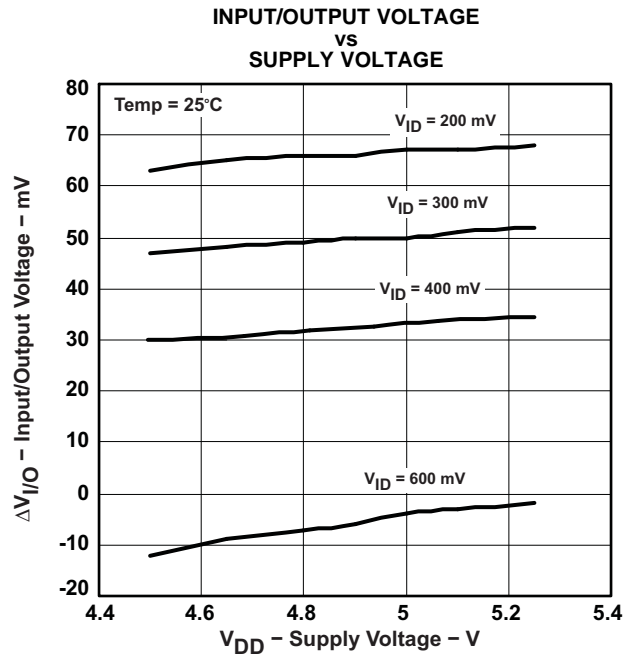


Figure 15.

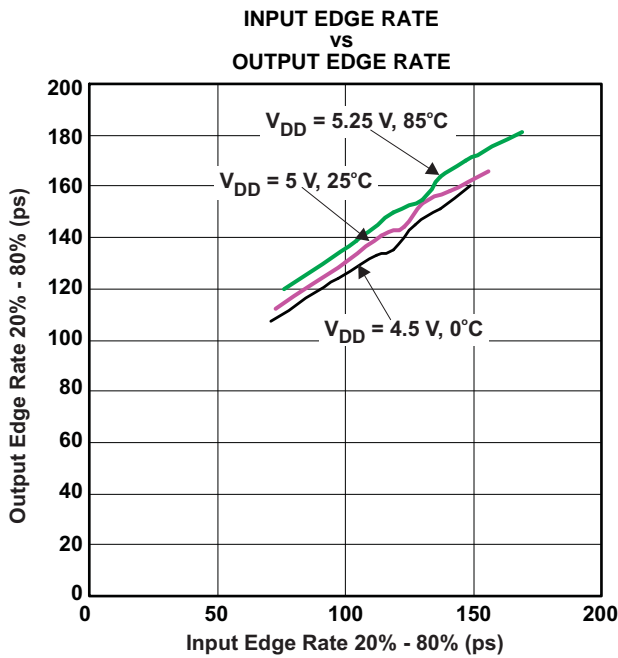


Figure 16.

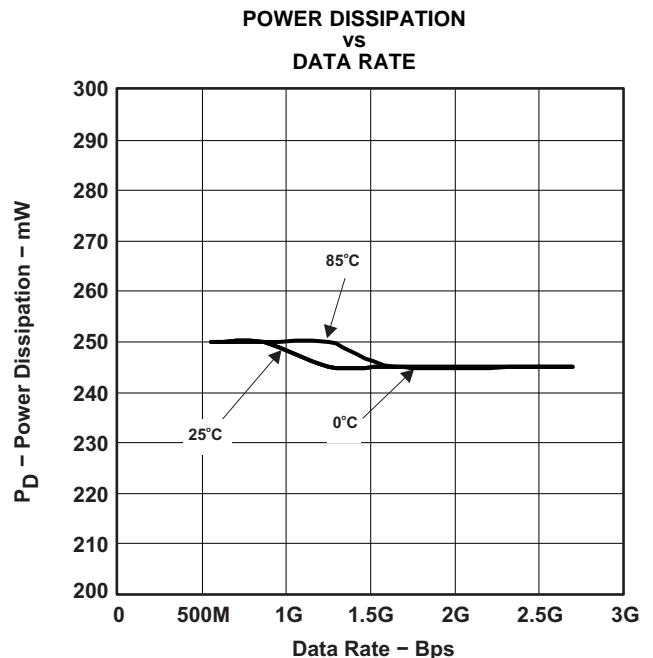


Figure 17.

APPLICATION INFORMATION

SWITCHING LOGIC

The switching logic of the SN75DP128A is tied to the state of the HPD input pins as well as the priority pin and low power pin. When both HPD_A and HPD_B input pins are LOW, the SN75DP128A enters the low power state. In this state the outputs are high impedance, and the device is shutdown to optimize power conservation. When either HPD_A or HPD_B goes high, the device enters the normal operational state, and the port associated with the HPD pin that went high is selected. If both HPD_A and HPD_B are HIGH, the port selection is determined by the state of the priority pin.

Several key factors were taken into consideration with this digital logic implementation of channel selection as well as HPD repeating. This logic has been divided into the following four scenarios.

1. Low power state to active state. There are two possible cases for this scenario depending on the state of the low power pin:
 - Case one: In this case both HPD inputs are initially LOW and the low power pin is also LOW. In this initial state the device is in a low power mode. Once one of the HPD inputs goes to a HIGH state, the device remains in the low power mode with both the main link and auxiliary I/O in a high impedance state. However, the port associated with the HPD input that went HIGH is still selected and the HPD output to the source is enabled and follows the logic state of the input HPD (see [Figure 18](#)). The state of the Priority pin has no effect in this scenario as only one HPD input port is active.

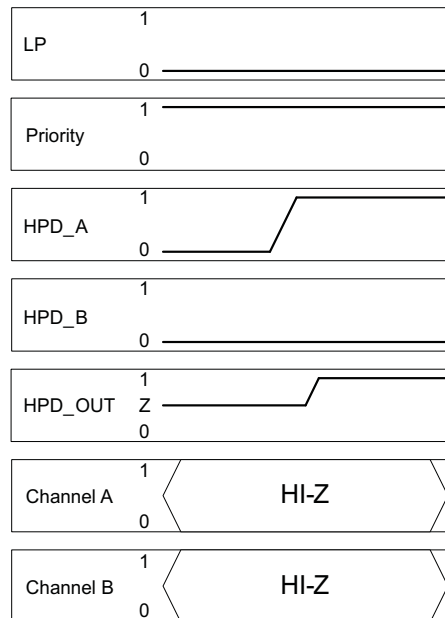


Figure 18.

- Case two: In this case both HPD inputs are initially LOW and the low power pin is HIGH. In this initial state the device is in a low power mode. Once one of the HPD inputs goes to a HIGH state, the device comes out of the low power mode and enters active mode enabling the main link and auxiliary I/O. The port associated with the HPD input that went HIGH is selected and the HPD output to the source is enabled and follows the logic state of the input HPD (see [Figure 19](#)). This is specified as $t_{Z(HPD)}$. Again, the state of the Priority pin has no effect in this scenario as only one HPD input port is active.

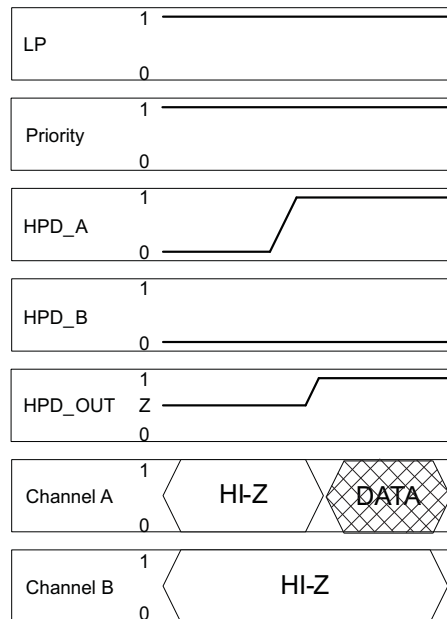


Figure 19.

2. HPD Changes on the selected port. There are also two possible starting cases for this scenario:
 - Case one: In this case only one HPD input is initially HIGH. The HPD output logic state follows the state of the HPD input. If the HPD input pulses LOW, as may be the case if the Sink device is requesting an interrupt, the HPD output to the source also pulses LOW for the same duration of time with a slight delay (see Figure 20). The delay of this signal through the SN75DP128A is specified as $t_{PD(HPD)}$. If the duration of the LOW pulse is less than $t_{M(HPD)}$, it may not be accurately repeated to the source. If the duration of the LOW pulse exceeds $t_{T2(HPD)}$, the device assumes that an unplug event has occurred and enters the low power state (see Figure 21). Once the HPD input goes high again, the device returns to the active state as indicated in scenario 1. The state of the Priority pin has no effect in this scenario as only one HPD input port is active.

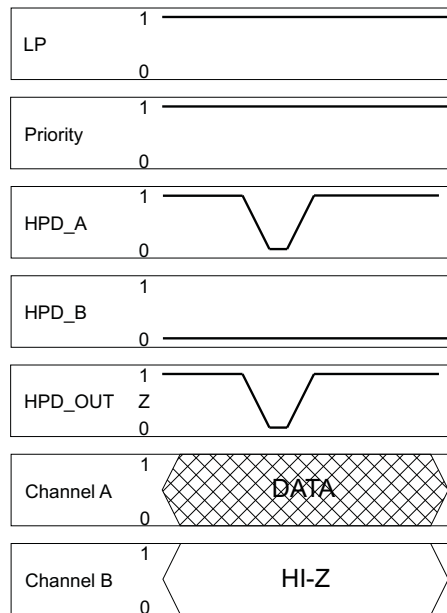


Figure 20.

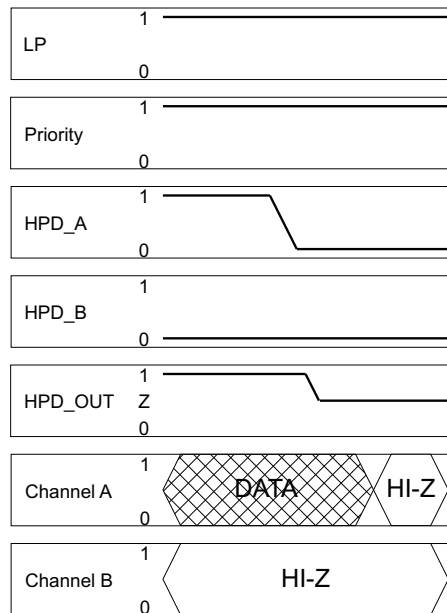


Figure 21.

- Case two: In this case both HPD inputs are initially HIGH and the selected port has been determined by the state of the priority pin. The HPD output logic state follows the state of the selected HPD input. If the HPD input pulses LOW, the HPD output to the source also pulses LOW for the same duration of time, again with a slight delay (see Figure 22). If the duration of the LOW pulse exceeds $t_{T2(HPD)}$, the device assumes that an unplug event has occurred and the other port is selected (see Figure 23). The case in which the previously selected port with priority goes high again is covered in scenario 3.

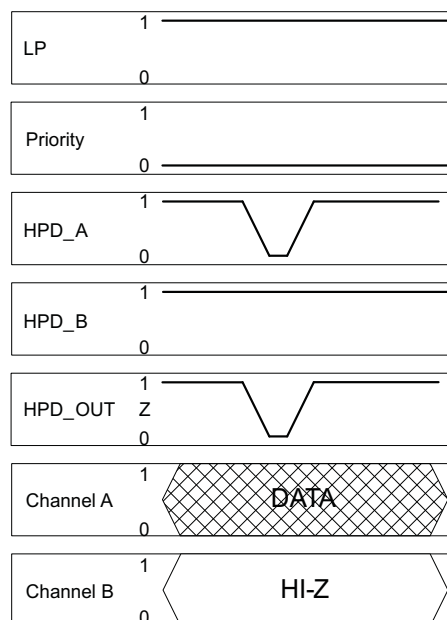


Figure 22.

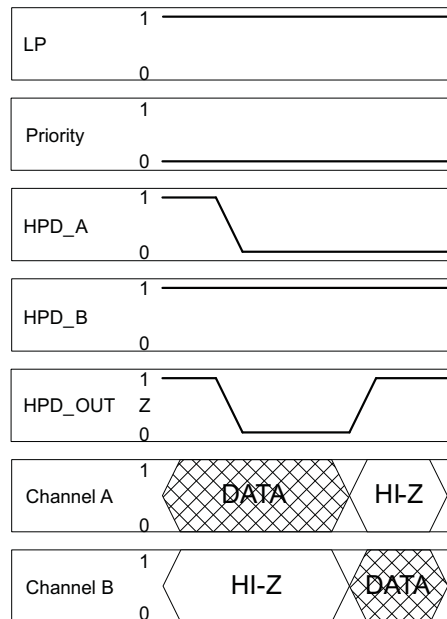


Figure 23.

3. One channel becomes active while other channel is already selected. There are also two possible starting cases for this scenario:
 - Case one: In this case the HPD input that is initially HIGH is from the port that has priority. Since the port with priority is already selected, any activity on the HPD input from the other port doesnot have any effect on the switch whatsoever (see [Figure 24](#)).

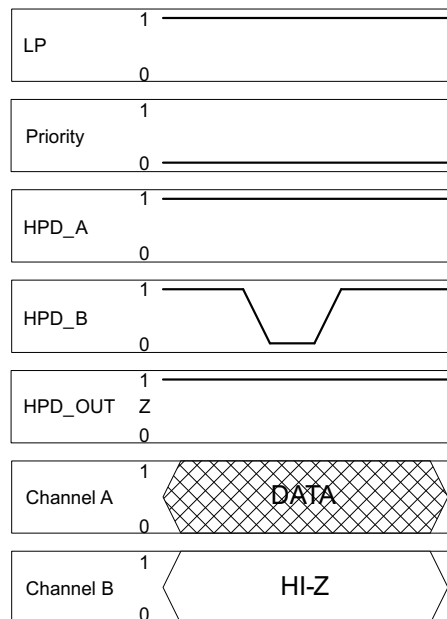


Figure 24.

- Case two: In this case the HPD input that is initially HIGH is not the port with priority. When the HPD input of the port that has priority goes high, the HPD output is forced LOW for some time in order to simulate an unplug event to the source device. The duration of this LOW output is defined as $t_{T2(HPD)}$. If the HPD input of the port with priority pulses LOW for a short duration while the $t_{T2(HPD)}$ timer is counting down, the timer is reset. Once this time has passed the switch switches to the port with priority and the output HPD

once again follows the state of the newly selected channel's HPD input (see Figure 25).

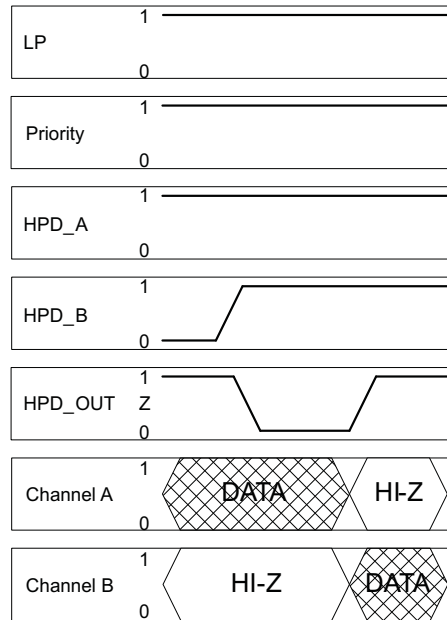


Figure 25.

4. 4. Priority pin is toggled. There are also two possible starting cases for this scenario:
 - Case one: In this case only one HPD input is HIGH. A port whose HPD input is LOW cannot be selected. In this case, the state of the priority pin has no effect on the switch (see Figure 26).

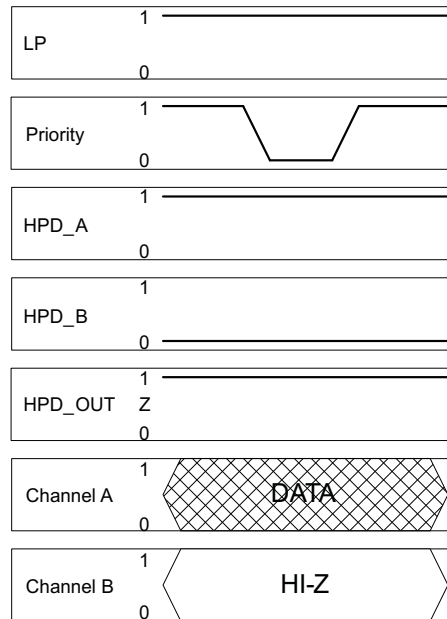


Figure 26.

- Case two: In this case both HPD inputs are HIGH. Changing the state of the priority pin when both HPD inputs are high forces the device to switch which channel is selected. When a state change is detected on the priority pin, the device waits for a short period of time $t_{T1(HPD)}$ before responding (see Figure 27). The purpose for this pause is to allow for the priority signal to settle and also to allow the device to ignore potential glitches on the priority pin. Once $t_{T1(HPD)}$ has expired, the HPD output is forced LOW for $t_{T2(HPD)}$ and the device follows the chain of events outlined in scenario 3 case 2.

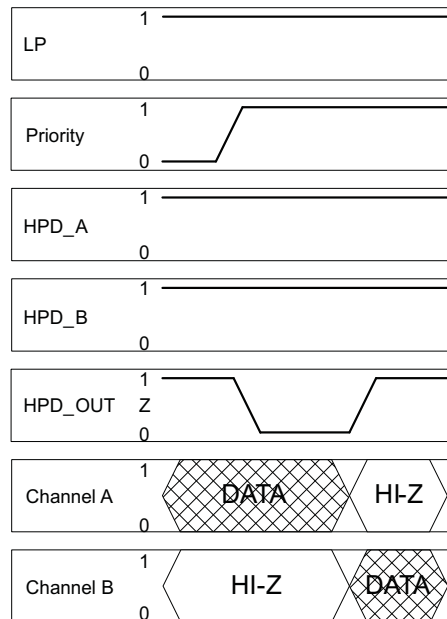


Figure 27.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75DP128ARTQR	Active	Production	QFN (RTQ) 56	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 85	DP128A
SN75DP128ARTQT	Active	Production	QFN (RTQ) 56	250 SMALL T&R	Yes	NIPDAU NIPDAU	Level-3-260C-168 HR	0 to 85	DP128A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP128ARTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
SN75DP128ARTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP128ARTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
SN75DP128ARTQT	QFN	RTQ	56	250	210.0	185.0	35.0

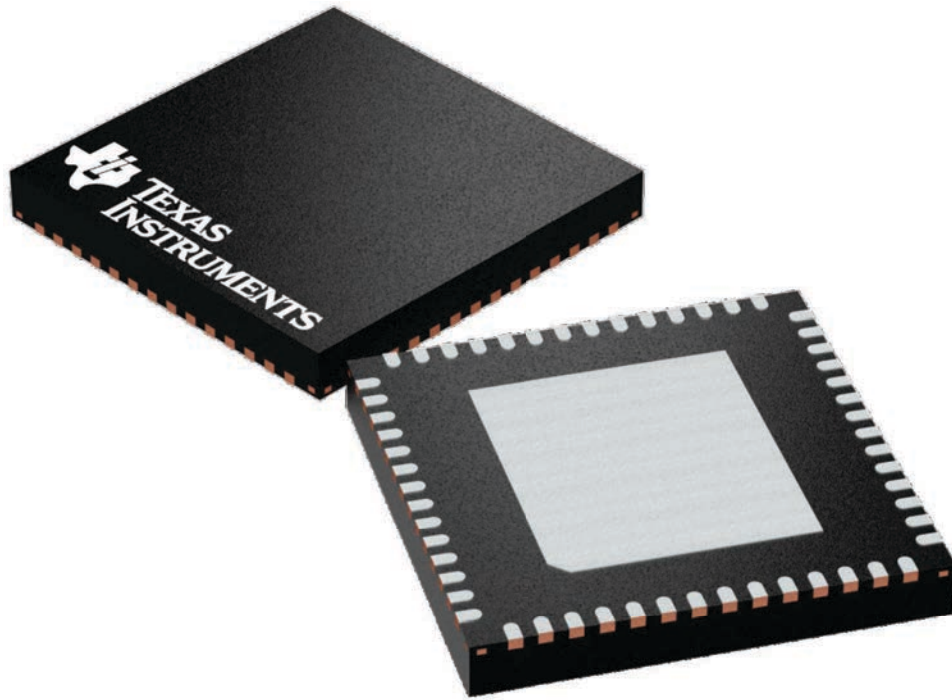
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

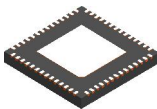
8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

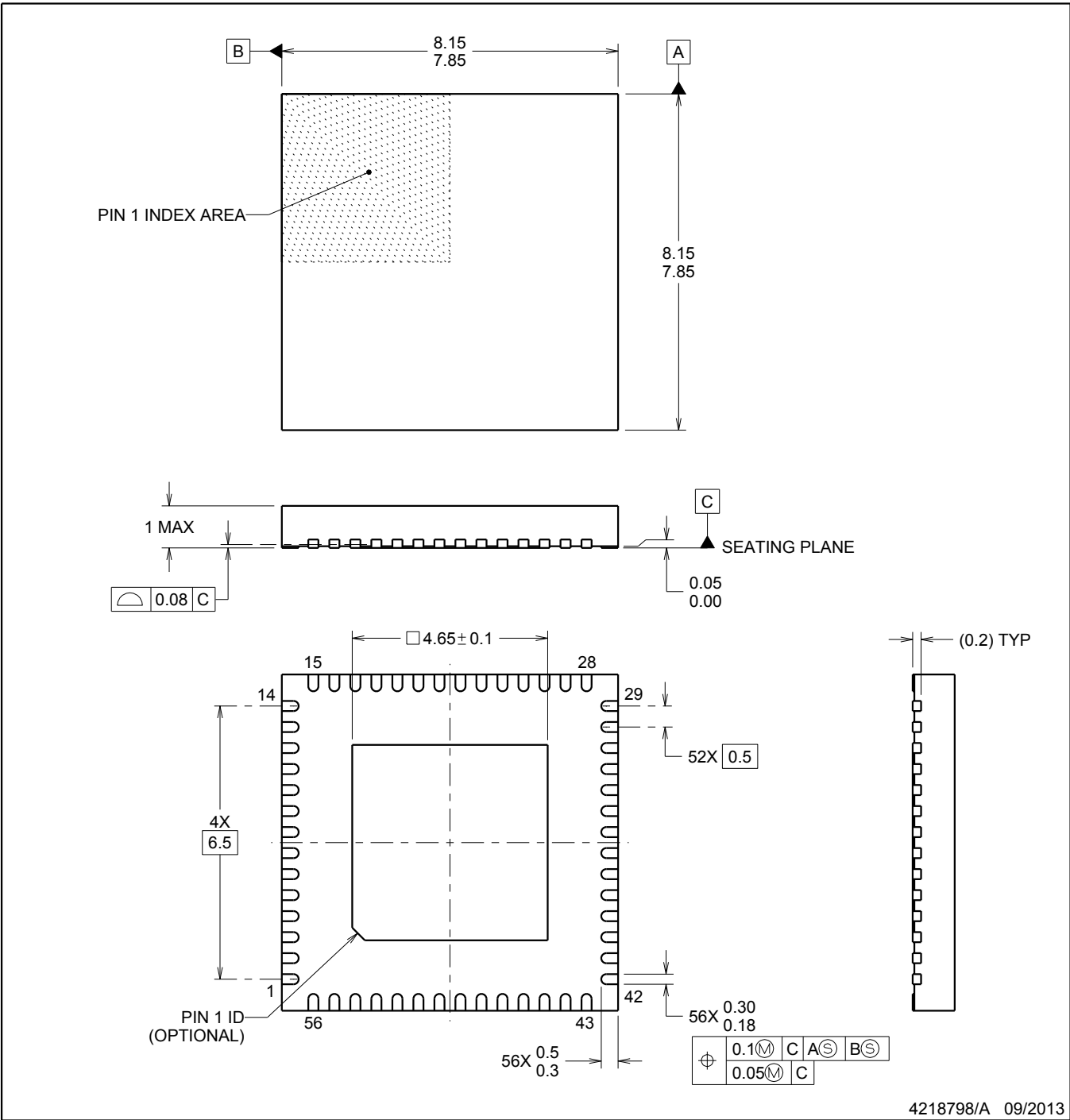
4224653/A



RTQ0056A

VQFN - 1 mm max height

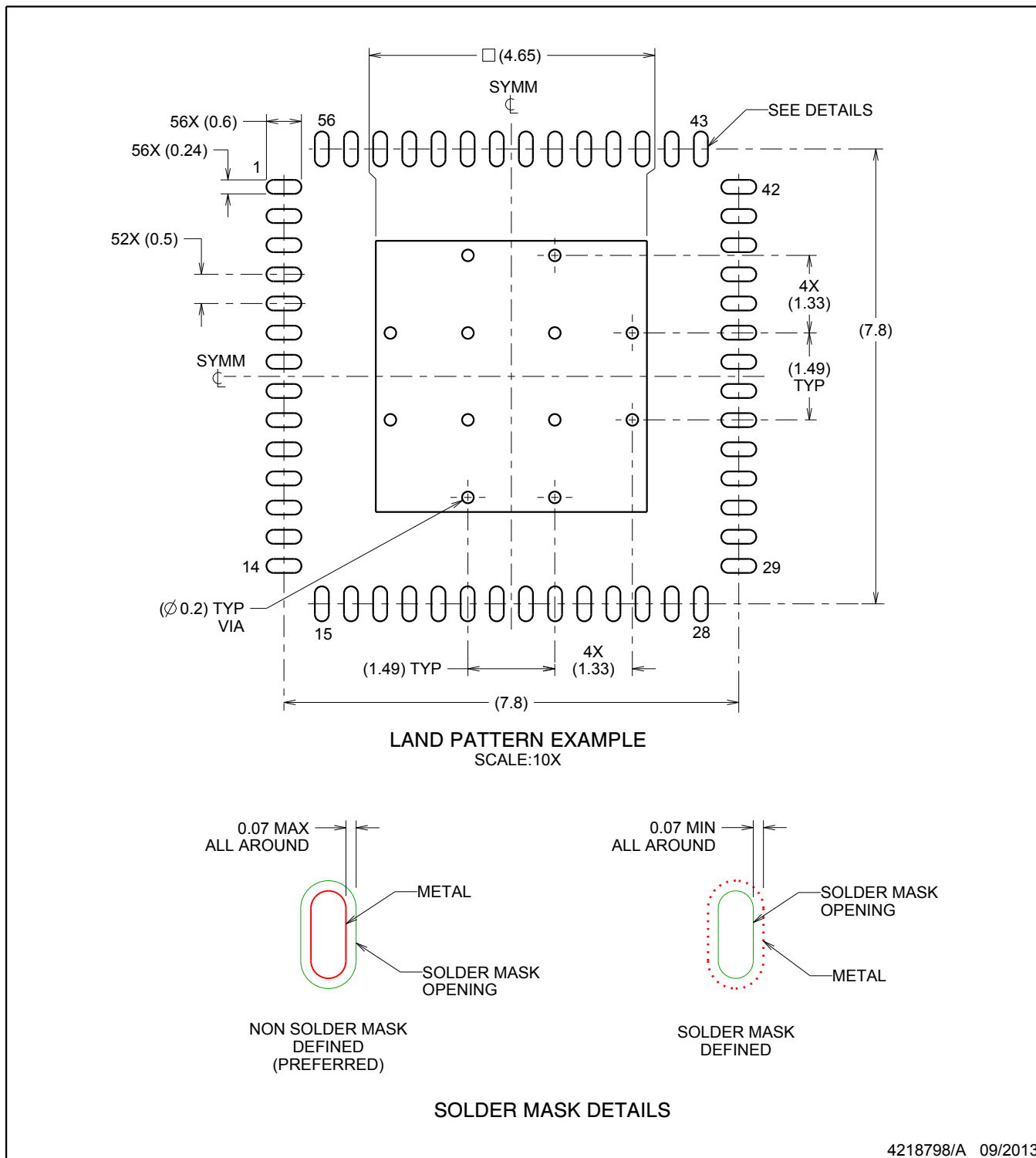
VQFN



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NOTES:

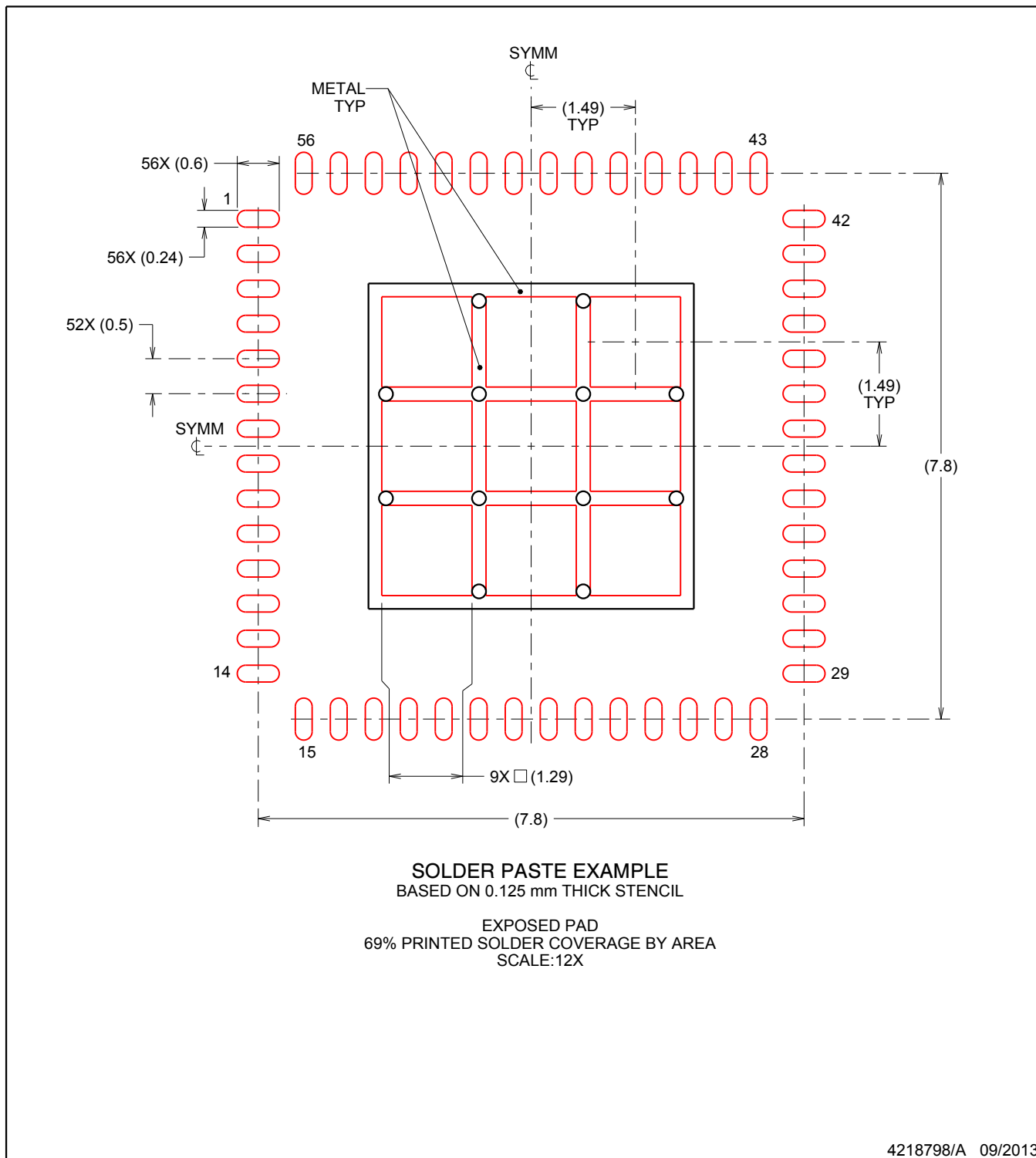
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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