SN75DP139 DisplayPort to TMDS Level-Shifting Re-Driver

1 Features

- DisplayPort Physical Layer Input Port to TMDS Physical Layer Output Port
- Integrated TMDS Level-Shifting Re-driver With Receiver Equalization
- Supports Data Rates up to 3.4 Gbps
- Achieves HDMI 1.4b Compliance
- 3D HDMI Support With TMDS Clock Rates up to 340 MHz
- 4k × 2k Operation (30 Hz, 24bpp)
- Deep Color Supporting 36bpp
- Integrated I^2C Logic Block for DVI/HDMI Connector Recognition
- Integrated Active I^2C Buffer
- Enhanced ESD: 10 kV on All Pins
- Enhanced Commercial Temperature Range: 0°C to 85°C
- 48-Pin 7-mm × 7-mm VQFN (RGZ) Package
- 40-Pin 5-mm × 5-mm WQFN (RSB) Package

2 Applications

- Personal Computer Market
  - DP/TMDS Dongle
  - Desktop PC
  - Notebook PC
  - Docking Station
  - Stand-Alone Video Card

3 Description

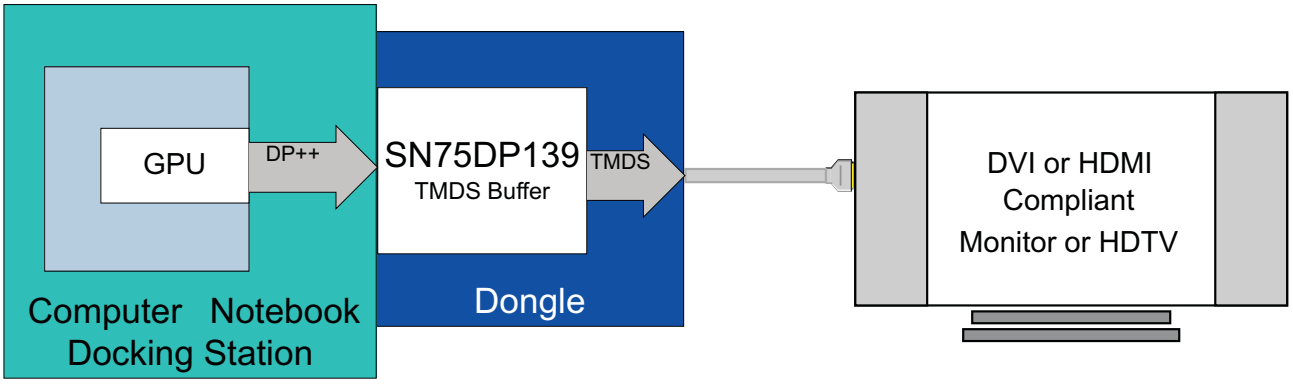
The SN75DP139 is a dual-mode DisplayPort input to Transition-Minimized Differential Signaling (TMDS) output. The TMDS output has a built-in level-shifting re-driver supporting Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.4b standards. The SN75DP139 is specified up to a maximum data rate of 3.4 Gbps, supporting resolutions greater then 1920 × 1200 or HDTV 12-bit color depth at 1080p (progressive scan). The SN75DP139 is compliant with the HDMI 1.4b specifications and supports optional protocol enhancements such as 3D graphics at resolutions demanding a pixel rate up to 340 MHz.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75DP139	VQFN (48)	7.00 mm x 7.00 mm
	WQFN (40)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



GPU - Graphics Processing Unit
DP++ - Dual-Mode DisplayPort
TMDS - Transition-Minimized Differential Signaling
DVI - Digital Visual Interface

HDMI - High Definition Multimedia Interface

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2013) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (December 2012) to Revision D — **Page**

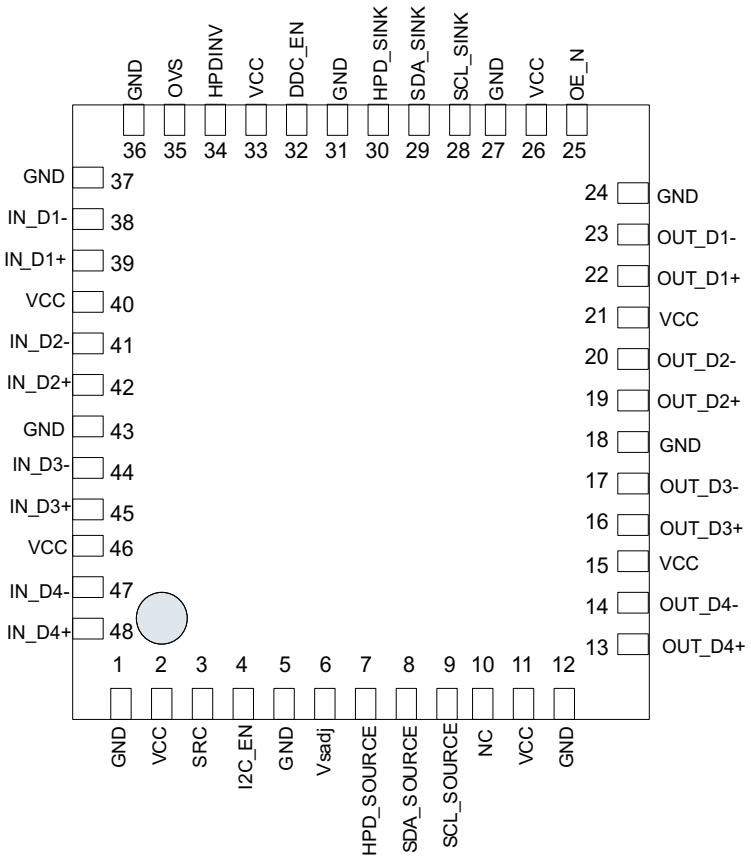
- Changed title and Feature bullet from "...TMDS Translator...." to "...TMDS Level Shifting Re-driver" ... 1
- Changed second sentence text string in Description section from "...built in level translator..." to "built in level shifting re-driver....." ... 1

Changes from Revision A (July 2010) to Revision B — **Page**

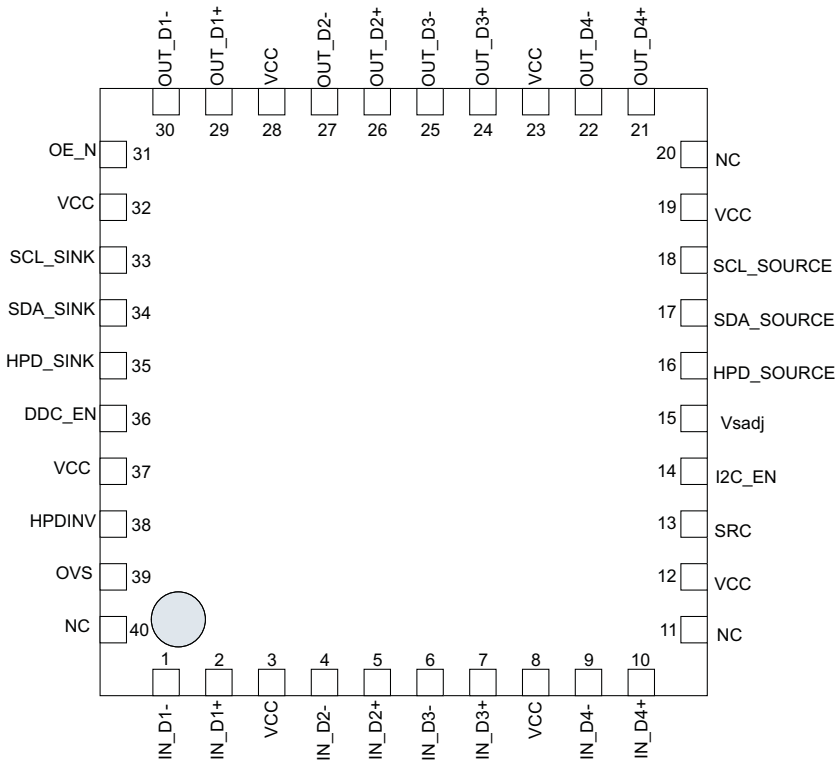
- Added to FEATURES "40 Pin 5 x 5 QFN (RSB) Package" ... 1
- Added RSB package drawing ... 4
- Changed PIN FUNCTIONS to include RSB package pins ... 5
- Added RSB package to ORDERING INFORMATION table ... 5
- Changed voltage range section of Absolute Maximum Ratings ... 6
- Changed input voltages within the Recommended Operating Conditions ... 7
- Changed thermal resistance info and enable voltages to 3.6V ... 7
- Changed enable voltages from 5V to 3.6V ... 8
- Changed $V_{IH(AUX)}$) max from 5.5V to 3.6V ... 9
- Changed OUT_Dx terminal connections ... 17

5 Pin Configuration and Functions

48-PIN VQFN
RGZ PACKAGE
(TOP VIEW)



40-PIN WQFN
RSB PACKAGE
(TOP VIEW)



Pin Functions

PIN			I/O	DESCRIPTION
SIGNAL	NO.			
	RGZ	RSB		
MAIN LINK INPUT PINS				
IN_D1	38, 39	1, 2	I	DisplayPort Main Link Channel 0 Differential Input
IN_D2	41, 42	4, 5	I	DisplayPort Main Link Channel 1 Differential Input
IN_D3	44, 45	6, 7	I	DisplayPort Main Link Channel 2 Differential Input
IN_D4	47, 48	9, 10	I	DisplayPort Main Link Channel 3 Differential Input
MAIN LINK PORT B OUTPUT PINS				
OUT_D1	23, 22	30, 29	O	TMDS Data 2 Differential Output
OUT_D2	20, 19	27, 26	O	TMDS Data 1 Differential Output
OUT_D3	17, 16	25, 24	O	TMDS Data 0 Differential Output
OUT_D4	14, 13	22, 21	O	TMDS Data Clock Differential Output
HOT PLUG DETECT PINS				
HPD_SOURCE	7	16	O	Hot Plug Detect Output
HPD_SINK	30	35	I	Hot Plug Detect Input
AUXILIARY DATA PINS				
SDA_SOURCE, SCL_SOURCE	8, 9	17, 18	I/O	Source Side Bidirectional DisplayPort Auxiliary Data Line
SDA_SINK, SCL_SINK	29, 28	34, 33	I/O	TMDS Port Bidirectional DDC Data Lines
CONTROL PINS				
OE_N	25	31	I	Output Enable and power saving function for High Speed Differential level shifter path.
NC	10	11, 20, 40		No Connect
OVS	35	39	I	DDC I2C buffer offset select
DDC_EN	32	36	I	Enables or Disables the DDC I2C buffer
HPDINV	34	38	I	HPD_SOURCE Logic and Level Select
VSadj	6	15	I	TMDS Compliant Voltage Swing Control
SRC	3	13	I	TMDS outputs rise and fall time select
I2C_EN	4	14	I	Internal I^2C register enable, used for HDMI / DVI connector differentiation
SUPPLY AND GROUND PINS				
VCC	2, 11, 15, 21, 26, 33, 40, 46	3, 8, 12, 19, 23 28, 32, 37		3.3V Supply
GND	1, 5, 12, 18, 24, 27, 31, 36, 37, 43	Thermal Pad		Ground

Table 1. Control Pin Lookup Table

SIGNAL	LEVEL (1)	STATE	DESCRIPTION
OE_N	H	Power Saving Mode	Main Link is disabled. IN_Dx termination = 50 Ω with common mode voltage set to 0V. OUT_Dx outputs = high impedance
	L	Normal Mode	IN_Dx termination = 50 Ω OUT_Dx outputs = active
I^2C_EN	H	HDMI	The Internal I2C register is active and readable when the TMDS port is selected indicating that the connector being used is HDMI. This mode selects the fastest rise and fall time for the TMDS differential output signals
	L	DVI	The Internal I2C register is disabled and not readable when the TMDS port is selected indicating that the connector being used is DVI. This mode selects a slower rise and fall time for the TMDS differential output signals See *Application Information*.

(1) (H) Logic High; (L) Logic Low; (Z) High Z

Table 1. Control Pin Lookup Table (continued)

SIGNAL	LEVEL(1)	STATE	DESCRIPTION
VSadj	4.02 kΩ ±5%	Output Voltage Swing Contol	Driver output voltage swing precision control to aid with system compliance
HPDINV	H	HPD Inversion	HPD_SOURCE VOH =0.9V (typical) and HPD logic is inverted
	L	HPD non-inversion	HPD_SOURCE VOH =3.2V (typical) and HPD logic is non-inverted
SRC	H	Edge Rate: Slowest	SRC helps to slow down the rise and fall time. SRC =High adds ~60ps to the rise and fall time of the TMDS differential output signals in addition to the I2C_EN pin selection (recommended setting)
	L	Edge Rate: Slow	SRC helps to slow down the rise and fall time. SRC =Low adds ~30ps to the rise and fall time of the TMDS differential output signals in addition to the I^2C_EN pin selection
	Hi-Z	Edge Rate	Leaving the SRC pin High Z, will keep the default rise and fall time of the TMDS differential output signals as selected by the I^2C_EN pin. It is recommended that an external resistor-divider (less than 100 kΩ) is used so that voltage on this pin = VCC/2, if Hi-Z logic level is intended on this pin.
OVS	H	Offset 1	DDC source side VOL and VIL offset range 1
	L	Offset 2	DDC source side VOL and VIL offset range 2
	Hi-Z	Offset 3	DDC source side VOL and VIL offset range 3 It is recommended that an external resistor-divider (less than 100 kΩ) is used so that voltage on this pin = VCC/2, if Hi-Z logic level is intended on this pin.
DDC_EN	H	DDC Buffer enabled	DDC Buffer is enabled
	L	DDC buffer disabled	DDC Buffer is disabled

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range(2)	VCC	–0.3	3.6	V
Voltage range	Main Link Input (IN_Dx) differential voltage	–0.3	VCC + 0.3	V
	TMDS Outputs (OUT_Dx)	–0.3	VCC + 0.3	
	HPD_SOURCE, SDA_SOURCE, SCL_SOURCE, OVS, DDC_EN, VSadj, SRC, I^2C_EN	–0.3	VCC + 0.3	
	HPD_SINK, SDA_SINK, SCL_SINK, OE_EN, HPDINV	–0.3	5.5	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model(1)	–10	10	kV
		Charged-device model(2)	–1.5	1.5	
		Machine model(3)	–200	200	V

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(2) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(3) Tested in accordance with JEDEC Standard 22, Test Method A115-A

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage		3	3.3	3.6	V
T_A	Operating free-air temperature		0		85	°C
MAIN LINK DIFFERENTIAL INPUT PINS						
V_{ID_PP}	Peak-to-peak AC input differential voltage		0.15		1.2	V
d_R	Data rate	RGZ package	0.25		3.4	Gbps
		RSB package	0.25		3.4	
$t_{rise\ fall\ time}$	Input Signal Rise and Fall time (20%-80%)		75			ps
V_{PRE}	Pre-emphasis on the Input Signal at IN_Dx pins		0	0	0	db
TMDS DIFFERENTIAL OUTPUT PINS						
AV_{CC}	TMDS output termination voltage		3	3.3	3.6	V
d_R	Data rate	RGZ package	0.25		3.4	Gbps
		RSB package	0.25		3.4	
R_T	Termination resistance		45	50	55	Ω
R_{Vsadj}	TMDS output swing voltage bias resistor(1)		3.65	4.02		kΩ
AUXILIARY AND I2C PINS						
V_I	Input voltage	SDA_SINK, SCL_SINK	0		5.5	V
		SDA_SOURCE, SCL_SOURCE			3.6	
$d_{R(I2C)}$	I^2C data rate				100	kHz
HPD_SINK, HPDINV, OE_N						
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage		0		0.8	V
DDC_EN, I2C_EN						
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage		0		0.8	V
SRC, OVS						
$V_{IH\_SRC\_OVS}$	High-level input voltage		3		3.6	V
$V_{IL\_SRC\_OVS}$	Low-level input voltage		0		0.5	V

(1) R_{Vsadj} resistor controls the SN75DP139 Driver output voltage swing and thus helps in meeting system compliance. It is recommended that R_{Vsadj} resistor should be above the MIN value as indicated in the RECOMMENDED OPERATING CONDITIONS table, however for NOM and MAX value, Figure 19 could be used as reference. It is important to note that system level losses, AV_{CC} and R_T variation affect R_{Vsadj} resistor selection. Worse case variation on system level losses, AV_{CC}, R_T could make R_{Vsadj} resistor value of 4.02 kΩ ±5% result in non-compliant TMDS output voltage swing. In such cases Figure 19 could be used as reference.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX(1)	UNIT
θ_{JB}	Junction-to-board thermal resistance		RGZ package		10.9		°C/W
			RSB package		10.8		
θ_{JCT}	Junction-to-case-top thermal resistance		RGZ package		22.5		°C/W
			RSB package		24.4		
ψ_{JB}	Junction-to-board thermal resistance metric	High-K board(2)	RGZ package		10.9		°C/W
			RSB package		10.8		
ψ_{JT}	Junction-to-top thermal resistance metric	High-K board(2)	RGZ package		0.5		°C/W
			RSB package		0.4		

(1) The maximum rating is simulated under 3.6V V_{CC} unless otherwise noted.
(2) Test conditions for ψ_{JB} and ψ_{JT} are clarified in TI document SPRA953, IC Package Thermal Metrics.

Thermal Information (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
P_{D1}	Device power dissipation(3)	**HDMI Mode:** OE_N = 0V, DDC_EN = 3.6V, V_{CC} = 3.6V, ML: VID_PP = 1200mV, 3Gbps TMDS pattern AUX: V_I = 3.3V, 100 kHz PRBS HPD: HPD_SINK = 5V, I2C_EN = 3.6V, SRC = Hi-Z		270+146	396+146	mW
P_{D2}	Device power dissipation(3)	**DVI Mode:** OE_N = 0V, DDC_EN = 3.6V, V_{CC} = 3.6V, ML: VID_PP = 1200mV, 3Gbps TMDS pattern AUX: V_I = 3.3V, 100 kHz PRBS HPD: HPD_SINK= 5V, I2C_EN = 0V, SRC = Hi-Z		214+146	306+146	mW
P_{SD1}	Device power dissipation under low power with HPDINV = LOW	OE_N = 5V, DDC_EN = 0V, HPDINV = 0V, HPD_SINK = 0V		18	54	µW
P_{SD2}	Device power dissipation under low power with HPDINV =HIGH	OE_N = 5V, DDC_EN = 0V, HPDINV = 5V		1.7	3	mW
P_{SD3}	Device power dissipation under low power with DDC enabled with HPDINV = HIGH	OE_N = 5V, DDC_EN = 3.6V, HPDINV = 5V		16.5	29	mW
P_{SD4}	Device power dissipation under low power with DDC enabled with HPDINV = LOW	OE_N = 5V, DDC_EN = 3.6V, HPDINV = 0V		15	26	mW

(3) Power dissipation is the sum of the power consumption from the VCC pins, plus the 146 mW of power from the AVCC (HDMI/DVI Receiver Termination Supply).

6.5 Electrical Characteristics (Device Power)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current (HDMI Mode)	**HDMI Mode:** OE_N = 0V, DDC_EN = 3.6 V, V_{CC} = 3.6 V, ML: VID_PP = 1200 mV, 3 Gbps TMDS pattern AUX: V_I = 3.3 V, 100 kHz PRBS HPD: HPD_SINK = 5 V, I2C_EN = 3.6 V, SRC = Hi-Z		82	110	mA
I_{CC2}	Supply Current (DVI Mode)	**DVI Mode:** OE_N = 0V, DDC_EN = 3.6 V, V_{CC} = 3.6 V, ML: VID_PP = 1200 mV, 3 Gbps TMDS pattern AUX: V_I = 3.3 V, 100 kHz PRBS HPD: HPD_SINK= 5 V, I2C_EN = 0 V, SRC = Hi-Z		65	85	mA
I_{SD1}	Shutdown current with HPDINV = LOW	OE_N = 5 V, DDC_EN = 0 V, HPDINV = 0 V, HPD_SINK = 0 V		5.5	15	µA
I_{SD2}	Shutdown current with HPDINV = HIGH	OE_N = 5 V, DDC_EN = 0 V, HPDINV = 5 V		0.5	0.8	mA
I_{SD3}	Shutdown current with DDC enabled with HPDINV = HIGH	OE_N = 5 V, DDC_EN = 3.6 V, HPDINV = 5 V		5	8	mA
I_{SD4}	Shutdown current with DDC enabled with HPDINV = LOW	OE_N = 5 V, DDC_EN = 3.6 V, HPDINV = 0 V		4.5	7.2	mA

6.6 Electrical Characteristics (Hot Plug Detect)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH3.3}$	High-level output voltage	I_{OH} = –100 µA, V_{CC} = 3.3 V ±10%, HPDINV = LOW	2.8		3.6	V
$V_{OH1.1}$	High-level output voltage	I_{OH} = –100 µA, V_{CC} = 3.3 V ±10%, HPDINV = HIGH	0.8		1.1	V
V_{OL}	Low-level output voltage	I_{OH} = 100 µA	0		0.1	V

Electrical Characteristics (Hot Plug Detect) (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	V_{IH} = 2.0 V, V_{CC} = 3.6 V	–30		30	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V, V_{CC} = 3.6 V	–30		30	µA
R_{INTHPD}	Input pull down on HPD_SINK (HPD Input)		110	130	160	kΩ

6.7 Electrical Characteristics (Aux / I²C Pins)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	Low input current		V_{CC} = 3.6 V, V_I = 0 V	–10		10	µA
$I_{lkg(AUX)}$	Input leakage current	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)	V_{CC} = 3.6V, V_I = 3.6 V	–10		10	µA
$C_{IO(AUX)}$	Input/Output capacitance	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)	DC bias = 1.65 V, AC = 2.1Vp-p, f = 100 kHz			15	pF
$V_{IH(AUX)}$	High-level input voltage	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)		1.6		3.6	V
$V_{IL1(AUX)}$	Low-level input voltage	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)	OVS = HIGH	–0.2		0.36	V
$V_{OL1(AUX)}$	Low-level output voltage	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)	I_O = 3 mA, OVS = HIGH	0.6		0.7	V
$V_{IL2(AUX)}$	Low-level input voltage	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)	OVS = Hi-Z	–0.2		0.36	V
$V_{OL2(AUX)}$	Low-level output voltage	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)	I_O = 3 mA, OVS = Hi-Z	0.5		0.6	V
$V_{IL3(AUX)}$	Low-level input voltage	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)	OVS = Low	–0.2		0.27	V
$V_{OL3(AUX)}$	Low-level output voltage	AUX_I²C pins (SCL_SOURCE, SDA_SOURCE)	I_O = 3 mA, OVS = Low	0.4		0.5	V
$I_{lkg(I2C)}$	Input leakage current	I²C SDA/SCL pins (SCL_SINK, SDA_SINK)	V_{CC} = 3.6 V, V_I = 4.95 V	–10		10	µA
$C_{IO(I2C)}$	Input/Output capacitance	I²C SDA/SCL pins (SCL_SINK, SDA_SINK)	DC bias = 2.5 V, AC = 3.5Vp-p, f = 100 kHz			15	pF
$V_{IH(I2C)}$	High-level input voltage	I²C SDA/SCL pins (SCL_SINK, SDA_SINK)		2.1		5.5	V
$V_{IL(I2C)}$	Low-level input voltage	I²C SDA/SCL pins (SCL_SINK, SDA_SINK)		–0.2		1.5	V
$V_{OL(I2C)}$	Low-level output voltage	I²C SDA/SCL pins (SCL_SINK, SDA_SINK)	I_O = 3mA			0.2	V

6.8 Electrical Characteristics (TMDS and Main Link Pins)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Single-ended HIGH level output voltage	AVCC = 3.3 V, R_T = 50 Ω,	AVCC–10		AVCC+10	mV
V_{OL}	Single-ended LOW level output voltage		AVCC–600		AVCC-400	mV
V_{SWING}	Single-ended output voltage swing		400		600	mV
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–5		5	mV
$V_{OD(PP)}$	Peak-to-Peak output differential voltage		800		1200	mV
$V_{(O)SBY}$	Single-ended standby output voltage	AVCC = 3.3 V, R_T = 50 Ω, OE_N = High	AVCC–10		AVCC+10	mV
$I_{(O)OFF}$	Single-ended power down output current	0V ≤ VCC ≤ 1.5 V, AVCC = 3.3 V, R_T = 50Ω	–10		10	µA
I_{OS}	Short circuit output current	See Figure 14	–15		15	mA
R_{INT}	Input termination impedance		40	50	60	Ω
V_{term}	Input termination voltage		1		2	V

6.9 Switching Characteristics (Hot Plug Detect)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(HPD)}$	Propagation delay	V_{CC} = 3.6 V	2		30	ns

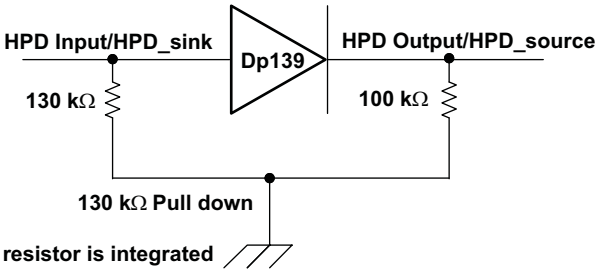


Figure 1. HPD Test Circuit (HPDINV = LOW)

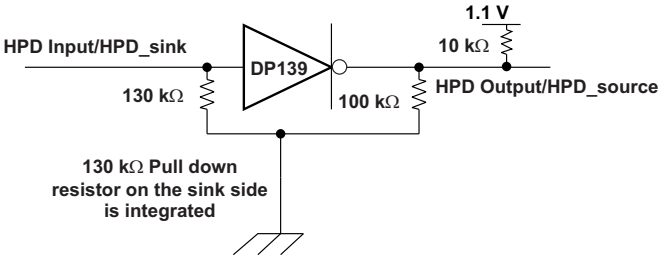


Figure 2. HPD Test Circuit (VOH =1.1), HPDINV = HIGH

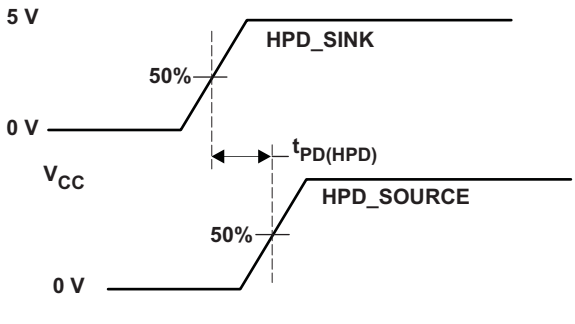


Figure 3. HPD Timing Diagram (HPDINV = LOW)

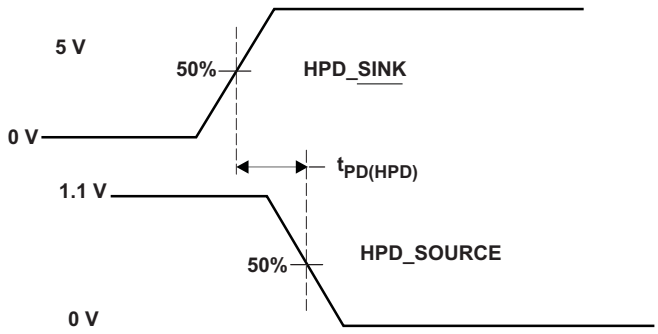


Figure 4. HPD Timing Diagram (HPDINV = HIGH)

6.10 Switching Characteristics (Aux / I²C Pins)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Propagation delay time, low to high	Source to Sink	204		600	ns
t_{PHL1}	Propagation delay time, high to low	Source to Sink	35		200	ns
t_{PLH2}	Propagation delay time, low to high	Sink to Source	80		251	ns
t_{PHL2}	Propagation delay time, high to low	Sink to Source	35		200	ns
t_{f1}	Output signal fall time	Sink Side	20		72	ns
t_{f2}	Output signal fall time	Source Side	20		72	ns
f_{SCL}	SCL clock frequency for internal register	Source Side			100	kHz
$t_{W(L)}$	Clock LOW period for I²C register	Source Side	4.7			µs
$t_{W(H)}$	Clock HIGH period for internal register	Source Side	4.0			µs
t_{SU1}	Internal register setup time, SDA to SCL	Source Side	250			ns
$t_{h(1)}$	Internal register hold time, SCL to SDA	Source Side	0			µs
$T_{(buf)}$	Internal register bus free time between STOP and START	Source Side	4.7			µs
$t_{su(2)}$	Internal register setup time, SCL to START	Source Side	4.7			µs
$t_{h(2)}$	Internal register hold time, START to SCL	Source Side	4.0			µs
$t_{su(3)}$	Internal register hold time, SCL to STOP	Source Side	4.0			µs

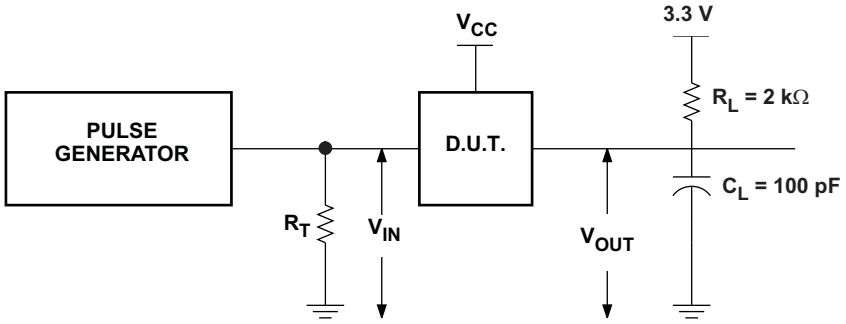


Figure 5. Source Side Test Circuit (SCL_SOURCE, SDA_SOURCE)

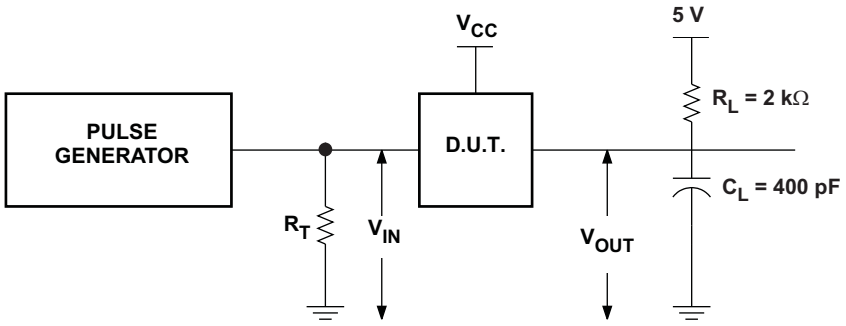


Figure 6. Sink Side Test Circuit (SCL_SINK,SDA_SINK)

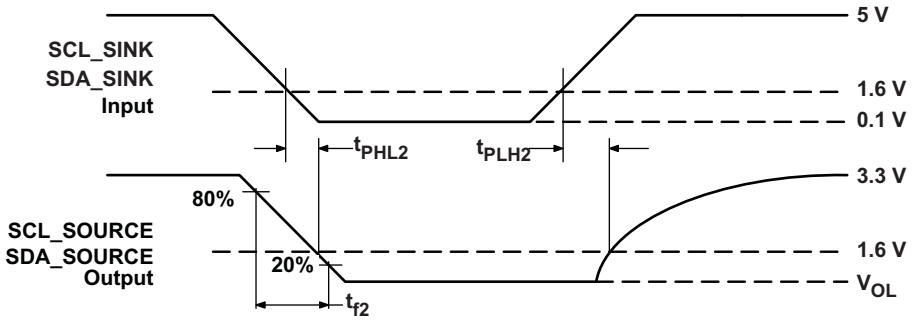


Figure 7. Source Side Output AC Measurements

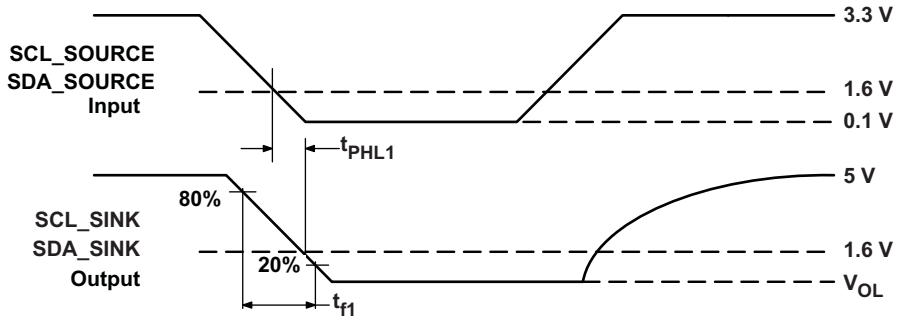


Figure 8. Sink Side Output AC Measurements

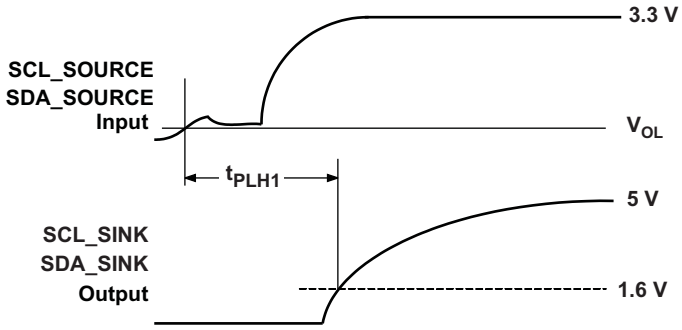


Figure 9. Sink Side Output AC Measurements Continued

6.11 Switching Characteristics (TMDS and Main Link Pins)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time	AVCC=3.3 V, R_T = 50 Ω, f = 1MHz, R_{Vsadj} = 4.02 kΩ	250	350	600	ps
t_{PHL}	Propagation delay time		250	350	600	ps
t_{R1}	Rise Time (I2C_EN = HI, SRC = Hi-Z)		60	85	120	ps
t_{F1}	Fall Time (I2C_EN = HI, SRC = Hi-Z)		60	85	120	ps
t_{R2}	Rise Time (I2C_EN = Low, SRC = Hi-Z)			115	150	ps
t_{F2}	Fall Time (I2C_EN = Low, SRC = Hi-Z)			115	150	ps
t_{R3}	Rise Time (I2C_EN = HI, SRC = HI)			150	180	ps
t_{F3}	Fall Time (I2C_EN = HI, SRC = HI)			150	180	ps
t_{R4}	Rise Time (I2C_EN = HI, SRC = Low)			115	150	ps
t_{F4}	Fall Time (I2C_EN = HI, SRC = Low)			115	150	ps
t_{R5}	Rise Time (I2C_EN = Low, SRC = HI)			175	220	ps
t_{F5}	Fall Time (I2C_EN = Low, SRC = HI)			175	220	ps
t_{R6}	Rise Time (I2C_EN = Low, SRC = Low)			150	180	ps
t_{F6}	Fall Time (I2C_EN = Low, SRC = Low)			150	180	ps
$t_{SK(P)}$	Pulse skew			8	15	ps
$t_{SK(D)}$	Intra-pair skew			20	65	ps
$t_{SK(O)}$	Inter-pair skew			20	100	ps
$t_{JITD(PP)}$	Peak-to-peak output residual data jitter	AVCC = 3.3 V, R_T = 50Ω, dR = 3Gbps, TMDS output slew rate (default). R_{Vsadj} = 4.02 kΩ (refer to Figure 13)		14	50	ps
$t_{JITC(PP)}$	Peak-to-peak output residual clock jitter	AVCC = 3.3 V, R_T = 50Ω, f = 300 MHz TMDS output slew rate (default). R_{Vsadj}= 4.02 kΩ (refer to Figure 13)		8	30	ps

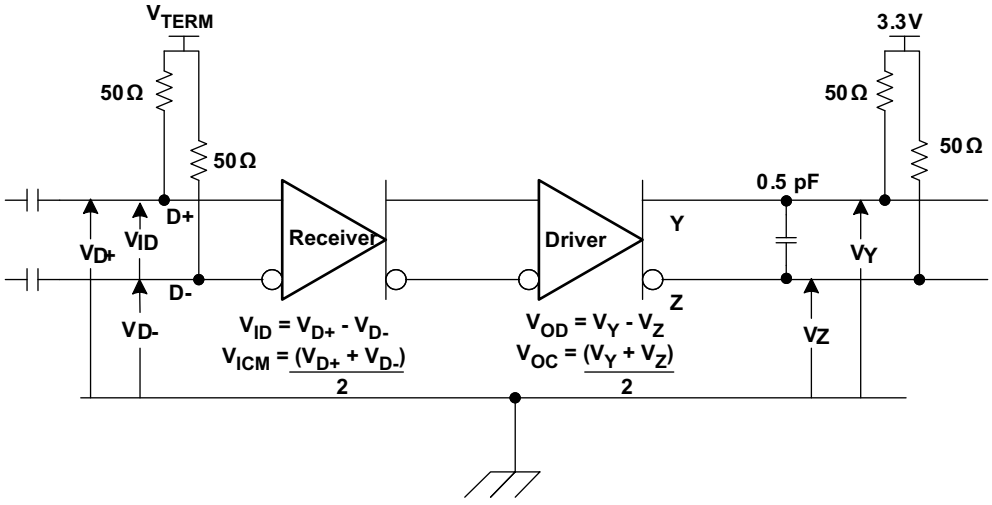


Figure 10. TMDS Main Link Test Circuit

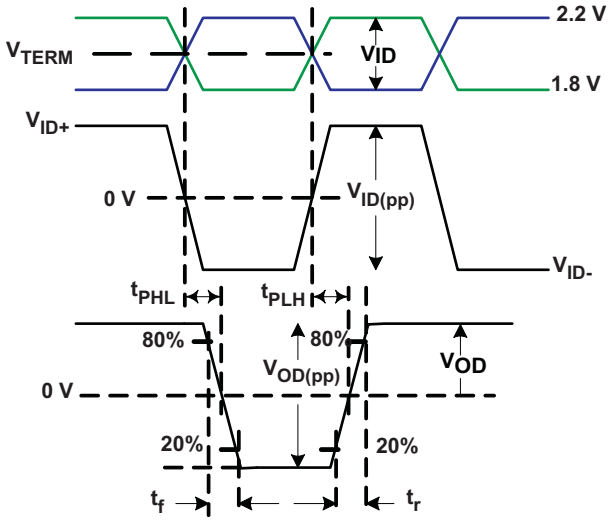


Figure 11. TMDS Main Link Timing Measurements

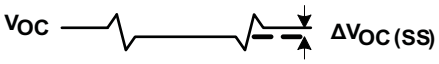
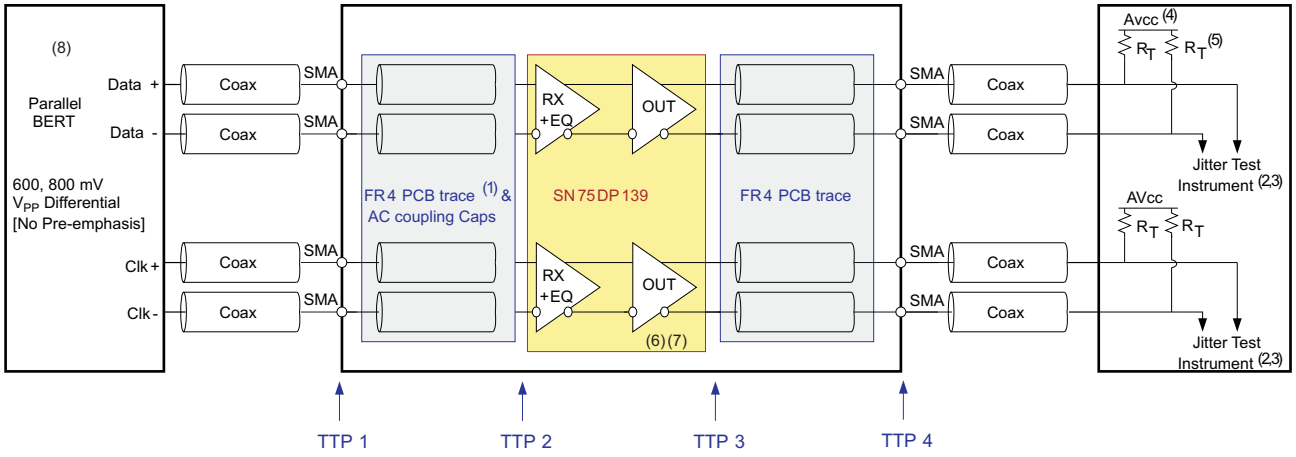


Figure 12. TMDS Main Link Common Mode Measurements



1. The FR4 trace between TTP1 and TTP2 is designed to emulate 1-8" of FR4, AC coupling cap, connector and another 1-8" of FR4. Trace width - 4 mils.
2. All Jitter is measured at a BER of 10^{-9}
3. Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1
4. AVCC = 3.3V
5. RT = 50Ω,
6. Jitter data is taken with SN75DP139 configured in the fastest slew rate setting(default)
7. Rvsadj = 4.02kΩ
8. The input signal from parallel BERT does not have any pre-emphasis. Refer to recommended operating conditions

Figure 13. TMDS Jitter Measurements

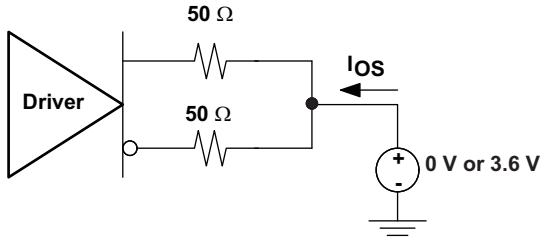


Figure 14. TMDS Main Link Short Circuit Output Circuit

6.12 Typical Characteristics

AVCC = 3.3 V, R_T = 50 Ω

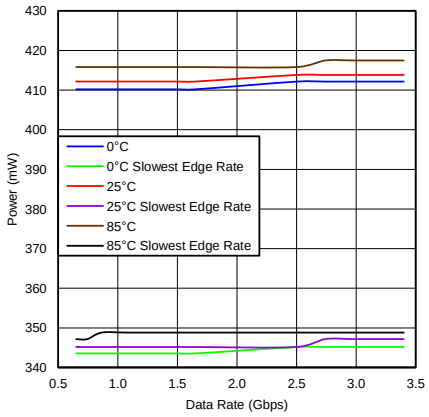


Figure 15. Power Dissipation vs Data Rate

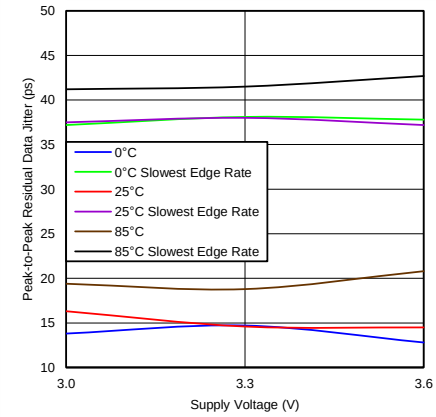


Figure 16. Residual Jitter of 3 Gbps vs Supply Voltage

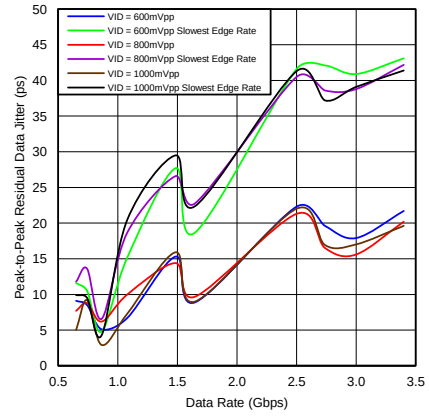


Figure 17. Residual Jitter vs Data Rate (RGZ Package)

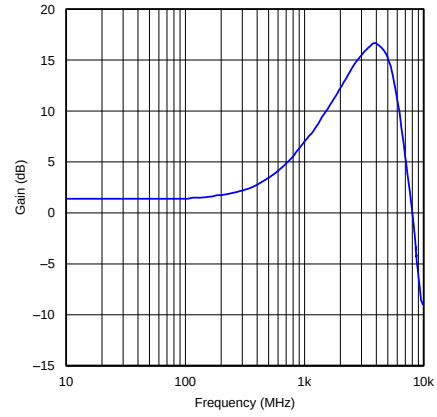


Figure 18. Gain vs Frequency

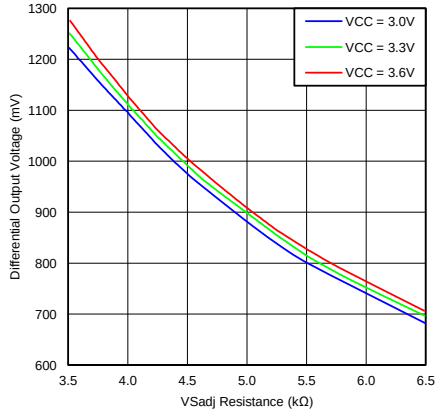


Figure 19. VOD vs V_{SADJ}

7 Detailed Description

7.1 Overview

The SN75DP139 is a Dual-Mode DisplayPort input to Transition-Minimized Differential Signaling (TMDS) output. The TMDS output has a built in level shifting re-driver supporting Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.4b standards.

An integrated Active I2C buffer isolates the capacitive loading of the source system from that of the sink and interconnecting cable. This isolation improves overall signal integrity of the system and allows for considerable design margin within the source system for DVI / HDMI compliance testing.

A logic block was designed into the SN75DP139 in order to assist with TMDS connector identification. Through the use of the I2C_EN pin, this logic block can be enabled to indicate the translated port is an HDMI port; therefore legally supporting HDMI content.

7.2 Functional Block Diagram

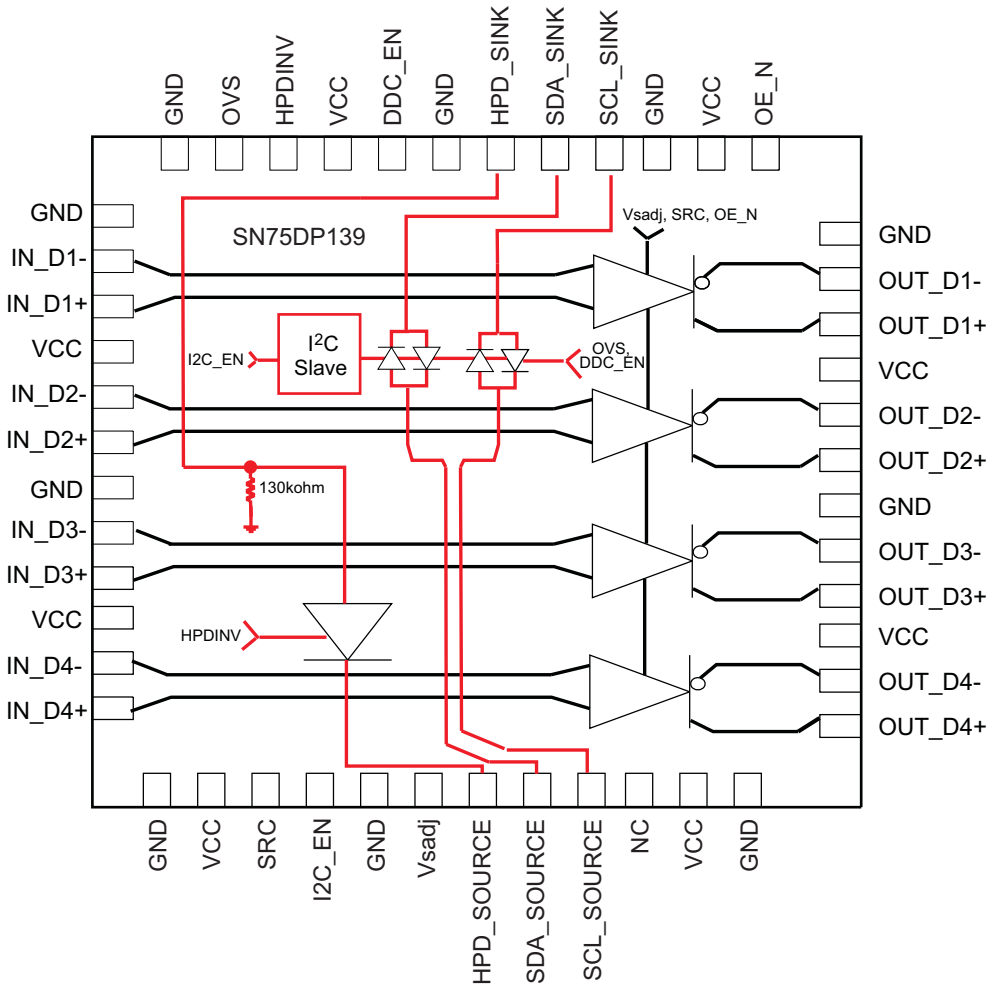


Figure 20. Data Flow Block Diagram

7.3 Feature Description

The SN75DP139 is designed to operate off of one supply voltage VCC.

The SN75DP139 offers features to enable or disable different functionality based on the status of the output enable (OE_N) and DDC Enable (DDC_EN) inputs.

- OE_N affects only the High Speed Differential channels (Main Link/TMDS link). OE_N has no influence on the HPD_SINK input, HPD_SOURCE output, or the DDC buffer.
- DDC_EN affects only the DDC channel. The DDC_EN should never change state during the I2C operation. Disabling DDC_EN during a bus operation will hang the bus, while enabling the DDC_EN during bus traffic will corrupt the I2C bus operation. DDC_EN should only be toggled while the bus is idle.
- TMDS output edge rate control has impact on the SN75DP139 Active power. See Figure 15. TMDS output edge rate can be controlled by SRC pin. Slower output Edge Rate Setting helps in reducing the Active power consumption.

Table 2. Packaging Options

HPD_SINK	HPDINV	OE_N	DDC_EN	IN_Dx	OUT_Dx	DDC	HPD_SOURCE	MODE
Input = H or L	L	L	L	50 Ω termination active	Enabled	High-impedance	Output = non inverted, follows HPD_SINK	Active
Input = H or L	L	L	H	50 Ω termination active	Enabled	enabled	Output = non inverted, follows HPD_SINK	Active
Input = H or L	L	H	L	50 Ω termination active: Terminations connected to common Mode Voltage = 0V.	High-impedance	High-impedance	Output = non inverted, follows HPD_SINK	Low Power
Input = H or L	L	H	H	50 Ω termination active: Terminations connected to common Mode Voltage = 0V.	High-impedance	enabled	Output = non inverted, follows HPD_SINK	Low Power with DDC channel enabled
Input = H or L	H	L	L	50 Ω termination active	Enabled	High-impedance	Output = inverted, follows HPD_SINK	Active
Input = H or L	H	L	H	50 Ω termination active	Enabled	enabled	Output = inverted, follows HPD_SINK	Active
Input = H or L	H	H	L	50 Ω termination active: Terminations connected to common Mode Voltage = 0V.	High-impedance	High-impedance	Output = inverted, follows HPD_SINK	Low Power
Input = H or L	H	H	H	50 Ω termination active: Terminations connected to common Mode Voltage = 0V.	High-impedance	enabled	Output = inverted, follows HPD_SINK	Low Power with DDC channel enabled
L = LOW, H = HIGH								

7.3.1 Hot Plug Detect

The SN75DP139 has a built in level shifter for the HPD outputs. The output voltage level of the HPD pin is defined by the voltage level of the VCC pin. The HPD input or HPD_SINK side has 130kohm of pull down resistor integrated.

The logic of the HPD_SOURCE output always follows the logic state of the HPD_SINK input based on the HPDINV pin logic, regardless of whether the device is in Active or Low Power Mode

7.3.2 Aux / I²C Pins

The SN75DP139 utilizes an active I²C repeater. The repeater is designed to isolate the parasitic effects of the system in order to aid with system level compliance.

In addition to the I²C repeater, the SN75DP139 also supports the connector detection I²C register. This register is enabled via the I²C_EN pin. When active an internal memory register is readable via the AUX_I²C I/O. The functionality of this register block is described in the *Programming* section.

7.3.3 TMDS and Main Link Pins

The main link inputs are designed to support DisplayPort 1.1 specification. The TMDS outputs of the SN75DP139 are designed to support the Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.4b specifications. The differential output voltage swing can be fine tuned with the R_{Vsadj} resistor.

The DP++ (dual-mode) input of the SN75DP139 is designed to accommodate the standard DP level ac coupled signal with no pre-emphasis with up to 16 inches of trace (4 mil 100 Ω differential stripline).

7.3.4 Input/Output Equivalent Circuits

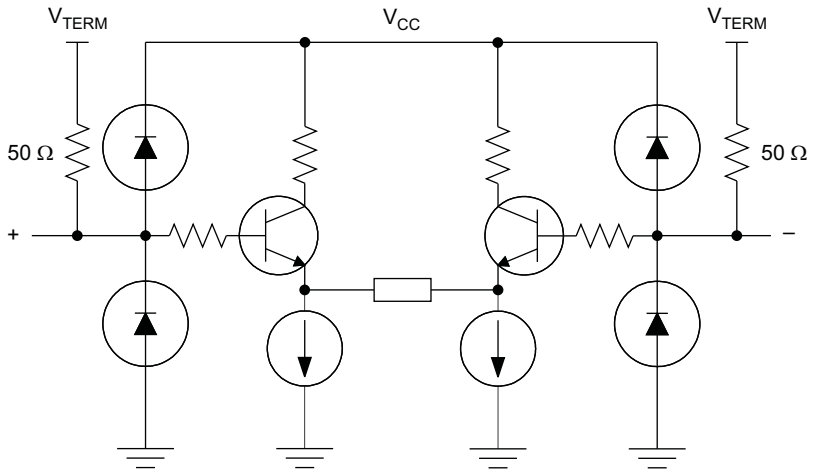


Figure 21. DisplayPort Input Stage

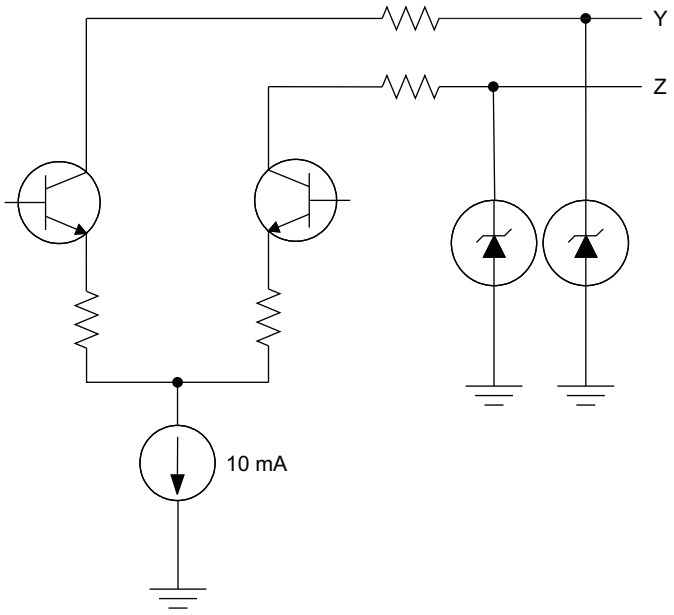


Figure 22. TMDS Output Stage

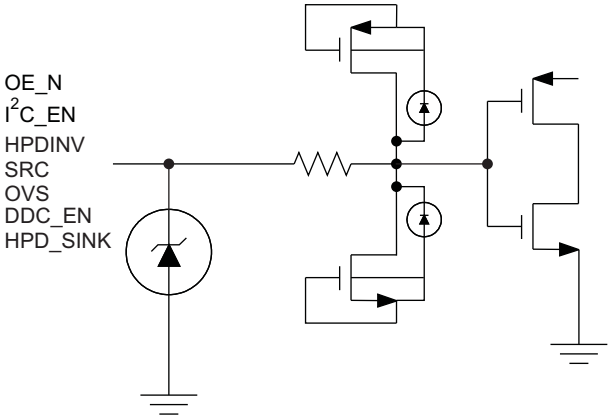


Figure 23. HPD and Control Input Stage

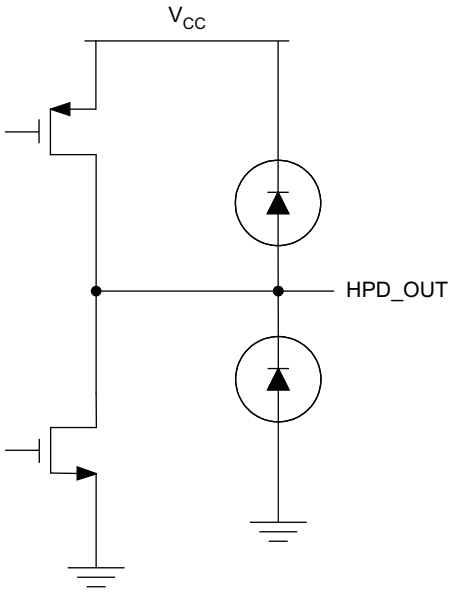


Figure 24. HPD Output Stage

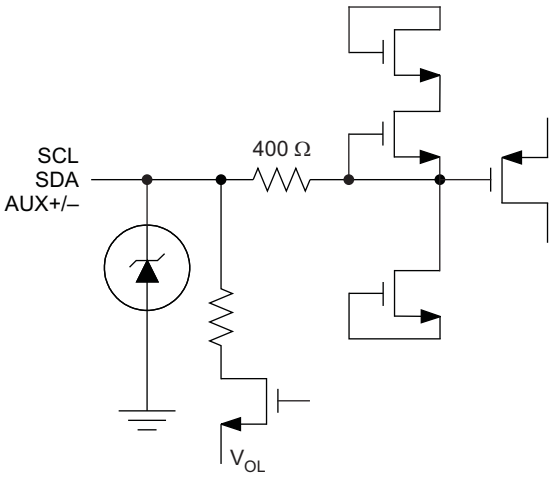


Figure 25. I^2C Input and Output Stage

7.4 Device Functional Modes

7.4.1 Active

The SN75DP139 activates the main link channel and thus is able to transmit the TMDS content.

7.4.2 Low Power With DDC Channel Enabled

The SN75DP139 is in low power but keeps its DDC channel active, this allows the device to configure its internal I2C registers.

7.4.3 Low Power

The SN75DP139 is in the lowest power mode, with no activity on the DDC or main link channels.

7.5 Programming

7.5.1 I²C Interface Notes

The I²C interface can be used to access the internal memory of the SN75DP139. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device. The SN75DP139 works as a slave and supports the standard mode transfer (100 kbps) as defined in the I²C-Bus Specification.

The basic I²C start and stop access cycles are shown in Figure 26.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

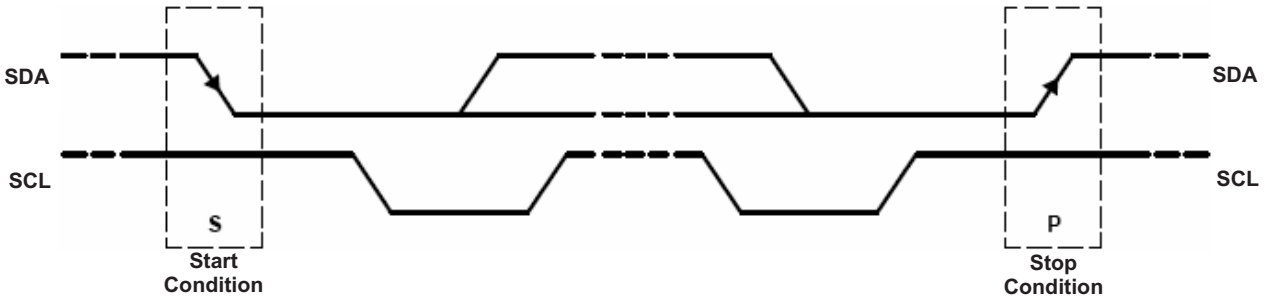


Figure 26. I²C Start And Stop Conditions

7.5.2 General I²C Protocol

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 28. All I²C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data condition* requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 27). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 28) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either *transmit* data to the slave (R/W bit 0) or *receive* data from the slave (R/W bit 1). In either case, the receiver needs to acknowledge the data sent by the *transmitter*. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (See Figure 29).
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 29). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a *stop condition*, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

Programming (continued)

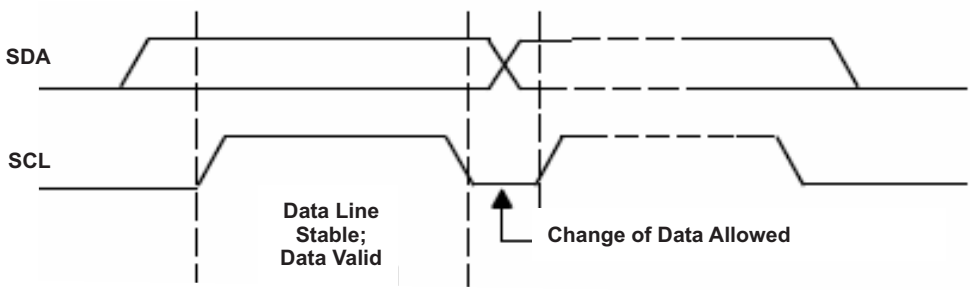


Figure 27. I²C Bit Transfer

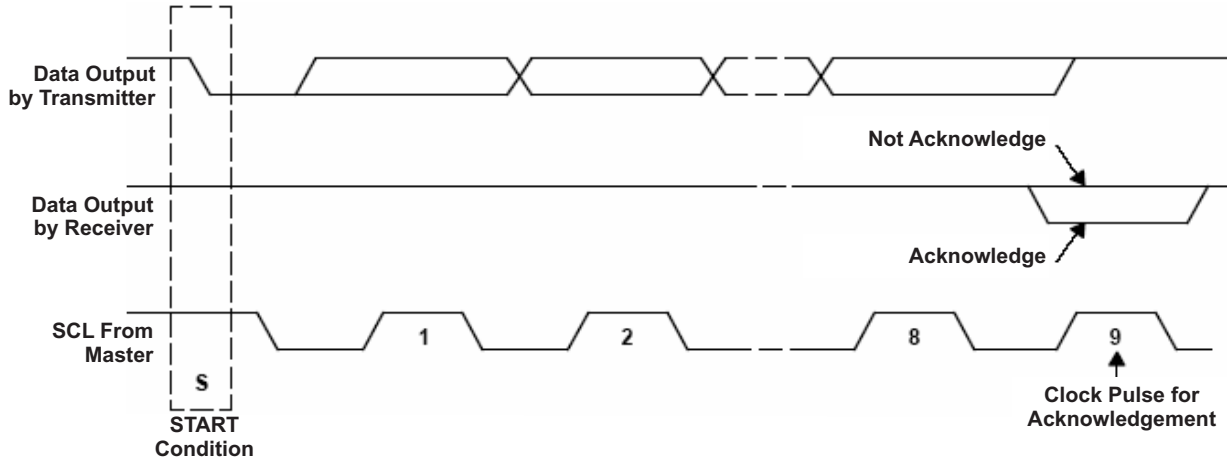


Figure 28. I²C Acknowledge

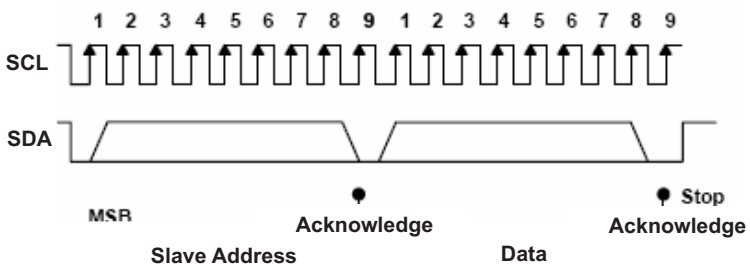


Figure 29. I²C Address And Data Cycles

During a read cycle, the slave receiver will acknowledge the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 30 and Figure 31. See Example – Reading from the SN75DP139 section for more information.

Programming (continued)

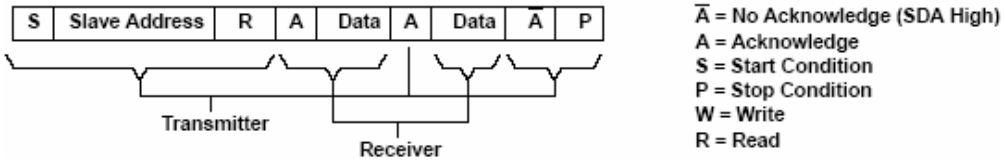


Figure 30. I²C Read Cycle

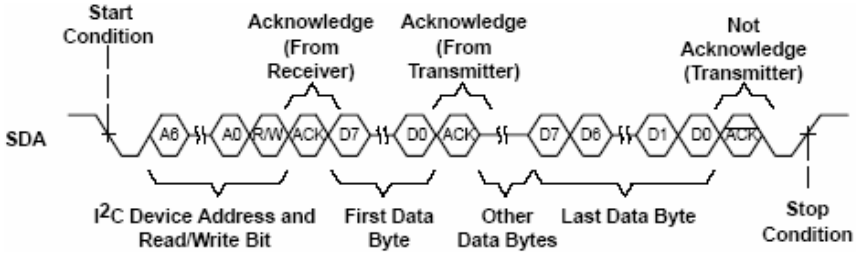


Figure 31. Multiple Byte Read Transfer

7.5.3 Slave Address

Both SDA and SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I²C specification that ranges from 2kΩ to 19kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The 7-bit address is factory preset to 1000000. Table 3 lists the calls that the SN75DP139 will respond to.

Table 3. SN75DP139 Slave Address

Fixed Address							Read/Write Bit
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (R/W)
1	0	0	0	0	0	0	1

7.5.3.1 Sink Port Selection Register And Source Plug-In Status Register Description (Sub-Address)

The SN75DP139 operates using a multiple byte transfer protocol similar to Figure 31. The internal memory of the SN75DP139 contains the phrase “DP-HDMI ADAPTOR<EOT>” converted to ASCII characters. The internal memory address registers and the value of each can be found in Table 4.

During a read cycle, the SN75DP139 will send the data in its selected sub-address in a single transfer to the master device requesting the information. See the ***Example – Reading from the SN75DP139*** section of this document for the proper procedure on reading from the SN75DP139.

Table 4. SN75DP139 Sink Port And Source Plug-In Status Registers Selection

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	0x10
Data	44	50	2D	48	44	4D	49	20	41	44	41	50	54	4F	52	04	FF

7.5.3.2 Example – Reading From The SN75DP139:

The read operation consists of several steps. The I²C master begins the communication with the transmission of the start sequence followed by the slave address of the SN75DP139 and logic address of 00h. The SN75DP139 will acknowledge it’s presence to the master and begin to transmit the contents of the memory registers. After each byte is transferred the SN75DP139 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master. If an ACK is received the next byte of data will be transmitted. If a NACK is received the data transmission sequence is expected to end and the master should send the stop command.

The SN75DP139 will continue to send data as long as the master continues to acknowledge each byte transmission. If an ACK is received after the transmission of byte 0x0F the SN75DP139 will transmit byte 0x10 and continue to transmit byte 0x10 for all further ACK's until a NACK is received.

The SN75DP139 also supports an accelerated read mode where steps 1–6 can be skipped.

SN75DP139 Read Phase

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address Write (Master)	1	0	0	0	0	0	0	0

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Logic Address (Master)	0	0	0	0	0	0	0	0

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	0
I^2C Stop (Master)	P

Step 7	0
I^2C Start (Master)	S

Step 8	7	6	5	4	3	2	1	0
I^2C General Address Read (Master)	1	0	0	0	0	0	0	1

Step 9	9
I^2C Acknowledge (Slave)	A

Step 10	7	6	5	4	3	2	1	0
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the Logic values Contained in the Sink Port Register

Step 11	9
I^2C Not-Acknowledge (Master)	X

Where X is an A (Acknowledge) or $\overline{A}$ (Not-Acknowledge)
An A causes the pointer to increment and step 10 is repeated.
An $\overline{A}$ causes the slave to stop transmitting and proceeds to step 12.

Step 12	0
I^2C Stop (Master)	P

8 Application and Implementation

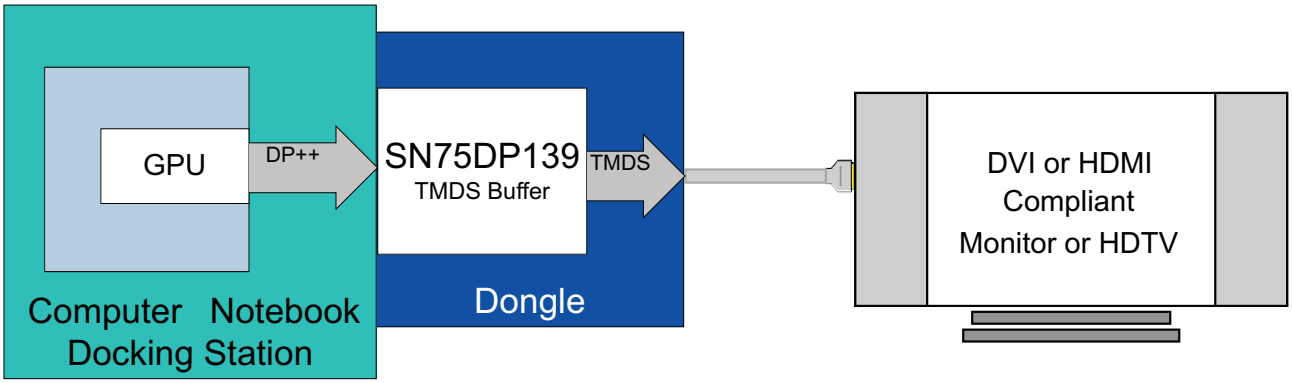
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The typical application for the SN75DP139 is to translate from DP++ to TMDS, and thus expand the connectivity for any DP++ source to HDMI 1.4b and DVI sinks. This can be clearly explained when you have the SN75DP139 in a dongle connected to the DP++ source.

8.2 Typical Application



GPU - Graphics Processing Unit
DP++ - Dual-Mode DisplayPort
TMDS - Transition-Minimized Differential Signaling
DVI - Digital Visual Interface

HDMI - High Definition Multimedia Interface

Figure 32. Typical Application

8.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
VDD Main Power Supply	3.0 - 3.6 V
Main Link Peak-to-Peak AC Input Differential Voltage	0.15 - 1.2 V
TMDS Output Termination Voltage	3.0 - 3.6 V
TMDS Output Swing Voltage Bias Resistor	3.65 - 4.02 kΩ

8.2.2 Detailed Design Procedure

8.2.2.1 DVI Application

In DVI application case, it is recommended that between the SN75DP139 TMDS outputs (OUT_Dx) and a through hole DVI connector that a series resistor placeholder is incorporated. This could help in case if there are signal integrity issues as well as help pass system level compliance.

8.2.3 Application Curve

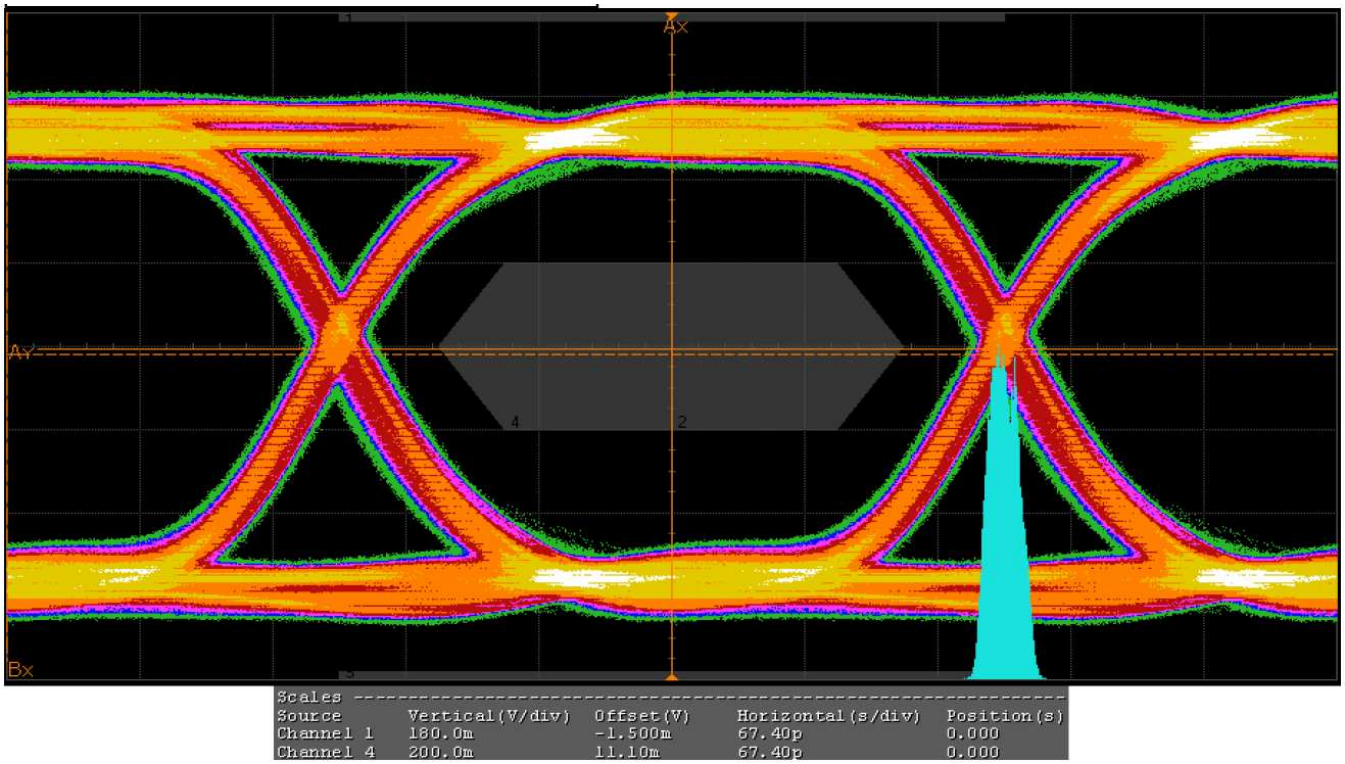


Figure 33. Data Jitter

9 Power Supply Recommendations

Use a VCC power rail able to supply 110 mA for the SN75DP139, Place four 1 uF, two 0.1 uF and two 0.01 uF capacitors under the SN75DP139 and close to the VCC pins, all connecter in parallel between VCC and GND.

10 Layout

10.1 Layout Guidelines

10.1.1 Layer Stack

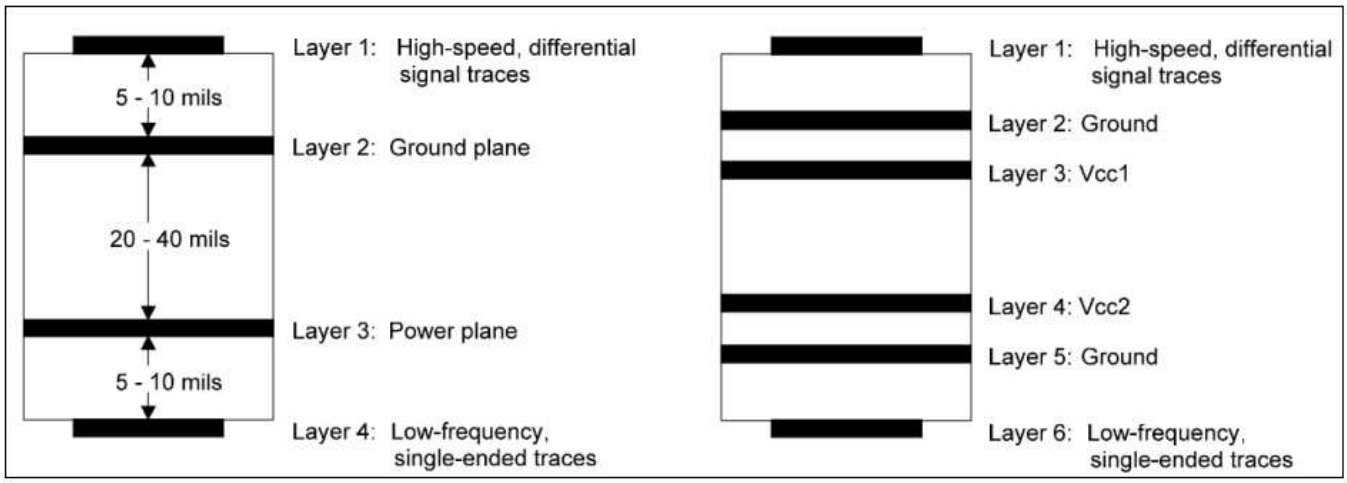


Figure 34. Recommended 4- or 6- Layer (0.062") Stack for a Receiver PCB Design

Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit.

Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.

Routing the fast-edged control signals on the bottom layer by prevents them from cross-talking into the high-speed signal traces and minimizes EMI.

If the receiver requires a supply voltage different from the one of the repeater, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. Finally, a second power/ground system provides added isolation between the signal layers.

10.1.2 Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and lower EMI. Although there seems to be an endless number of precautions to be taken, this section provides only a few main recommendations as layout guidance.

1. Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.
2. Reduce inter-pair skew, caused by component placement and IC pinouts, by making larger meandering correction along the signal path. Use chamfered corners with a length-to-trace width ratio of between 3 and 5. The distance between bends should be 8 to 10 times the trace width.
3. Use 45 degree bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase

Layout Guidelines (continued)

the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45o bends is seen as a smaller discontinuity.

4. When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.
5. Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area.
6. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
7. Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.
8. Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 100 Ω differential impedance. Large vias and pads can cause the impedance to drop below 85 Ω.
9. Use solid power and ground planes for 100 Ω impedance control and minimum power noise.
10. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
11. Keep the trace length between the DisplayPort connector and the DisplayPort device as short as possible to minimize attenuation.
12. Use good DisplayPort connectors whose impedances meet the specifications.
13. Place bulk capacitors (for example, 10 µF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
14. Place smaller 0.1 µF or 0.01 µF capacitors at the device.

10.2 Layout Example

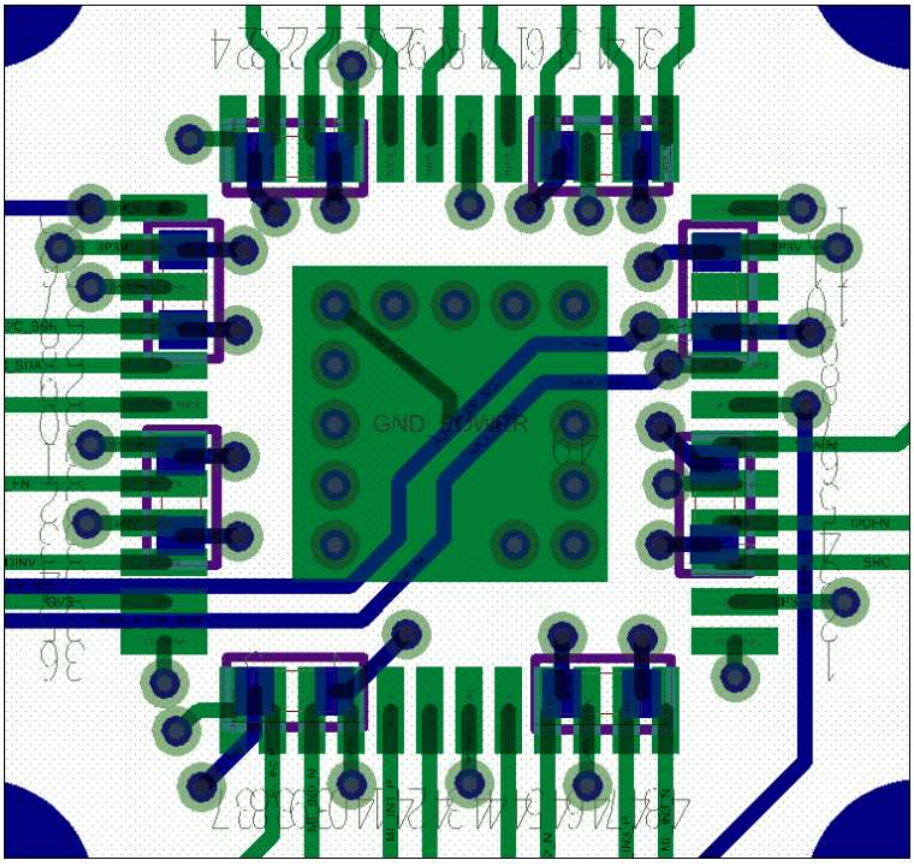


Figure 35. Footprint Example

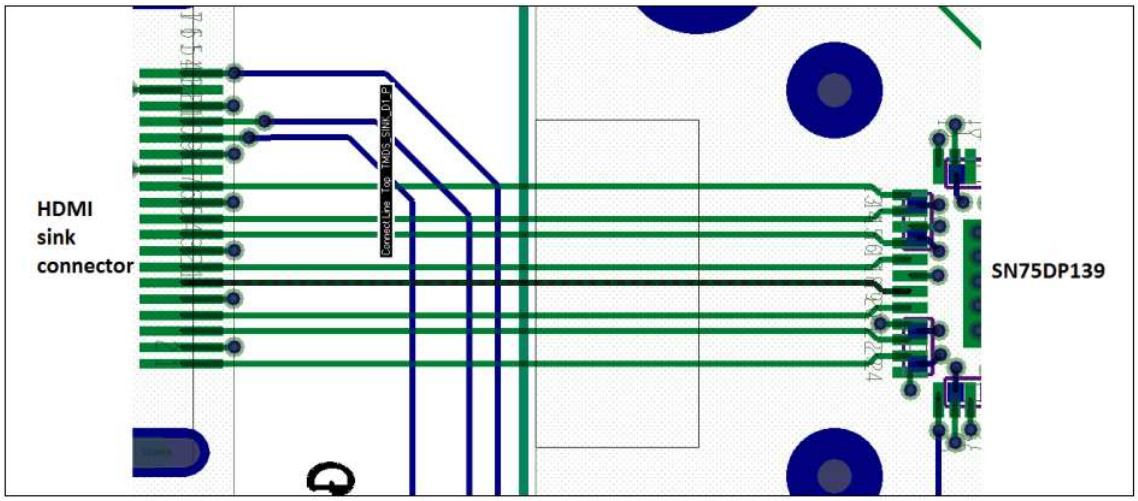


Figure 36. Sink Side Layout Example

Layout Example (continued)

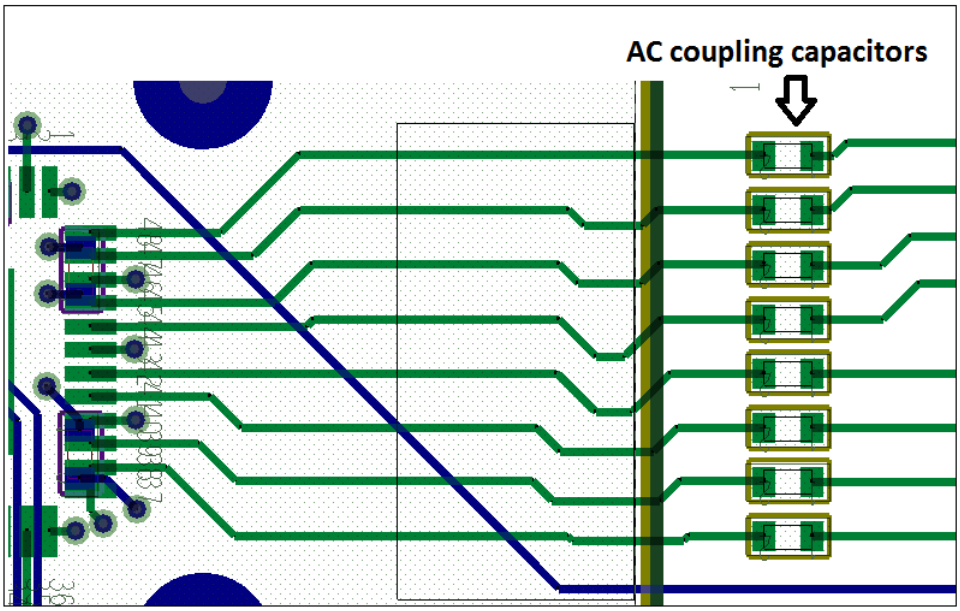


Figure 37. AC Capacitors Placement and Routing Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75DP139RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	DP139	Samples
SN75DP139RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	DP139	Samples
SN75DP139RSBR	ACTIVE	WQFN	RSB	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	DP139	Samples
SN75DP139RSBT	ACTIVE	WQFN	RSB	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	DP139	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

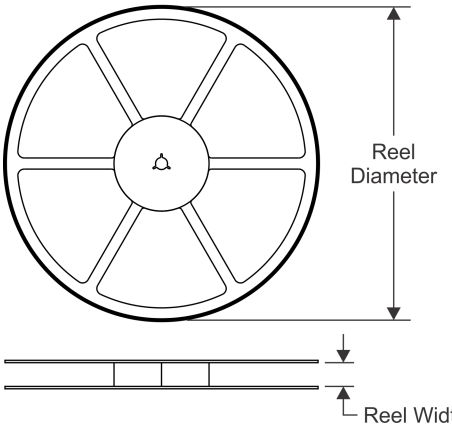
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

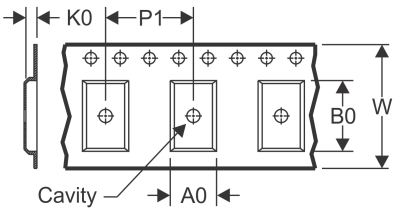
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

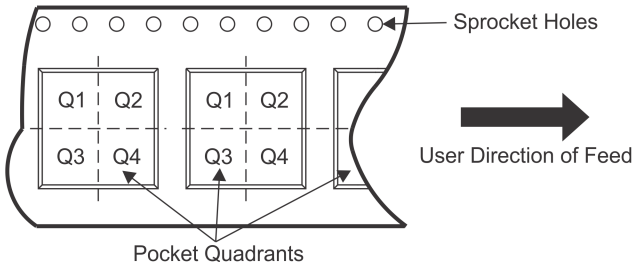


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

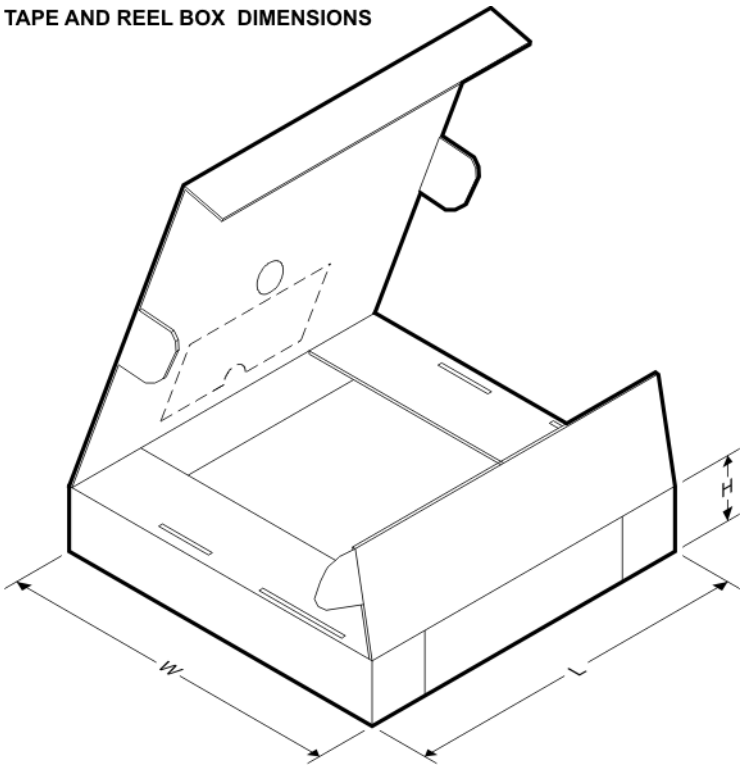
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP139RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
SN75DP139RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN75DP139RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN75DP139RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
SN75DP139RSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
SN75DP139RSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

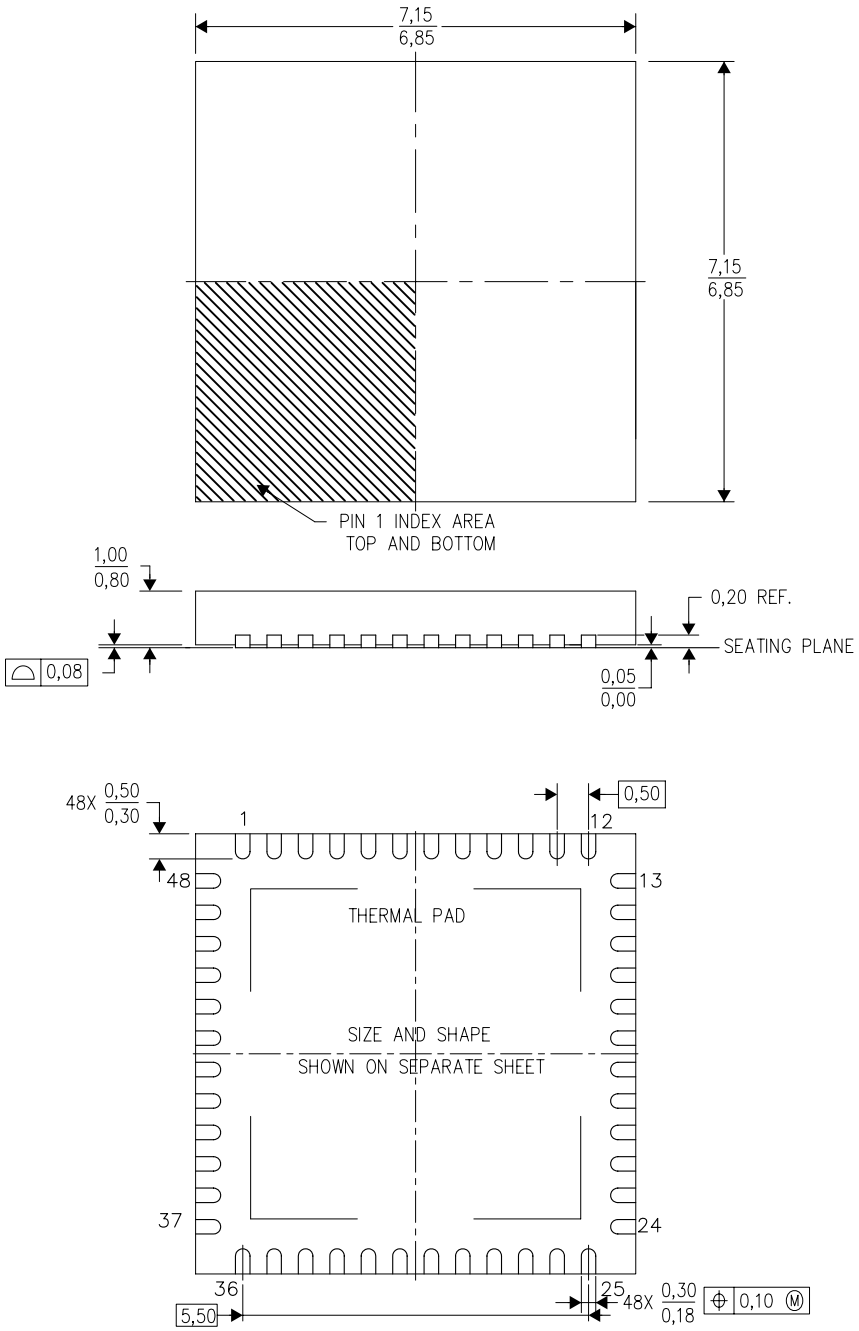
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP139RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN75DP139RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN75DP139RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
SN75DP139RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
SN75DP139RSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
SN75DP139RSBT	WQFN	RSB	40	250	210.0	185.0	35.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

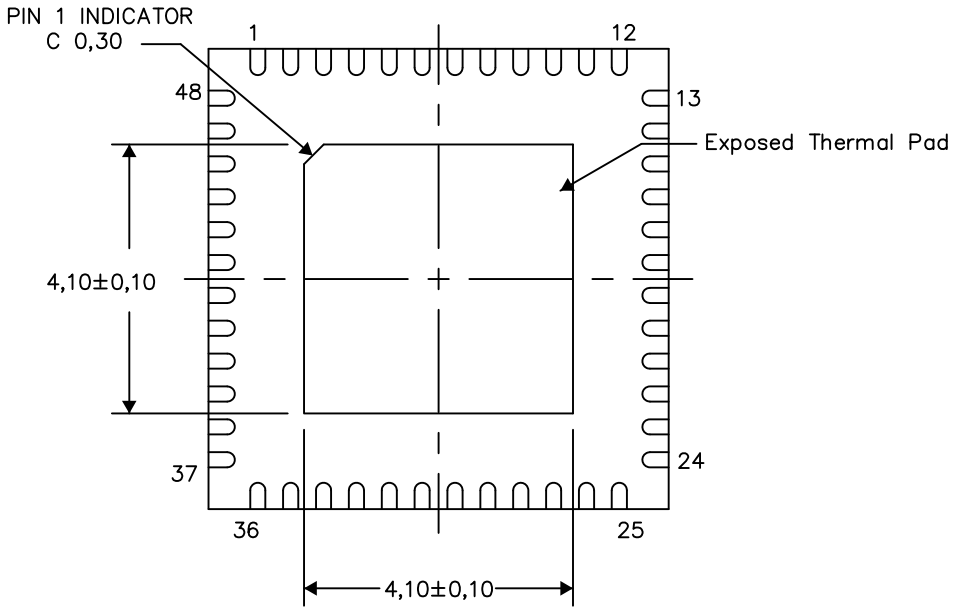
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



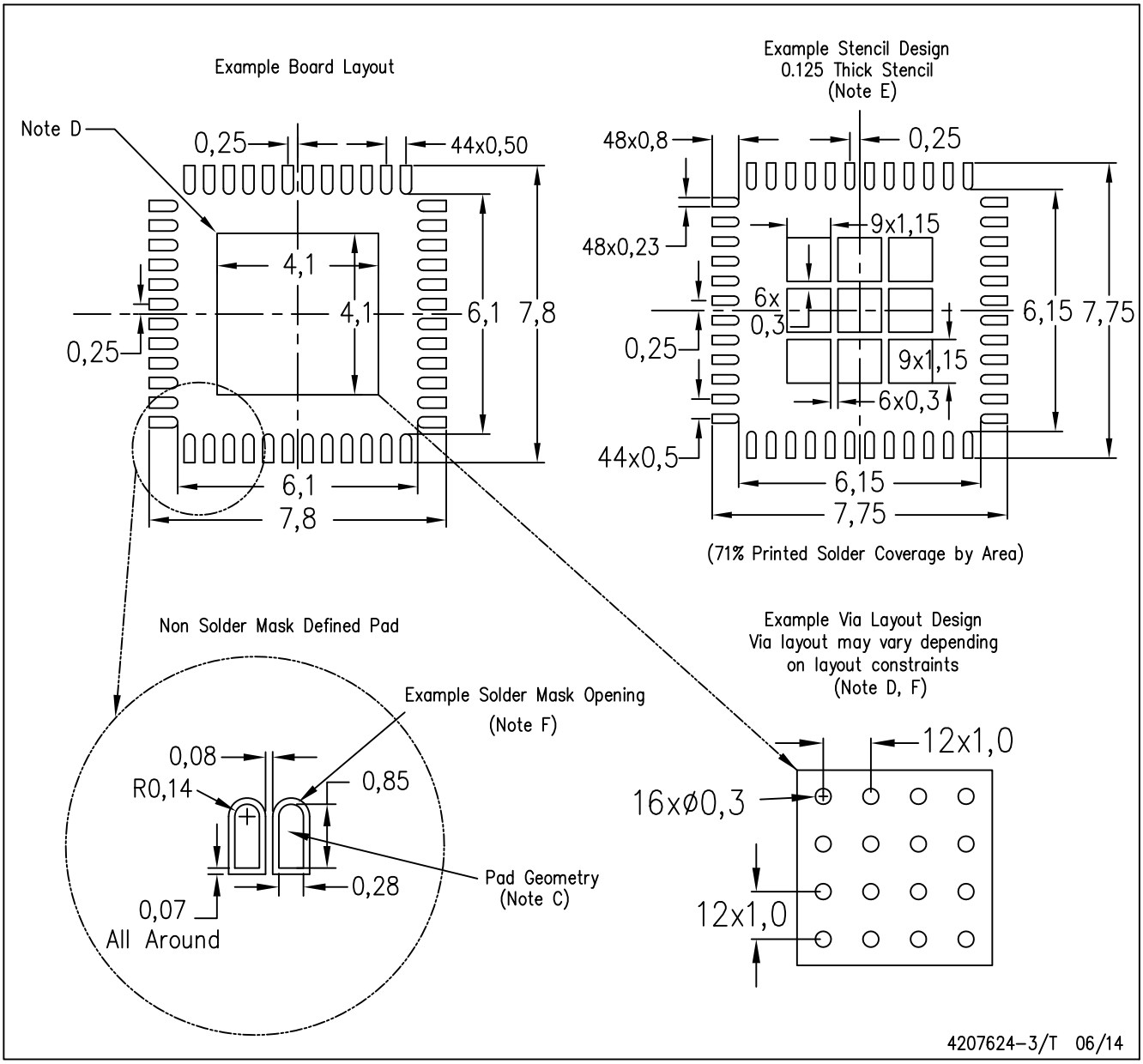
Bottom View

Exposed Thermal Pad Dimensions

4206354–3/Z 03/15

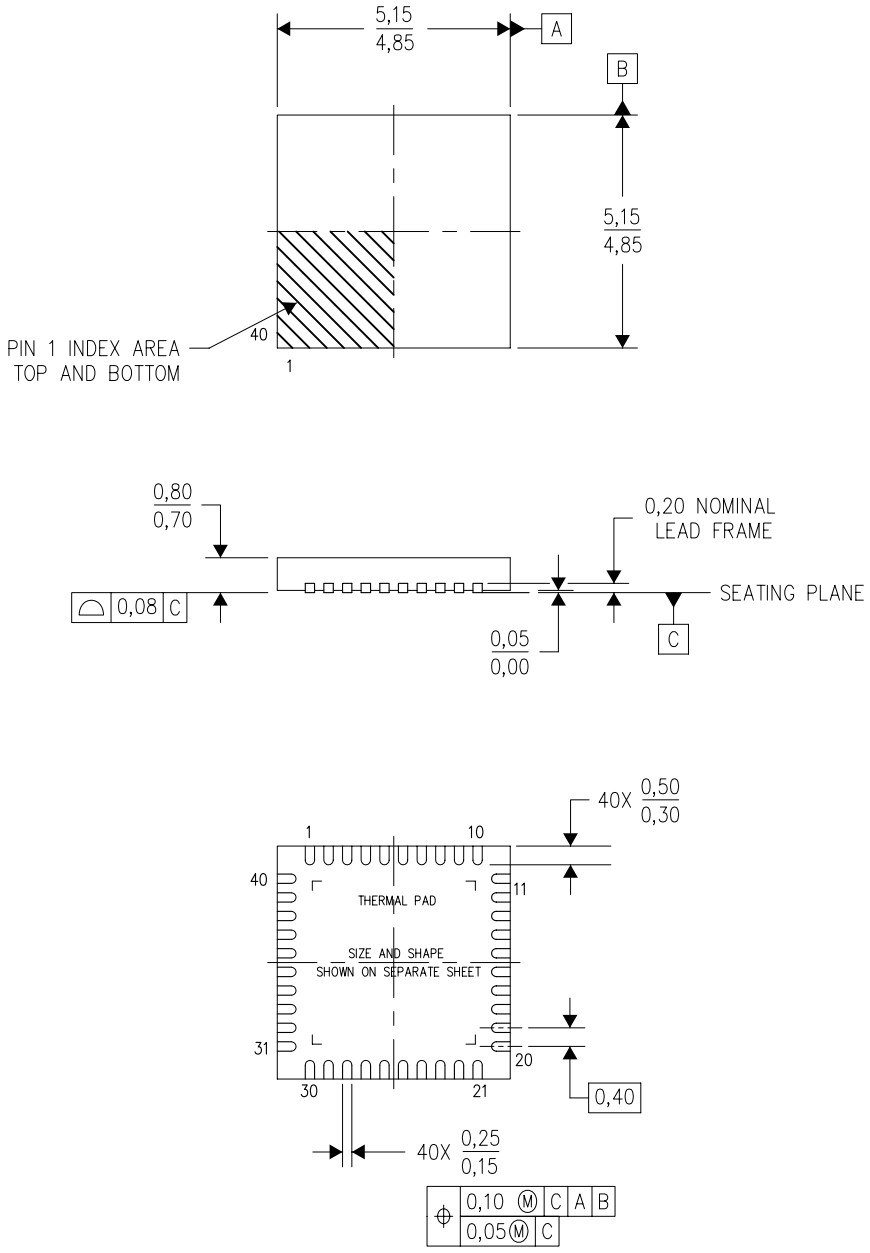
NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



4207182/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

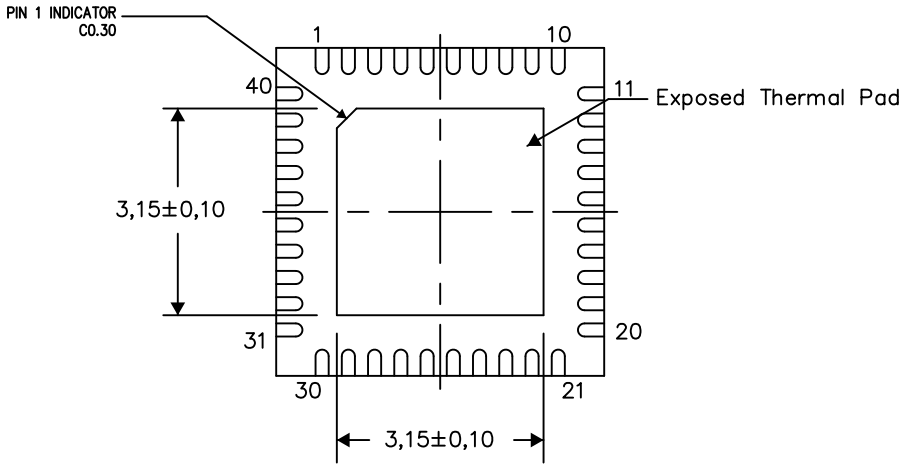
RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



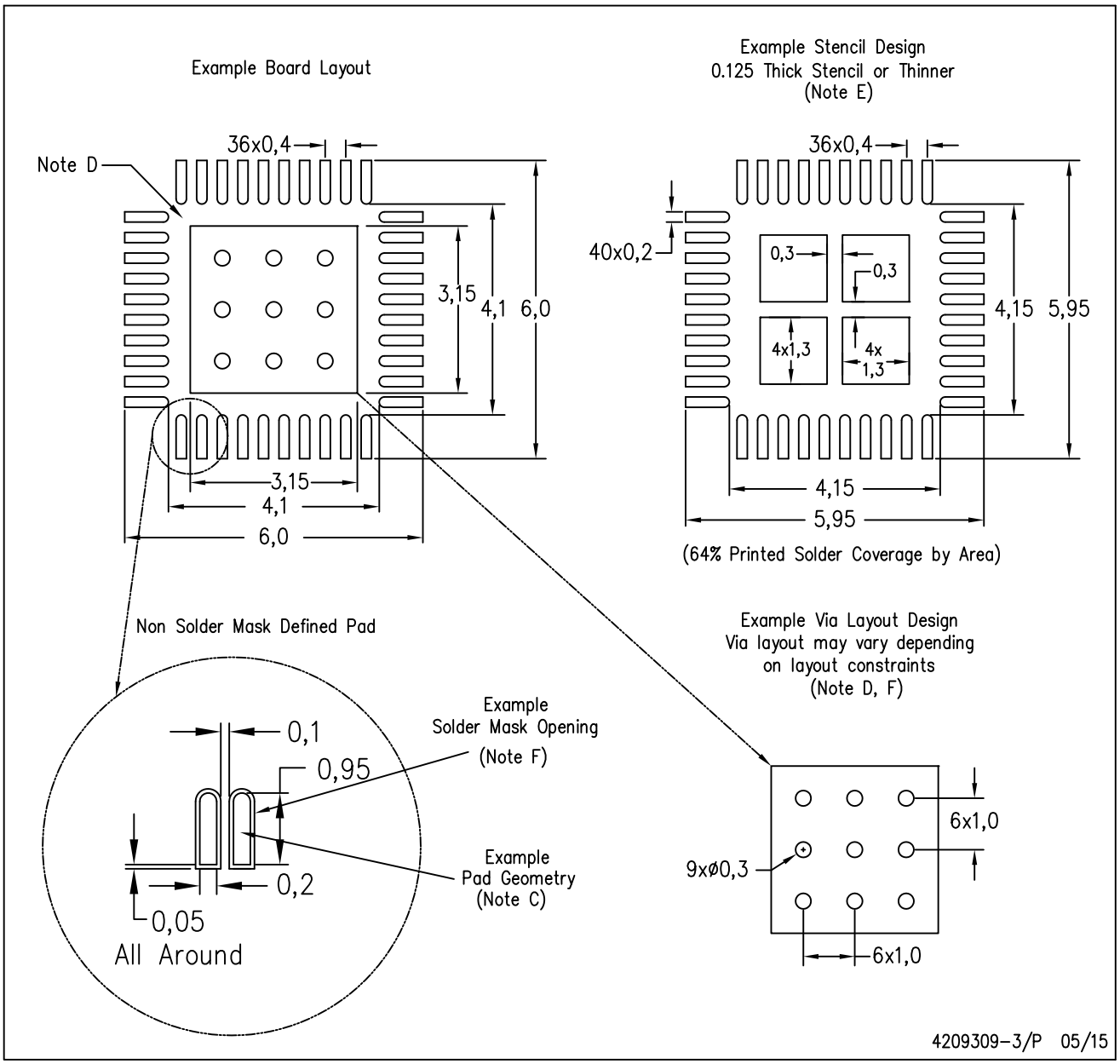
Bottom View

Exposed Thermal Pad Dimensions

4207183–3/R 05/15

NOTE: All linear dimensions are in millimeters

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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