ISO674x-Q1 Automotive, General-Purpose, Reinforced, Quad-Channel Digital Isolators With Robust EMC

1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design: ISO6740-Q1, ISO6741-Q1, ISO6742-Q1
- AEC-Q100 qualified with the following results:
  - Device temperature Grade 1: –40°C to 125°C ambient operating temperature range
- Meets VDA320 isolation requirements
- 50Mbps data rate
- Robust isolation barrier:
  - High lifetime at 1500V_{RMS} working voltage
  - Up to 5000V_{RMS} isolation rating
  - Up to 10kV surge capability
  - ±150kV/µs typical CMTI
- Wide supply range: 1.71V to 1.89V and 2.25V to 5.5V
- 1.71V to 5.5V level translation
- Default output *high* (ISO674x-Q1) and *low* (ISO674xF-Q1) options
- 1.6mA per channel typical at 1Mbps
- Low propagation delay: 11ns typical
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - ±8kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Wide-SOIC (DW-16) Package
- Safety-Related Certifications :
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1
  - GB 4943.1

2 Applications

- Hybrid, electric and power train system (EV/HEV)
  - Battery management system (BMS)
  - On-board charger
  - DC/DC converter
  - Inverter and motor control

3 Description

The ISO674x-Q1 devices are high-performance, quad-channel digital isolators designed for cost-sensitive applications requiring up to 5000V_{RMS} isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO674x-Q1 devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO_2) insulation barrier. These devices come with enable pins which can be used to put the respective outputs in high impedance for multi-controller driving applications. The ISO6740-Q1 device has all four channels in the same direction, the ISO6741-Q1 device has three forward and one reverse-direction channels, and the ISO6742-Q1 device has two forward and two reverse-direction channels. In the event of input power or signal loss, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See also Device Functional Modes section.

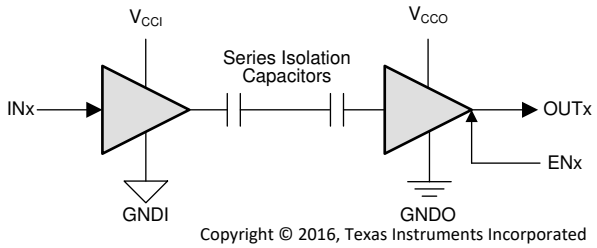
Used in conjunction with isolated power supplies, the ISO674x-Q1 devices help prevent noise currents on data buses, such as CAN and LIN from damaging sensitive circuitry. Through remarkable chip design and layout techniques, the electromagnetic compatibility of the ISO674x-Q1 devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO674x-Q1 family of devices is available in a 16-pin SOIC wide-body (DW) package and is a pin-to-pin upgrade to the older generations.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)	PACKAGE SIZE(2)
ISO6740-Q1, ISO6740F-Q1 ISO6741-Q1, ISO6741F-Q1 ISO6742-Q1, ISO6742F-Q1	DW (SOIC, 16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO6742-Q1, ISO6742F-Q1	DWW (Extra wide SOIC, 16)(3)	10.30mm × 14.0mm	10.30mm × 17.25mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product preview.



V_{CCI}=Input supply, V_{CCO}=Output supply
GNDI=Input ground, GNDO=Output ground

Simplified Schematic

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4 Pin Configuration and Functions

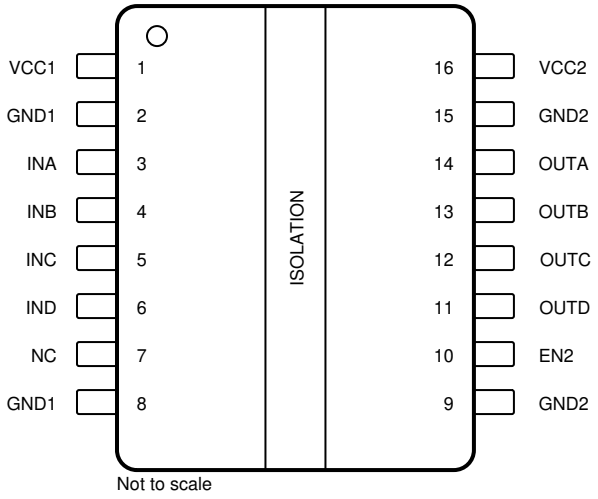

Figure 4-1. ISO6740-Q1 DW Package 16-Pin SOIC-WB Top View

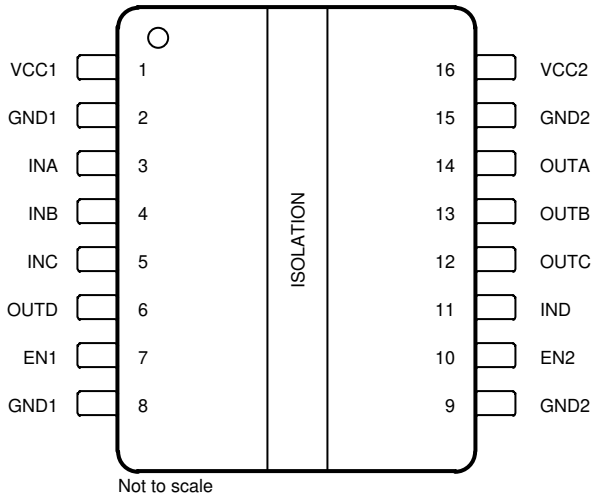

Figure 4-2. ISO6741-Q1 DW Package 16-Pin SOIC-WB Top View

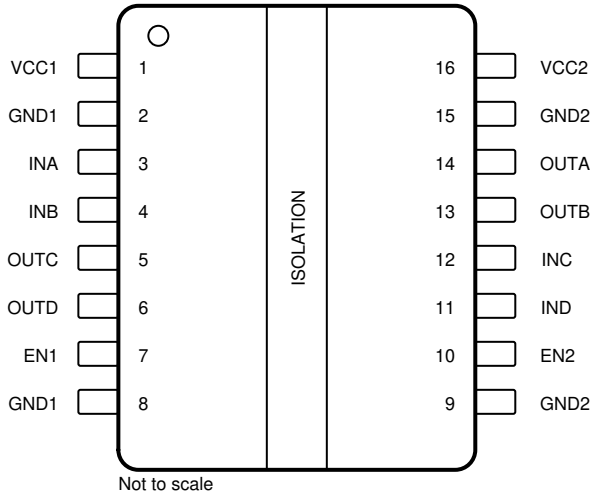

Figure 4-3. ISO6742-Q1 DWW Package 16-Pin SOIC-Extra-WB, SOIC-WB Top View

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Table 4-1. Pin Functions

PIN				Type[1]	DESCRIPTION
NAME	ISO6740-Q1	ISO6741-Q1	ISO6742-Q1		
EN1	-	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	10	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	2,8	2,8	—	Ground connection for V_{CC1}
GND2	9, 15	9,15	9,15	—	Ground connection for V_{CC2}
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	5	5	12	I	Input, channel C
IND	6	11	11	I	Input, channel D
NC	7	-	-		Not connected
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	12	12	5	O	Output, channel C
OUTD	11	6	6	O	Output, channel D
V_{CC1}	1	1	1	—	Power supply, side 1
V_{CC2}	16	16	16	—	Power supply, side 2

(1) I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

See(1)

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC1} to GND1	-0.5	6	V
	V_{CC2} to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	V_{CCX} + 0.5 (3)	V
	OUTx to GNDx	-0.5	V_{CCX} + 0.5 (3)	
Output current	Io	-15	15	mA
Temperature	Operating junction temperature, T_J		150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4)	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1} (1)	Supply Voltage Side 1	V_{CC} = 1.8 V (3)	1.71		1.89	V
V_{CC1} (1)	Supply Voltage Side 1	V_{CC} = 2.5 V to 5 V (3)	2.25		5.5	V
V_{CC2} (1)	Supply Voltage Side 2	V_{CC} = 1.8 V (3)	1.71		1.89	V
V_{CC2} (1)	Supply Voltage Side 2	V_{CC} = 2.5 V to 5 V (3)	2.25		5.5	V
Vcc (UVLO+)	UVLO threshold when supply voltage is rising			1.53	1.71	V
Vcc (UVLO-)	UVLO threshold when supply voltage is falling		1.1	1.41		V
Vhys (UVLO)	Supply voltage UVLO hysteresis		0.08	0.13		V
V_{IH}	High level Input voltage		0.7 x V_{CCI} (2)		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	High level output current	V_{CCO} = 5 V (2)	-4			mA
		V_{CCO} = 3.3 V	-2			mA
		V_{CCO} = 2.5 V	-1			mA
		V_{CCO} = 1.8 V	-1			mA
I_{OL}	Low level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	mA
		V_{CCO} = 2.5 V			1	mA
		V_{CCO} = 1.8 V			1	mA
DR	Data Rate		0		50	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(3) The channel outputs are in undetermined state when 1.89 V < V_{CC1}, V_{CC2} < 2.25 V and 1.05 V < V_{CC1}, V_{CC2} < 1.71 V

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5.4 Thermal Information

THERMAL METRIC(1)		ISO674x-Q1 DW (SOIC) 16 PINS	ISO6742-Q1 DWW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	56.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.1	22	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.4	31	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.9	30.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO6740						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 25-MHz 50% duty cycle square wave			130.9	mW
P_{D1}	Maximum power dissipation (side-1)				33	mW
P_{D2}	Maximum power dissipation (side-2)				97.9	mW
ISO6741						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 25-MHz 50% duty cycle square wave			134.9	mW
P_{D1}	Maximum power dissipation (side-1)				50.8	mW
P_{D2}	Maximum power dissipation (side-2)				84.1	mW
ISO6742						
P_D	Maximum power dissipation (both sides)	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 25-MHz 50% duty cycle square wave			137.5	mW
P_{D1}	Maximum power dissipation (side-1)				68.75	mW
P_{D2}	Maximum power dissipation (side-2)				68.75	mW

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	DWW-16	
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	>14.5	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	>14.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	2121	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test; See Figure 8-8	1500	1500	V_{RMS}
		DC voltage	2121	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7071	8000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-us waveform per IEC 62368-1	7692	10000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	13000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, After Input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b: At routine test (100% production) and preconditioning (type test); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	≤5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	≅1	≅1	pF
R_{IO}	Isolation resistance(6)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
	Climatic category		40/125/21	40/125/21	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).

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(6) All pins on each side of the barrier tied together creating a two-terminal device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 2121 V_{PK}; Maximum surge isolation voltage, 10000 V_{PK}	5000 V_{RMS} insulation per CSA 62368-1, IEC 62368-1, CSA 61010-1 and IEC 61010-1, 1000 V_{RMS} basic and 600 V_{RMS} reinforced working voltage (pollution degree 2, material group I); 5000 V_{RMS} insulation per CSA 60601-1 and IEC 60601-1, 2 MOPP for 250 V_{RMS}	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage	5000 V_{RMS} reinforced insulation per EN 61010-1 and EN 62368-1 up to working voltage of 600 V_{RMS} and EN 60950- 1 up to working voltage of 800 V_{RMS}
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC21001304083	Client ID number: 077311

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5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =73°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			311.4	mA
		$R_{\theta JA}$ = 73°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			475.7	mA
		$R_{\theta JA}$ = 73°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			622	
		$R_{\theta JA}$ = 73°C/W, V_I = 1.89 V, T_J = 150°C, T_A = 25°C			905.1	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 73°C/W, T_J = 150°C, T_A = 25°C			1712.4	mW
T_S	Maximum safety temperature				150	°C
DWW-16 PACKAGE						
I_S	Safety input, output, or supply current	$R_{\theta JA}$ =56.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			402.2	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 56.5°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			614.5	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 56.5°C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C			804.5	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 56.5°C/W, V_I = 1.89 V, T_J = 150°C, T_A = 25°C			1170.5	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 56.5°C/W, T_J = 150°C, T_A = 25°C			2212.3	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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5.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4 mA; See Figure 6-1	V_{CCO} - 0.4 (1)			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 6-1			0.4	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at ENx			28	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at ENx	-28			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See Figure 6-4	100	150		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 5 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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5.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6740							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(ISO6740); V_I = 0 V (ISO6740 with F suffix)		I_{CC1}		1.6	2.2	mA
			I_{CC2}		2.1	3.4	
	V_I = 0 V (ISO6740); V_I = V_{CC1} (ISO6740 with F suffix)		I_{CC1}		5.8	8	
			I_{CC2}		2.3	3.7	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.7	5.1	
			I_{CC2}		2.4	3.8	
		10 Mbps	I_{CC1}		3.8	5.3	
			I_{CC2}		4.8	6.4	
		50 Mbps	I_{CC1}		4.4	6	
			I_{CC2}		15	17.8	
ISO6741							
Supply current - DC signal (2)	V_I = V_{CCI} (1)(ISO6741); V_I = 0 V (ISO6741 with F suffix)		I_{CC1}		1.9	2.8	mA
			I_{CC2}		2.2	3.5	
	V_I = 0 V (ISO6741); V_I = V_{CCI} (ISO6741 with F suffix)		I_{CC1}		5.1	7.2	
			I_{CC2}		3.4	5.1	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.6	5.1	
			I_{CC2}		3	4.5	
		10 Mbps	I_{CC1}		4.2	5.8	
			I_{CC2}		4.8	6.5	
		50 Mbps	I_{CC1}		7.3	9.3	
			I_{CC2}		12.6	15.3	
ISO6742							
Supply current - DC signal (2)	V_I = V_{CCI} (1)(ISO6742); V_I = 0 V (ISO6742 with F suffix)		I_{CC1} , I_{CC2}		2.2	3.3	mA
	V_I = 0 V (ISO6742); V_I = V_{CCI} (ISO6742 with F suffix)		I_{CC1} , I_{CC2}		4.4	6.3	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		3.4	5	
		10 Mbps	I_{CC1}, I_{CC2}		4.7	6.4	
		50 Mbps	I_{CC1}, I_{CC2}		10.2	12.5	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = 0V
(3) Supply current valid for ENx = V_{CCx}

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5.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -2 mA; See Figure 6-1	V_{CCO} - 0.2 (1)			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; See Figure 6-1			0.2	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at ENx			30	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at ENx	-30			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See Figure 6-4	100	150		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 3.3 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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5.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6740							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(ISO6740); V_I = 0 V (ISO6740 with F suffix)		I_{CC1}		1.6	2.2	mA
			I_{CC2}		2.1	3.3	
	V_I = 0 V (ISO6740); V_I = V_{CC1} (ISO6740 with F suffix)		I_{CC1}		5.7	8	
			I_{CC2}		2.3	3.6	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.7	5.1	
			I_{CC2}		2.4	3.7	
		10 Mbps	I_{CC1}		3.8	5.2	
			I_{CC2}		4	5.6	
		50 Mbps	I_{CC1}		4.2	5.7	
			I_{CC2}		11.2	13.8	
ISO6741							
Supply current - DC signal (2)	V_I = V_{CCI} (1)(ISO6741); V_I = 0 V (ISO6741 with F suffix)		I_{CC1}		1.9	2.7	mA
			I_{CC2}		2.2	3.4	
	V_I = 0 V (ISO6741); V_I = V_{CCI} (ISO6741 with F suffix)		I_{CC1}		5	7.1	
			I_{CC2}		3.4	5.1	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.5	5	
			I_{CC2}		2.9	4.4	
		10 Mbps	I_{CC1}		4	5.5	
			I_{CC2}		4.2	5.8	
		50 Mbps	I_{CC1}		6.1	8	
			I_{CC2}		9.7	12.1	
ISO6742							
Supply current - DC signal (2)	V_I = V_{CCI} (1)(ISO6742); V_I = 0 V (ISO6742 with F suffix)		I_{CC1} , I_{CC2}		2.2	3.3	mA
	V_I = 0 V (ISO6742); V_I = V_{CCI} (ISO6742 with F suffix)		I_{CC1} , I_{CC2}		4.4	6.3	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		3.4	4.9	
		10 Mbps	I_{CC1}, I_{CC2}		4.2	5.9	
		50 Mbps	I_{CC1}, I_{CC2}		8.2	10.3	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = 0V
(3) Supply current valid for ENx = V_{CCx}

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5.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1 mA; See Figure 6-1	V_{CCO} - 0.1 (1)			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; See Figure 6-1			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at ENx			30	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at ENx	-30			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See Figure 6-4	100	150		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 2.5 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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5.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6740							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(ISO6740); V_I = 0 V (ISO6740 with F suffix)		I_{CC1}		1.6	2.2	mA
			I_{CC2}		2.1	3.3	
	V_I = 0 V (ISO6740); V_I = V_{CC1} (ISO6740 with F suffix)		I_{CC1}		5.7	7.9	
			I_{CC2}		2.3	3.6	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.7	5.1	
			I_{CC2}		2.3	3.6	
		10 Mbps	I_{CC1}		3.7	5.1	
			I_{CC2}		3.5	5.1	
		50 Mbps	I_{CC1}		4.1	5.6	
			I_{CC2}		9	11.2	
ISO6741							
Supply current - DC signal (2)	V_I = V_{CCI} (1)(ISO6741); V_I = 0 V (ISO6741 with F suffix)		I_{CC1}		1.9	2.7	mA
			I_{CC2}		2.2	3.4	
	V_I = 0 V (ISO6741); V_I = V_{CCI} (ISO6741 with F suffix)		I_{CC1}		5	7.1	
			I_{CC2}		3.4	5.1	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.5	5	
			I_{CC2}		2.9	4.4	
		10 Mbps	I_{CC1}		3.9	5.4	
			I_{CC2}		3.8	5.4	
		50 Mbps	I_{CC1}		5.5	7.2	
			I_{CC2}		8.1	10.2	
ISO6742							
Supply current - DC signal (2)	V_I = V_{CCI} (1)(ISO6742); V_I = 0 V (ISO6742 with F suffix)		I_{CC1} , I_{CC2}		2.2	3.3	mA
	V_I = 0 V (ISO6742); V_I = V_{CCI} (ISO6742 with F suffix)		I_{CC1} , I_{CC2}		4.3	6.3	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		3.3	4.8	
		10 Mbps	I_{CC1}, I_{CC2}		4	5.6	
		50 Mbps	I_{CC1}, I_{CC2}		7	9	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = 0V
(3) Supply current valid for ENx = V_{CCx}

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5.15 Electrical Characteristics—1.8-V Supply

V_{CC1} = V_{CC2} = 1.8 V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -1 mA; See Figure 6-1	V_{CCO} - 0.1 (1)			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; See Figure 6-1			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold				0.7 x V_{CCI} (1)	V
$V_{IT-(IN)}$	Falling input switching threshold		0.3 x V_{CCI}			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 x V_{CCI}			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	-10			µA
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at ENx			30	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at ENx	-30			µA
CMTI	Common mode transient immunity	V_I = V_{CC} or 0 V, V_{CM} = 1200 V; See Figure 6-4	100	150		kV/µs
C_i	Input Capacitance (2)	V_I = V_{CC}/ 2 + 0.4×sin(2πft), f = 2 MHz, V_{CC} = 1.8 V		2.8		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}
(2) Measured from input pin to same side ground.

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5.16 Supply Current Characteristics—1.8-V Supply

V_{CC1} = V_{CC2} = 1.8 V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO6740							
Supply current - DC signal (2)	V_I = V_{CC1} (1)(ISO6740); V_I = 0 V (ISO6740 with F suffix)		I_{CC1}		1.2	1.8	mA
			I_{CC2}		2	3.4	
	V_I = 0 V (ISO6740); V_I = V_{CC1} (ISO6740 with F suffix)		I_{CC1}		5.1	7.6	
			I_{CC2}		2.2	3.7	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.1	4.7	
			I_{CC2}		2.2	3.7	
		10 Mbps	I_{CC1}		3.2	4.8	
			I_{CC2}		3.1	4.6	
		50 Mbps	I_{CC1}		3.4	5.1	
			I_{CC2}		7	8.9	
ISO6741							
Supply current - DC signal (2)	V_I = V_{CCI} (1)(ISO6741); V_I = 0 V (ISO6741 with F suffix)		I_{CC1}		1.5	2.4	mA
			I_{CC2}		2	3.4	
	V_I = 0 V (ISO6741); V_I = V_{CCI} (ISO6741 with F suffix)		I_{CC1}		4.5	6.9	
			I_{CC2}		3.2	5	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		3.1	4.7	
			I_{CC2}		2.7	4.3	
		10 Mbps	I_{CC1}		3.3	5	
			I_{CC2}		3.4	5	
		50 Mbps	I_{CC1}		4.5	6.3	
			I_{CC2}		6.4	8.3	
ISO6742							
Supply current - DC signal (2)	V_I = V_{CCI} (1)(ISO6742); V_I = 0 V (ISO6742 with F suffix)		I_{CC1} , I_{CC2}		1.9	3.1	mA
	V_I = 0 V (ISO6742); V_I = V_{CCI} (ISO6742 with F suffix)		I_{CC1} , I_{CC2}		4	6.1	
Supply current - AC signal (3)	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		3	4.7	
		10 Mbps	I_{CC1}, I_{CC2}		3.5	5.2	
		50 Mbps	I_{CC1}, I_{CC2}		5.6	7.6	

(1) V_{CCI} = Input-side V_{CC}
(2) Supply current valid for ENx = V_{CCx} and ENx = 0V
(3) Supply current valid for ENx = V_{CCx}

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5.17 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Figure 6-1		11	18	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				6	ns
t_r	Output signal rise time	See Figure 6-1		2.6	4.5	ns
t_f	Output signal fall time			2.6	4.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		18.6	25.8	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			18.6	25.8	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO674x			14.2	21.1	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO674x			14.2	21.1	ns
t_{PU}	Time from UVLO to valid output data				300	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2 V. See Figure 6-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.18 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Figure 6-1		11	18	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				7	ns
t_r	Output signal rise time	See Figure 6-1		1.6	3.2	ns
t_f	Output signal fall time			1.6	3.2	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		23.2	34.4	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			23.2	34.4	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO674x			16.6	23	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO674x			16.6	23	ns
t_{PU}	Time from UVLO to valid output data				300	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2 V. See Figure 6-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.19 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Figure 6-1		12	20.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	7.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				7	ns
t_r	Output signal rise time	See Figure 6-1		2	4	ns
t_f	Output signal fall time			2	4	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		28.1	43	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			28.1	43	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO674x			20.4	36.3	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO674x			20.4	36.3	ns
t_{PU}	Time from UVLO to valid output data				300	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2 V. See Figure 6-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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5.20 Switching Characteristics—1.8-V Supply

V_{CC1} = V_{CC2} = 1.8 V ±5% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	at 100kbps See Figure 6-1		15	24	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.7	8.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			6	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				8.8	ns
t_r	Output signal rise time	See Figure 6-1		2.7	5.3	ns
t_f	Output signal fall time			2.7	5.3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		40.3	63	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			40.3	63	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO674x			30	51.4	ns
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO674x			30	51.4	ns
t_{PU}	Time from UVLO to valid output data				300	µs
t_{DO}	Default output delay time from input power loss	Measured from the time VCC goes below 1.2 V. See Figure 6-3		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.21 Insulation Characteristics Curves

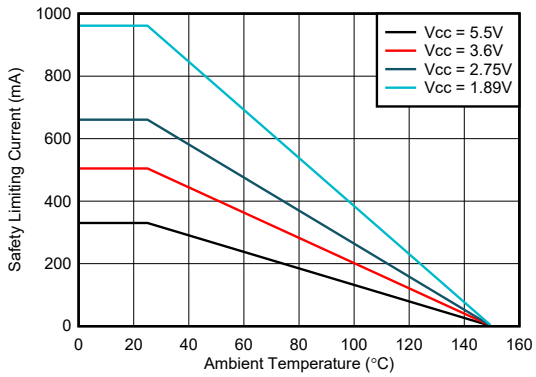

Figure 5-1. Thermal Derating Curve for Safety Limiting Current for DW-16 Package

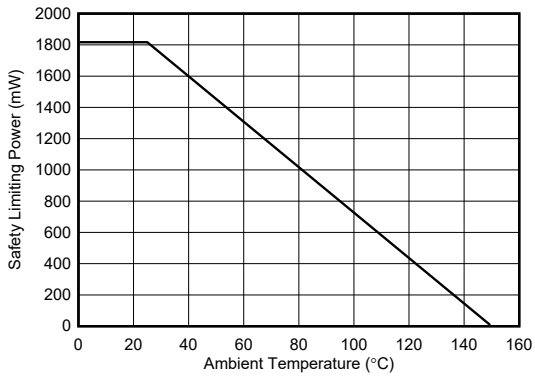

Figure 5-2. Thermal Derating Curve for Safety Limiting Power for DW-16 Package

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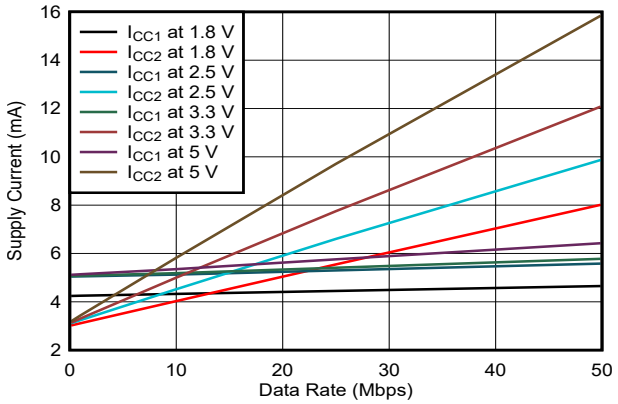
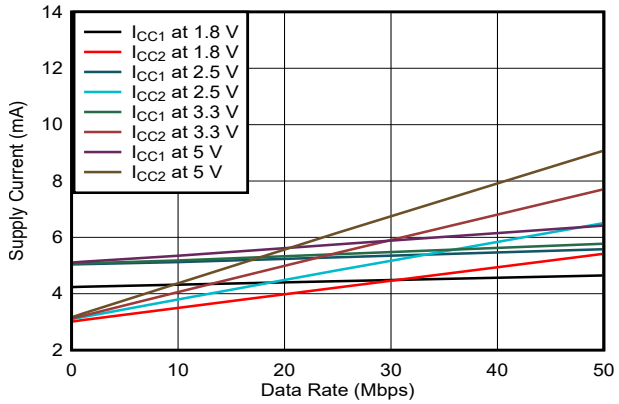
5.22 Typical Characteristics



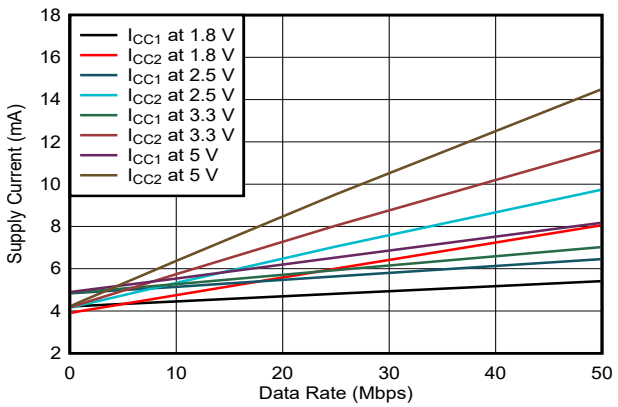
T_A = 25°C C_L = 15 pF

Figure 5-3. ISO6760-Q1 Supply Current vs Data Rate (With 15-pF Load)



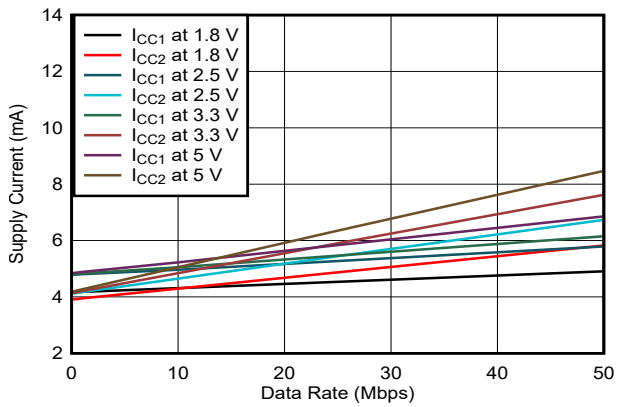
T_A = 25°C C_L = No Load

Figure 5-4. ISO6760-Q1 Supply Current vs Data Rate (With No Load)



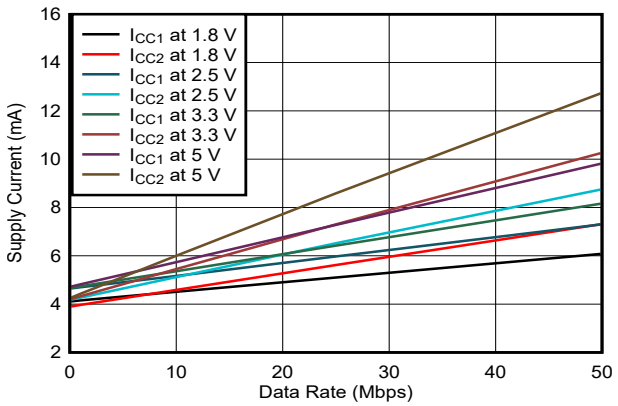
T_A = 25°C C_L = 15 pF

Figure 5-5. ISO6761-Q1 Supply Current vs Data Rate (With 15-pF Load)



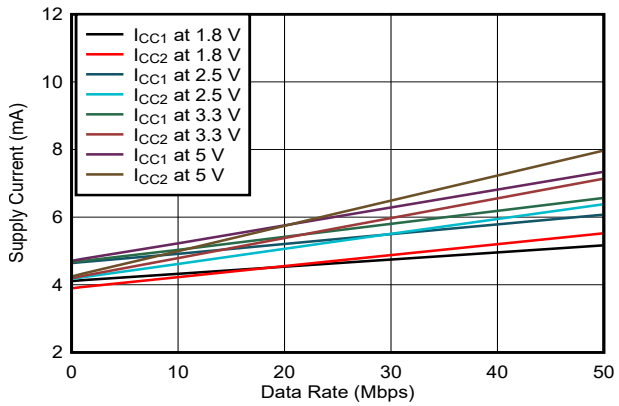
T_A = 25°C C_L = No Load

Figure 5-6. ISO6761-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C C_L = 15 pF

Figure 5-7. ISO6762-Q1 Supply Current vs Data Rate (With 15-pF Load)



T_A = 25°C C_L = No Load

Figure 5-8. ISO6762-Q1 Supply Current vs Data Rate (With No Load)

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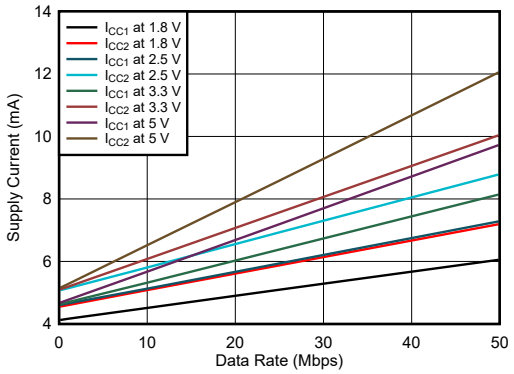
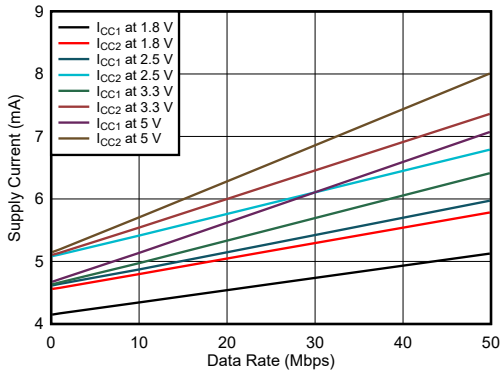


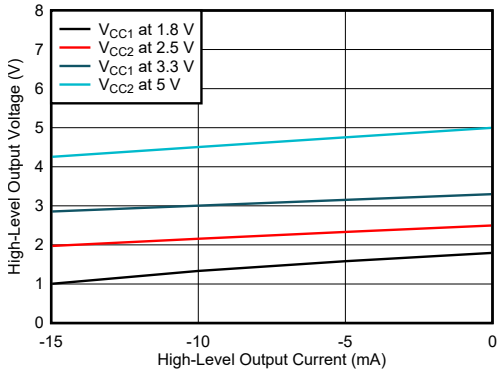
T_A = 25°C C_L = 15 pF

Figure 5-9. ISO6763-Q1 Supply Current vs Data Rate (With 15-pF Load)



T_A = 25°C C_L = No Load

Figure 5-10. ISO6763-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 5-11. High-Level Output Voltage vs High-level Output Current

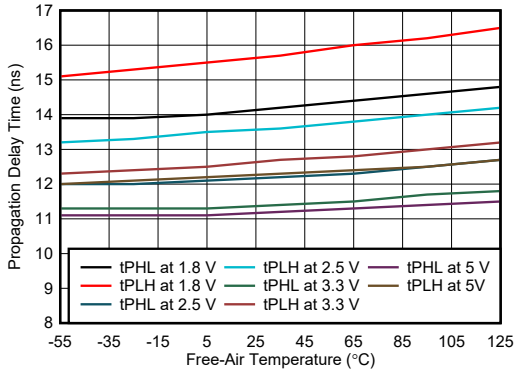


Figure 5-12. Propagation Delay Time vs Free-Air Temperature

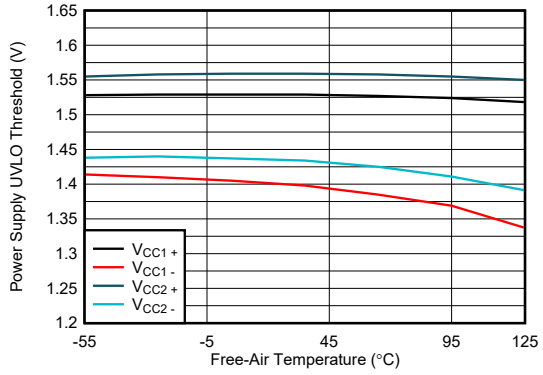
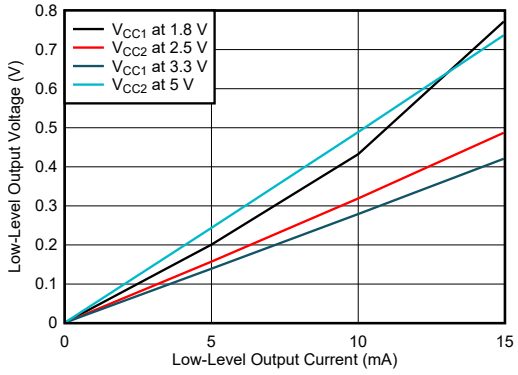


Figure 5-13. Power Supply Undervoltage Threshold vs Free-Air Temperature



T_A = 25°C

Figure 5-14. Low-Level Output Voltage vs Low-Level Output Current

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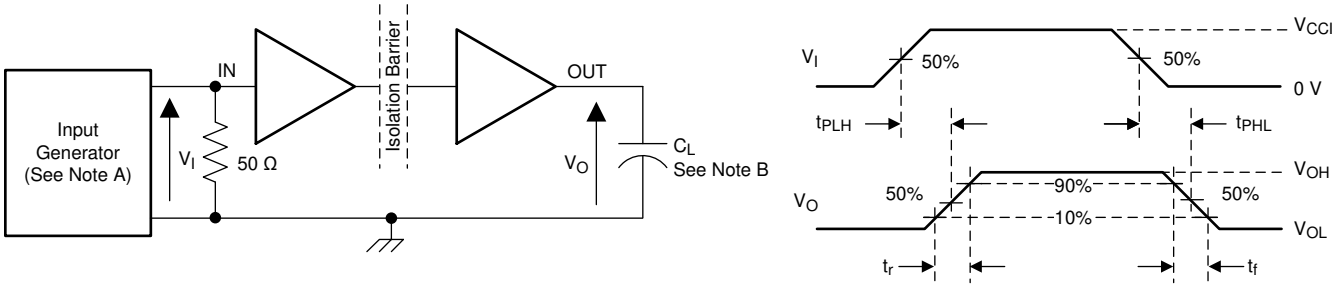
6 Parameter Measurement Information



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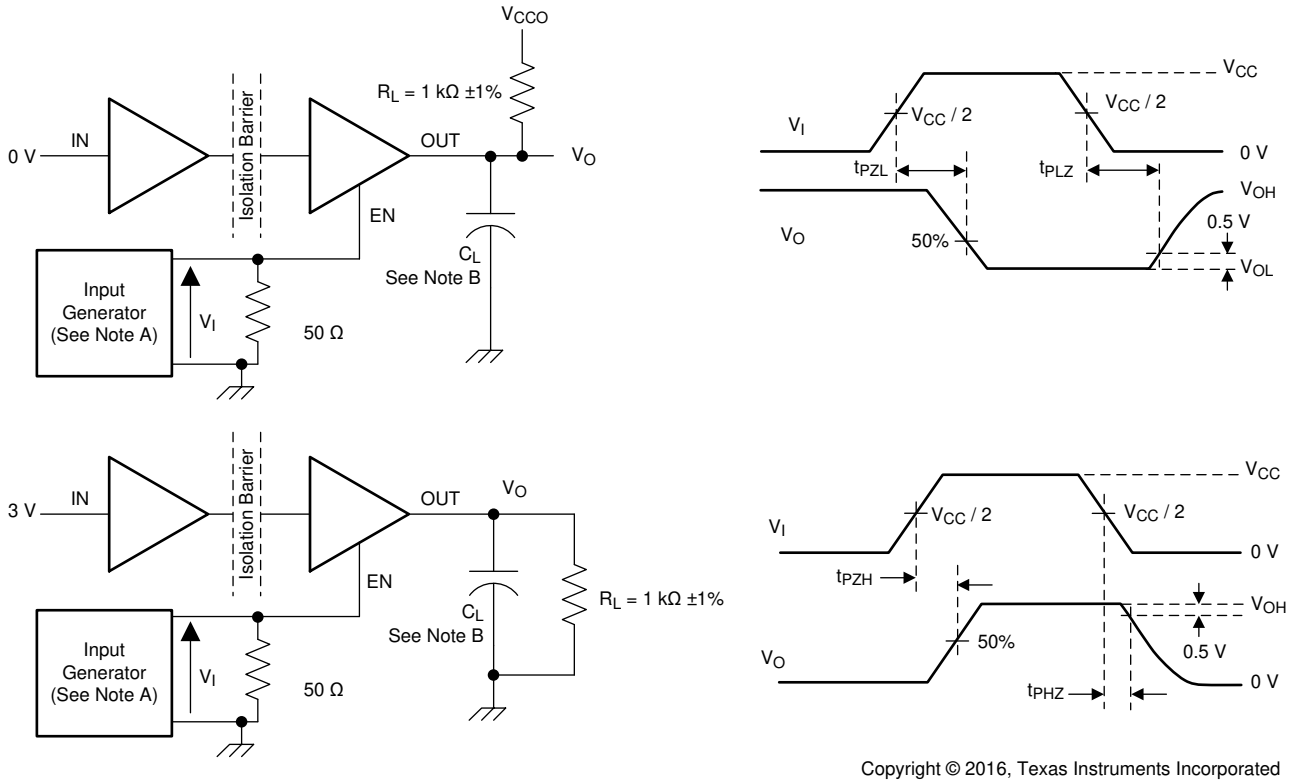
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. The 50 Ω is not needed in the actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



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A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

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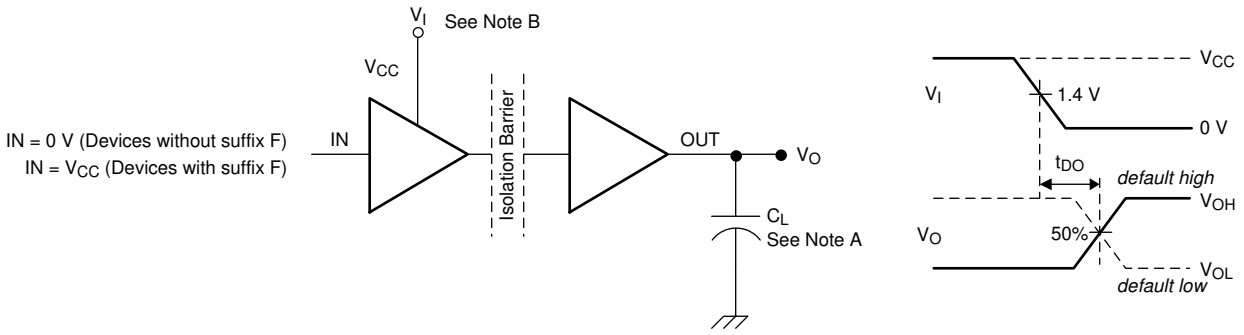
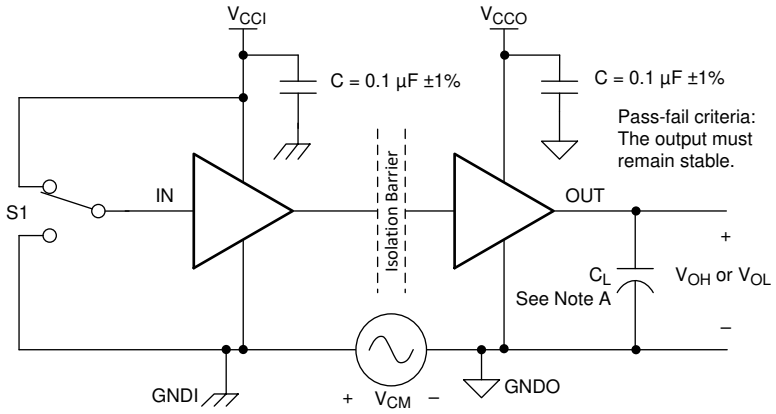


A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
B. Power Supply Ramp Rate = 10 mV/ns

Figure 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-4. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISO674x-Q1 family of devices have an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO674x-Q1 devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

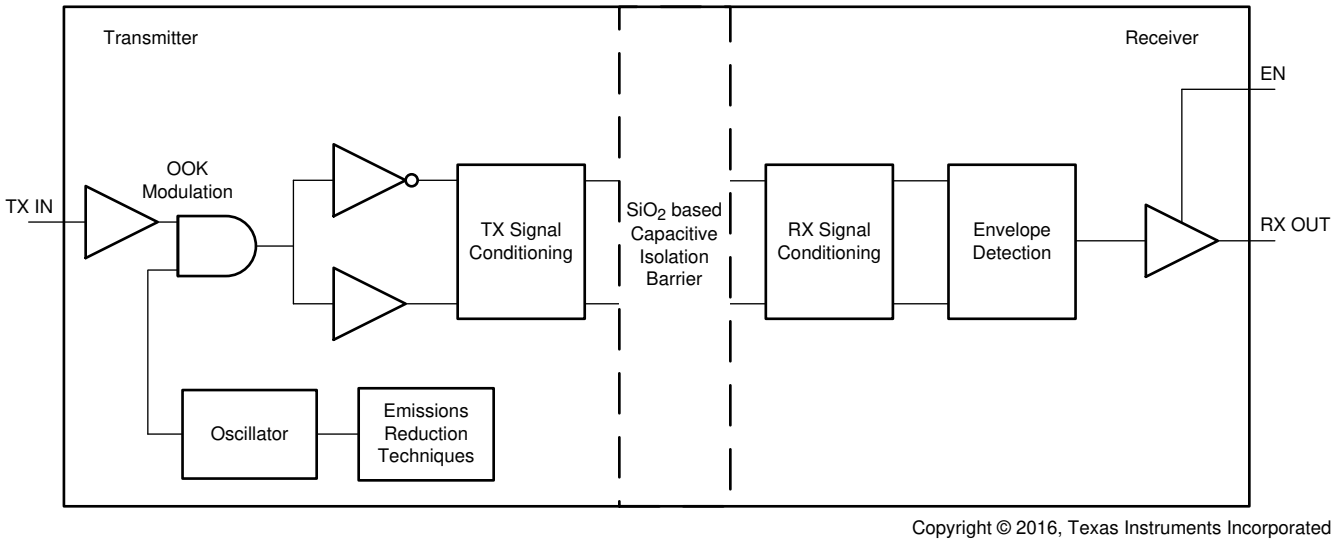


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Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

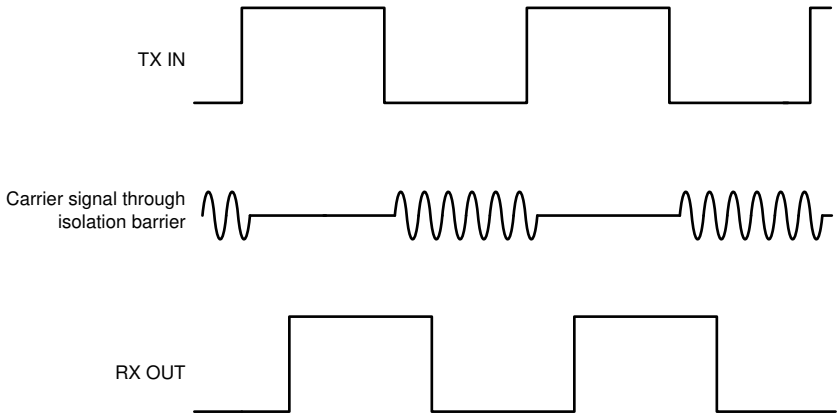

Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

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7.3 Feature Description

Table 7-1 provides an overview of the device features.

Table 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO6740-Q1	4 Forward, 0 Reverse	50 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
ISO6740F-Q1	4 Forward, 0 Reverse	50 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
ISO6741-Q1	3 Forward, 1 Reverse	50 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
ISO6741F-Q1	3 Forward, 1 Reverse	50 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
ISO6742-Q1	2 Forward, 2 Reverse	50 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
ISO6742F-Q1	2 Forward, 2 Reverse	50 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}

(1) See *Safety-Related Certifications* for detailed isolation ratings.

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 25. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO674x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

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7.4 Device Functional Modes

Table 7-2 lists the functional modes for the ISO674x-Q1 devices.

Table 7-2. Function Table

V_{CCI} (1)	V_{CCO}	INPUT (INx) (3)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO674x-Q1 and *Low* for ISO674x-Q1 with F suffix.
X	PU	X	L	Z	A low value of output enable causes the outputs to be high-impedance.
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO674x-Q1 and *Low* for ISO674x-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(2). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 1.71 V); PD = Powered down (V_{CC} ≤ 1.05 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) The outputs are in undetermined state when 1.89 V < V_{CCI}, V_{CCO} < 2.25 V and 1.05 V < V_{CCI}, V_{CCO} < 1.71 V
(3) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output

7.4.1 Device I/O Schematics

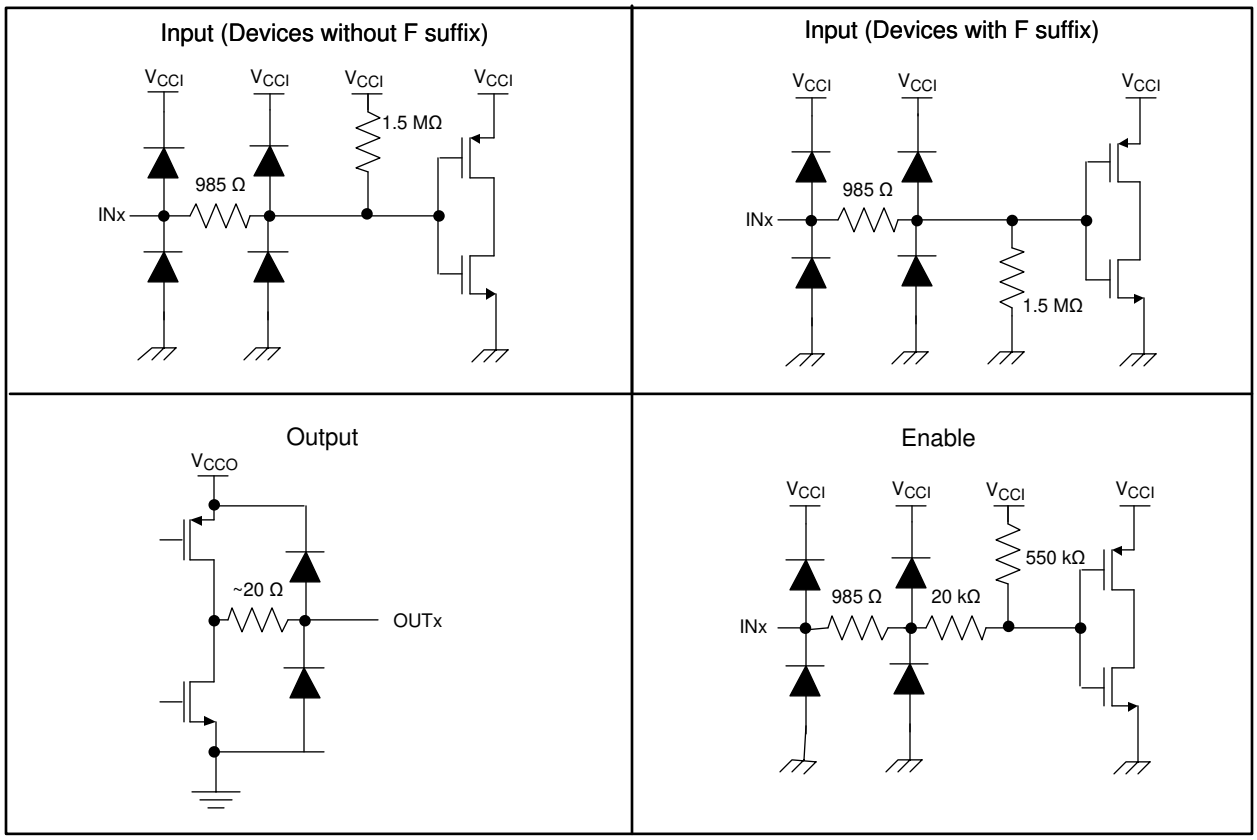

Figure 7-3. Device I/O Schematics

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO674x-Q1 devices are high-performance, quad-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi master driving applications. The ISO674x-Q1 devices use single-ended CMOS-logic switching technology. The supply voltage range is from 1.71 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, it is possible to supply ISO674x-Q1 V_{CC1} with 3.3 V (which is within 1.71 V to 5.5 V) and V_{CC2} with 5V (which is also within 1.71 V to 5.5 V). You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

Figure 8-1 shows the typical isolated CAN interface implementation.

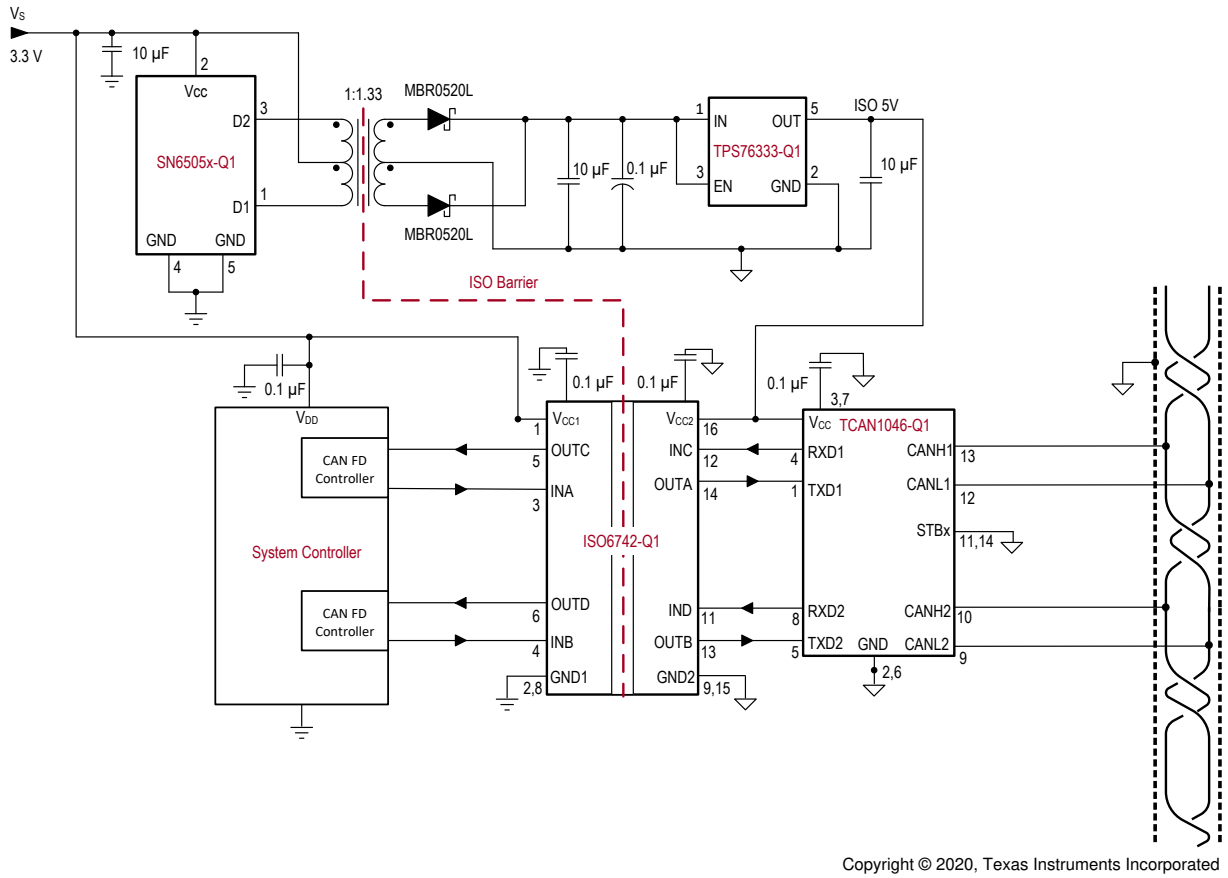

Figure 8-1. Typical Isolated CAN Application Circuit

8.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	1.71 V to 1.89 V and 2.25 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO674x-Q1 family of devices only require two external bypass capacitors to operate.

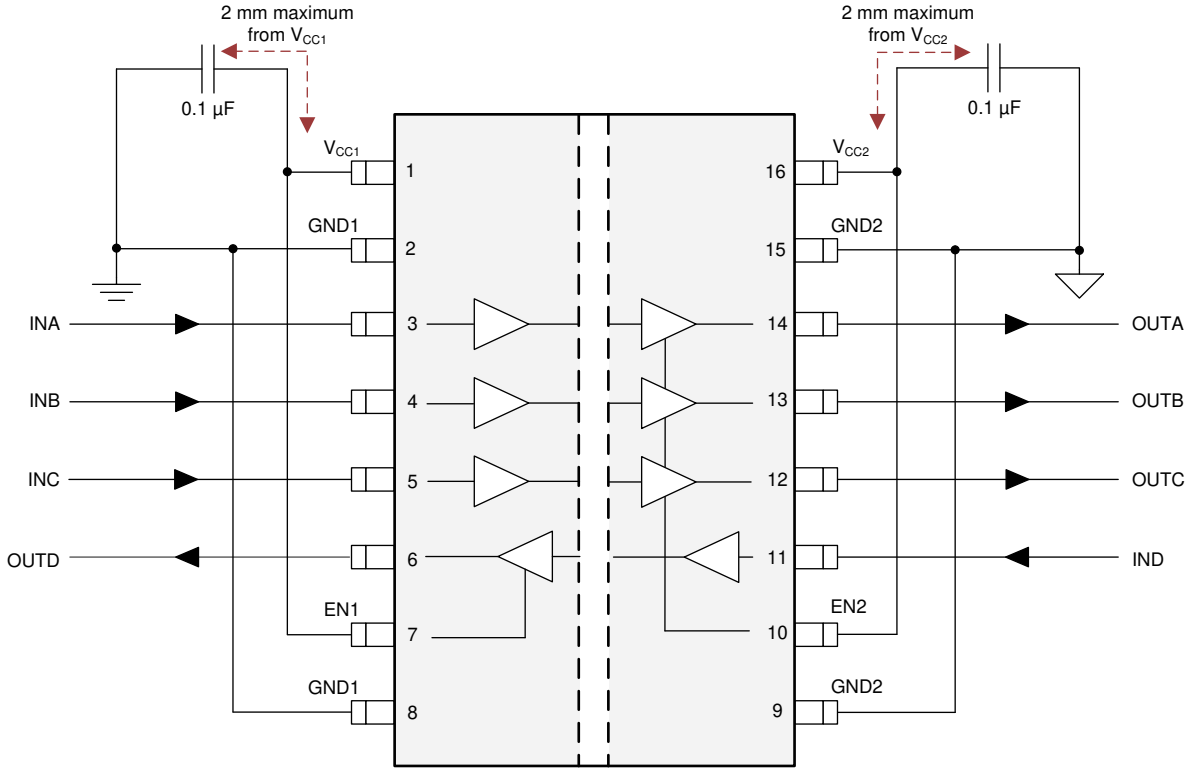

Figure 8-2. Typical ISO674x-Q1 Circuit Hook-up

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8.2.3 Application Curve

The following typical eye diagrams of the ISO674x-Q1 family of devices indicates low jitter and wide open eye at the maximum data rate of 50 Mbps.

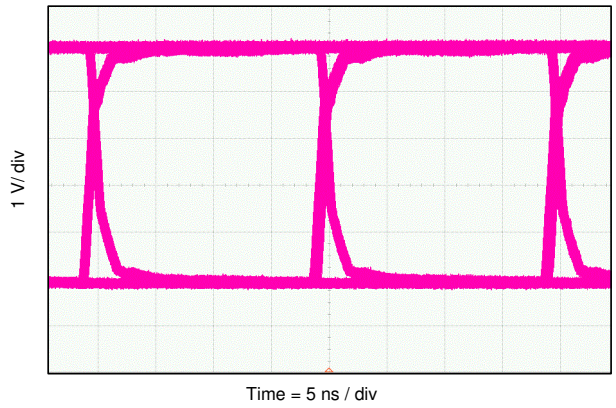

Figure 8-3. Eye Diagram at 50 Mbps PRBS 2^{16} – 1, 5 V and 25°C

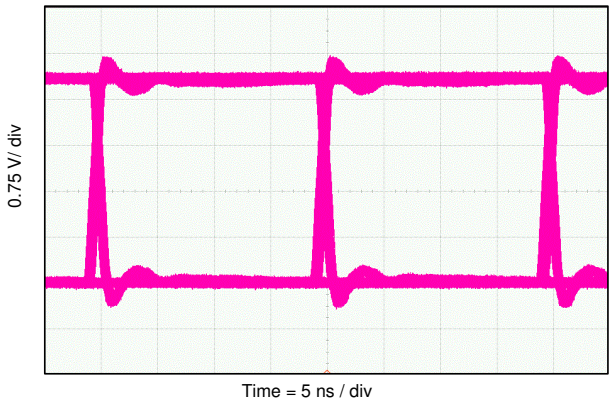

Figure 8-4. Eye Diagram at 50 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

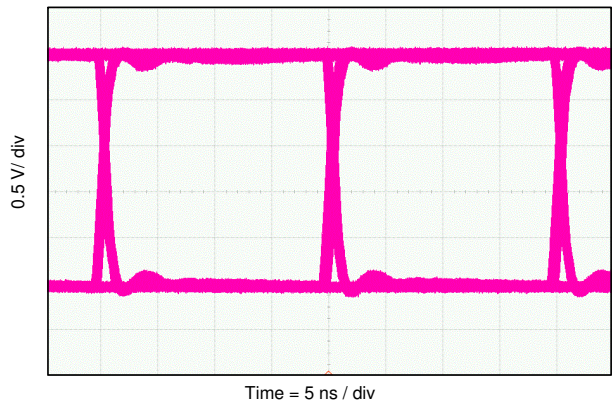

Figure 8-5. Eye Diagram at 50 Mbps PRBS 2^{16} – 1, 2.5 V and 25°C

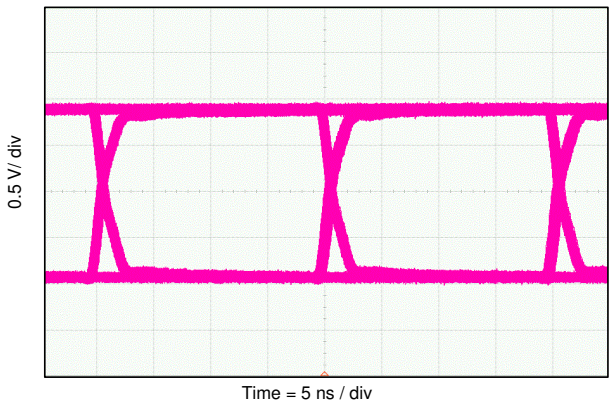

Figure 8-6. Eye Diagram at 50 Mbps PRBS 2^{16} – 1, 1.8 V and 25°C

8.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 8-7 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 8-8 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.

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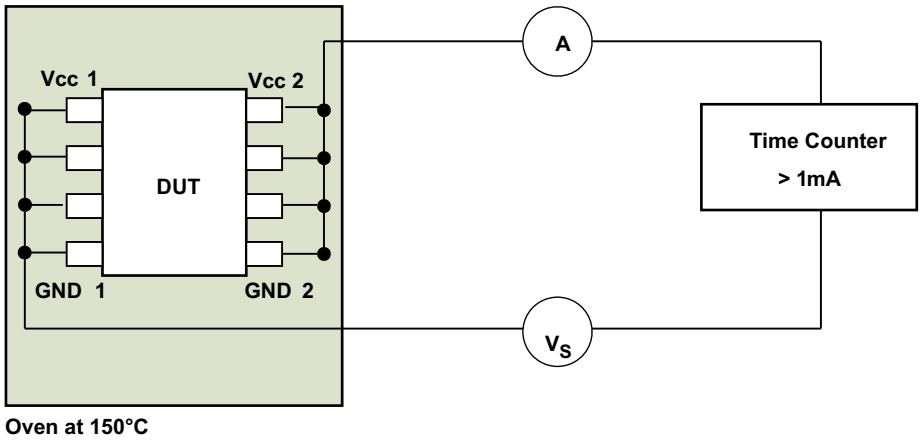

Figure 8-7. Test Setup for Insulation Lifetime Measurement

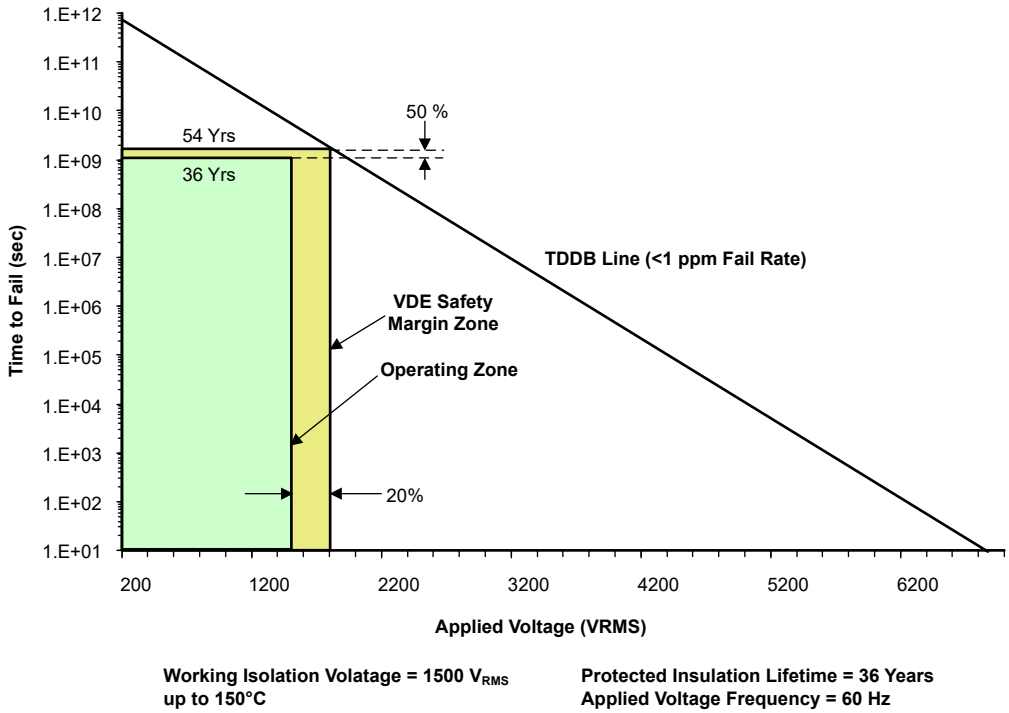

Figure 8-8. Insulation Lifetime Projection Data

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8.3 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For automotive applications, please use SN6501-Q1 or SN6505B-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* or *SN6505B-Q1 Automotive, low-noise, 1-A, 420-kHz transformer driver with soft start for isolated power supplies*.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see Figure 8-10). Layer stacking for a four layer board should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

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8.4.2 Layout Example

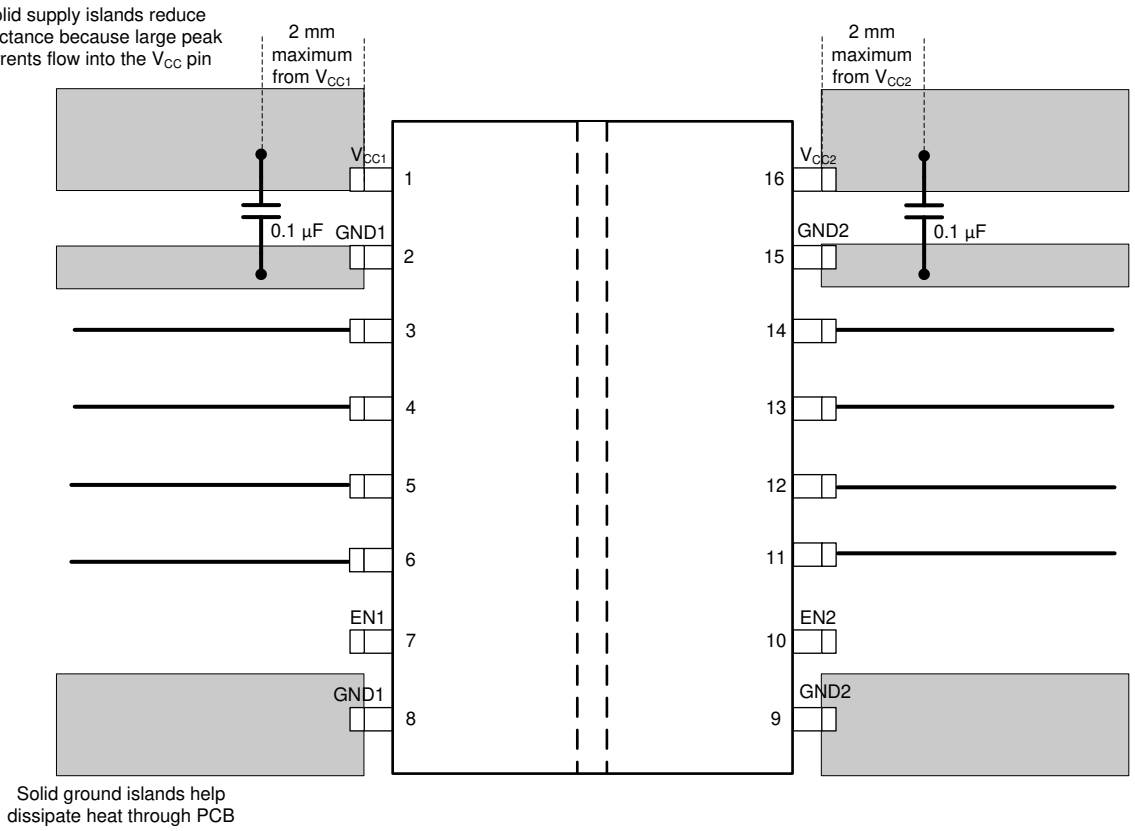

Figure 8-9. Layout Example

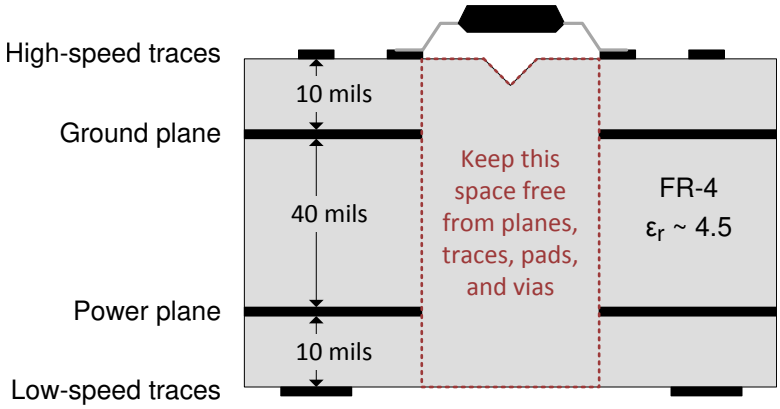

Figure 8-10. Layout Example Schematic

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*, application note
- Texas Instruments, *SN6505x-Q1 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies*, data sheet
- Texas Instruments, *TCAN1044-Q1 Automotive Fault-Protected CAN FD Transceiver*, data sheet
- Texas Instruments, *TPS763xx-Q1 Low-Power, 150-mA, Low-Dropout Linear Regulators* data sheet
- Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers*, data sheet

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (May 2022) to Revision F (May 2024)	Page
• Updated the number format for figures, tables, and cross-references throughout the document	1
• Added Thermal information for ISO6742-Q1 DWW package	8
• Added Safety limiting values for DWW package	11

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Changes from Revision D (July 2021) to Revision E (May 2022)	Page
• Updated CMTI typical to 150 kV/us and minimum to 100 kV/us	6

Changes from Revision C (March 2021) to Revision D (July 2021)	Page
• Updated high lifetime working voltage	1
• Insulation Specifications table 7.6 has been updated with VIOWM 1500Vrms, VIORM at 2121Vpk	6
• Updated Safety-Related Certification table	6
• Updated switching characteristics tables with test conditions for "Default output delay time from input power loss" line item	6
• Updated Typical Application diagram to reflect 5.5Viso	31
• Updated Insulation Lifetime Projection Data image	33
• Updated SN6505A reference with SN6505B in *Power Supply Recommendations*	35

Changes from Revision B (February 2021) to Revision C (March 2021)	Page
• Added ISO6742-Q1 data under Specifications	6
• Updated Typical Application figure	31

Changes from Revision A (January 2021) to Revision B (February 2021)	Page
• Updated device status to Production Data	1

Changes from Revision * (August 2020) to Revision A (January 2021)	Page
• Added ISO674x-Q1 to APL data sheet.	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO6740FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6740F
ISO6740FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6740F
ISO6740FQDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6740QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6740
ISO6740QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6740
ISO6740QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6741FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6741F
ISO6741FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6741F
ISO6741FQDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6741QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6741
ISO6741QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6741
ISO6741QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6742FQDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742F
ISO6742FQDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742F
ISO6742FQDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6742FQDWWRQ1	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742F
ISO6742FQDWWRQ1.A	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742F
ISO6742FQDWWRQ1.B	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6742QDWRQ1	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742
ISO6742QDWRQ1.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742
ISO6742QDWRQ1.B	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
ISO6742QDWWRQ1	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742
ISO6742QDWWRQ1.A	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO6742
ISO6742QDWWRQ1.B	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ISO6740-Q1, ISO6741-Q1, ISO6742-Q1 :

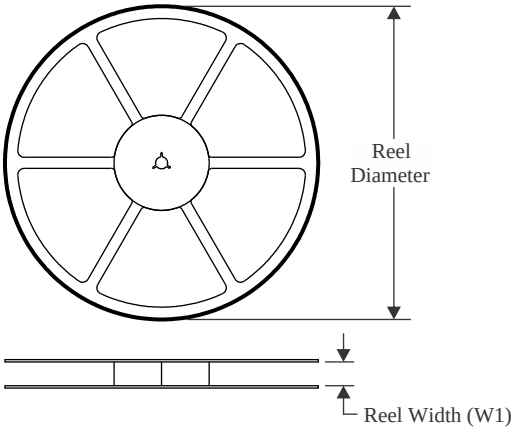
- Catalog : ISO6740, ISO6741, ISO6742

NOTE: Qualified Version Definitions:

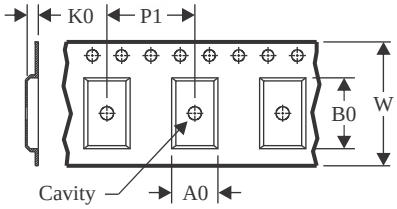
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

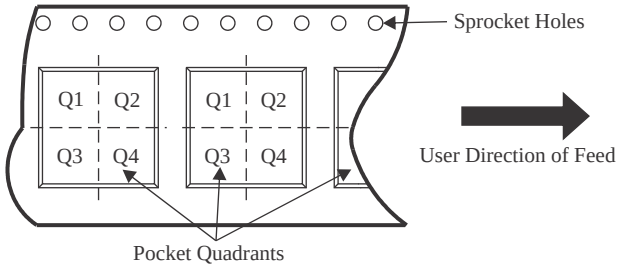


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

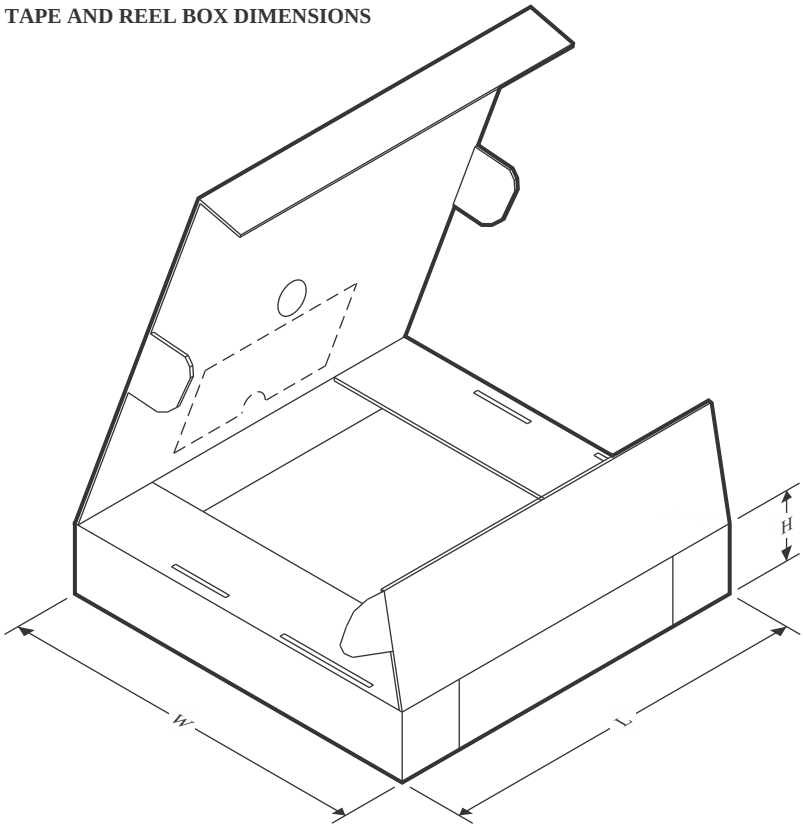
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6740FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6740FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6740QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6741FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6741QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6742FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6742FQDWWRQ1	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO6742QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO6742QDWWRQ1	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

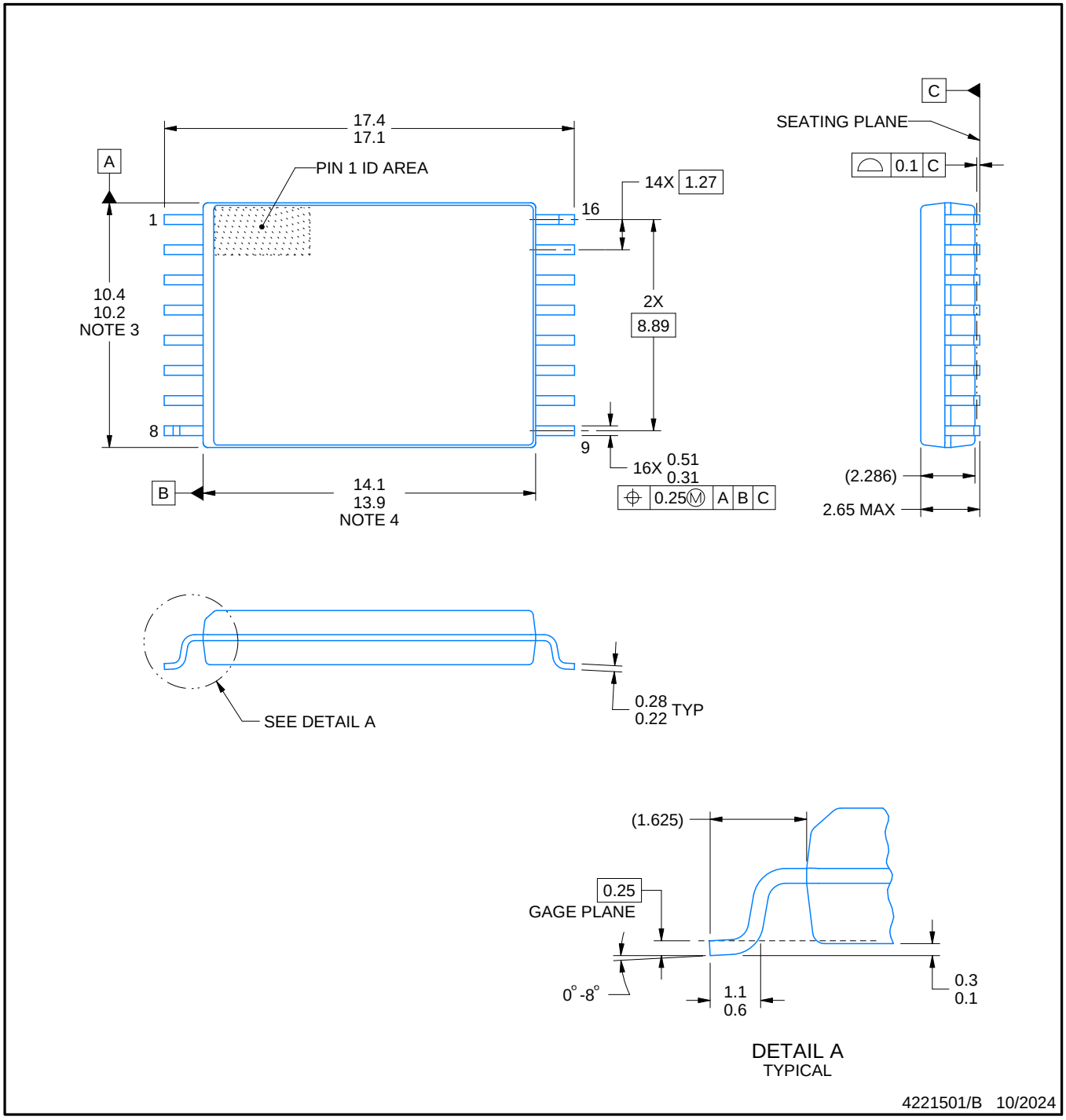
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6740FQDWRQ1	SOIC	DW	16	2000	356.0	356.0	36.0
ISO6740FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6740QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6741FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6741QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6742FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6742FQDWWRQ1	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO6742QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO6742QDWWRQ1	SOIC	DWW	16	1000	350.0	350.0	43.0

PACKAGE OUTLINE

DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



NOTES:

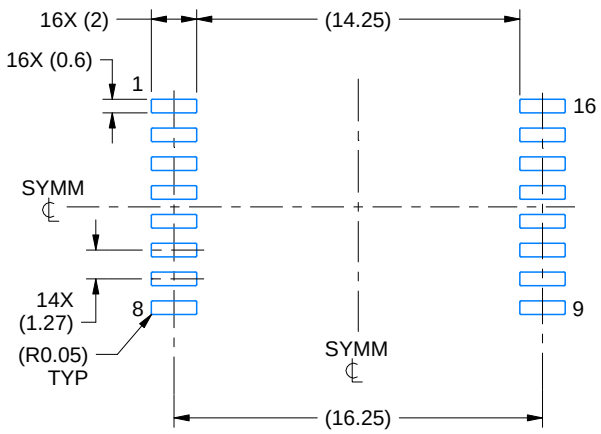
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

EXAMPLE BOARD LAYOUT

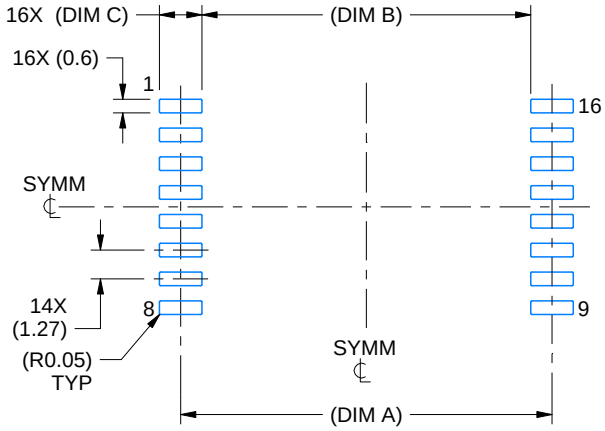
DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE

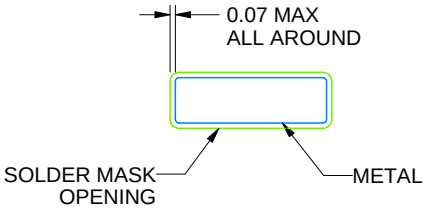


LAND PATTERN EXAMPLE
STANDARD
SCALE:3X

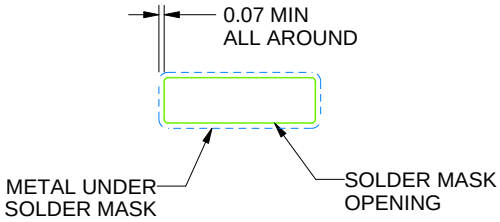


LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525



NON SOLDER MASK
DEFINED
(PREFERRED)



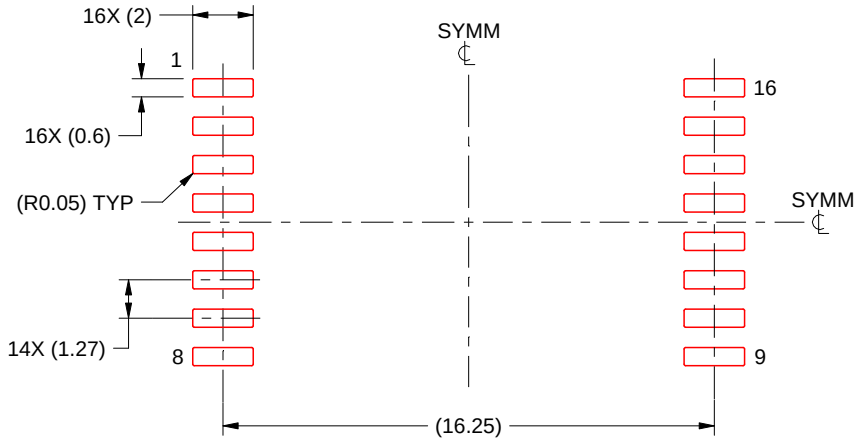
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

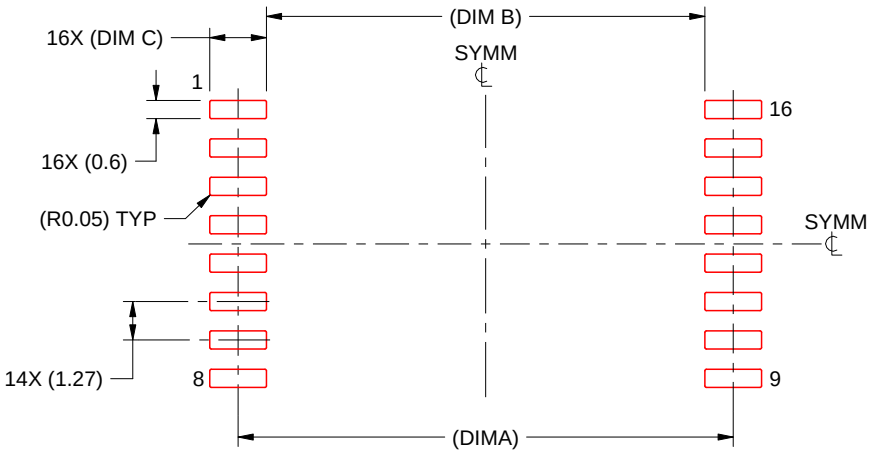
4221501/B 10/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525

4221501/B 10/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

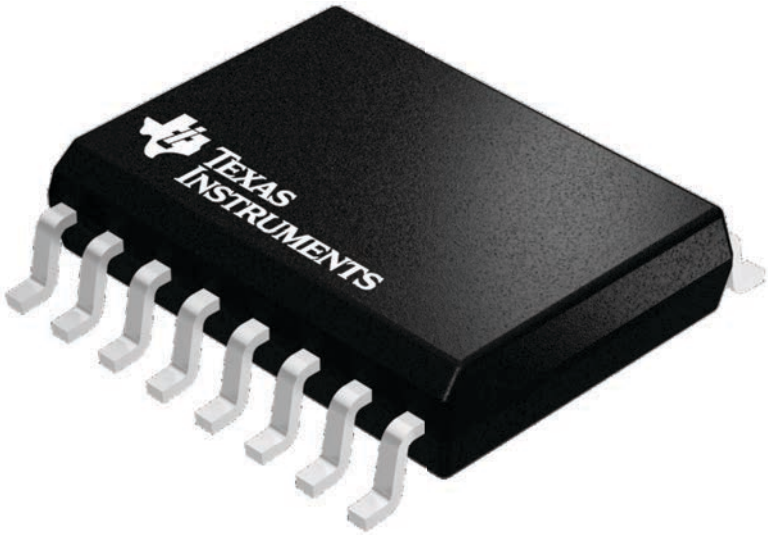
DW 16

SOIC - 2.65 mm max height

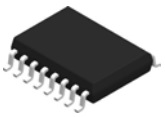
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

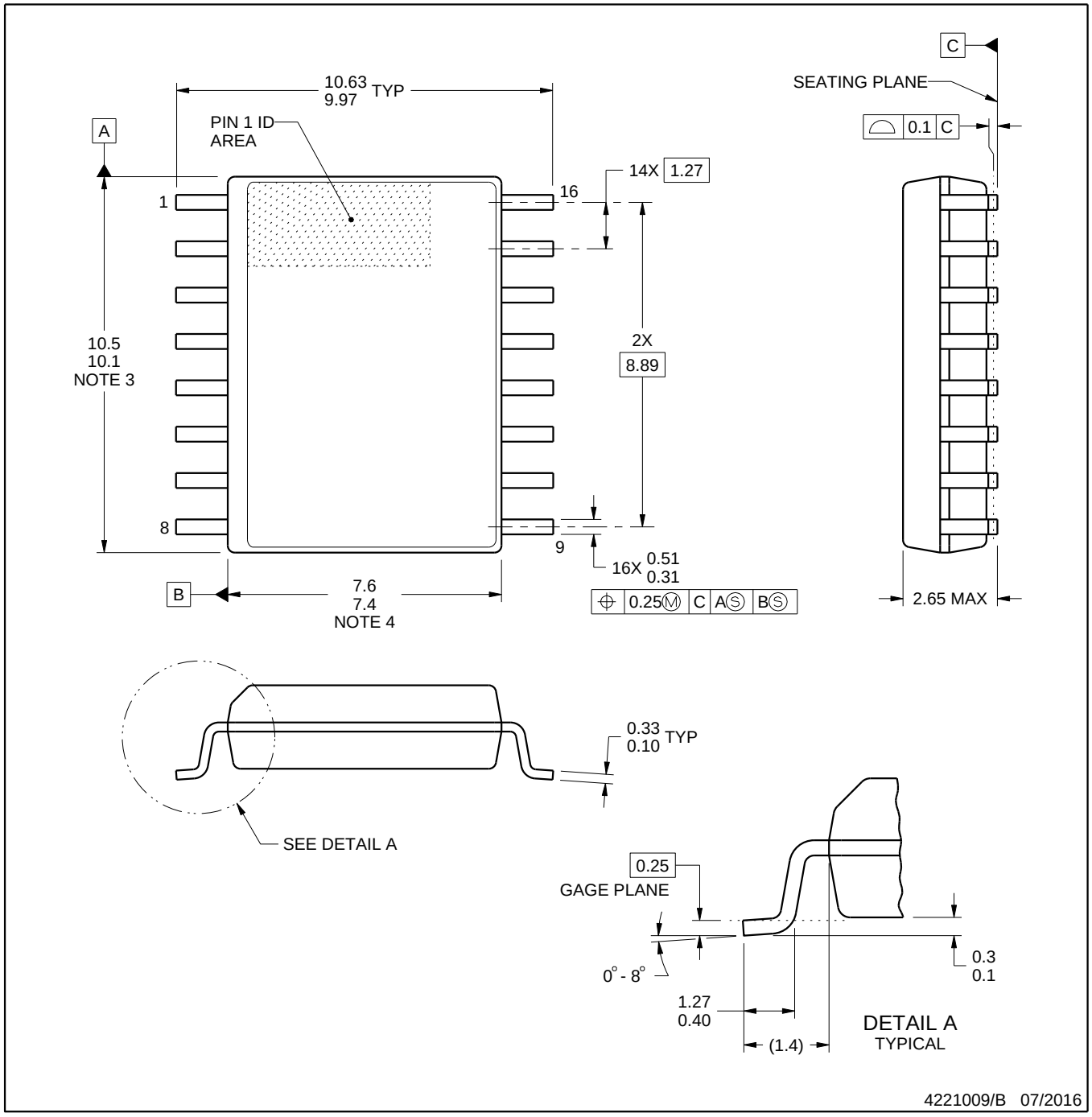


PACKAGE OUTLINE

DW0016B

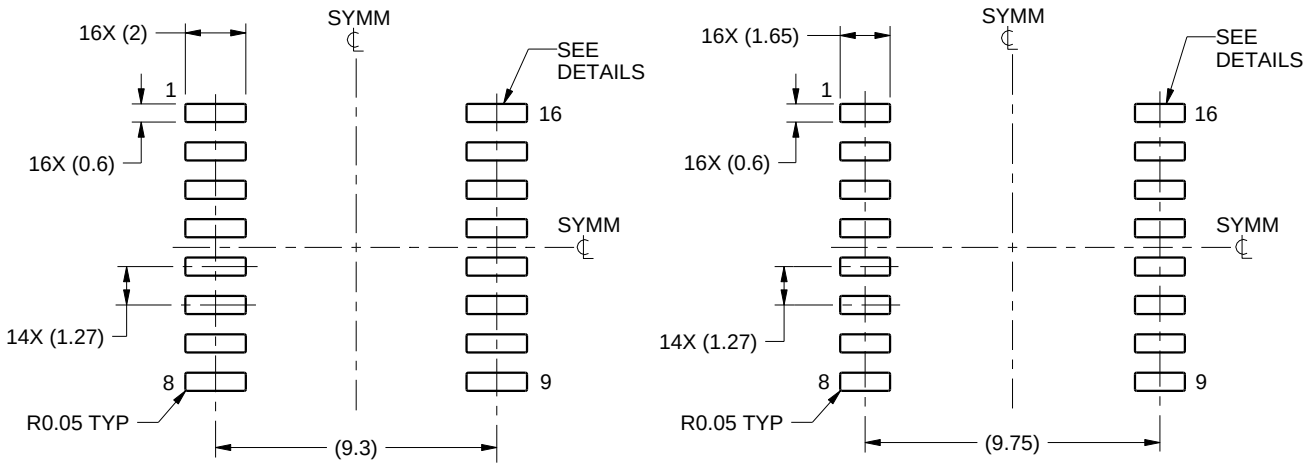
SOIC - 2.65 mm max height

SOIC



NOTES:

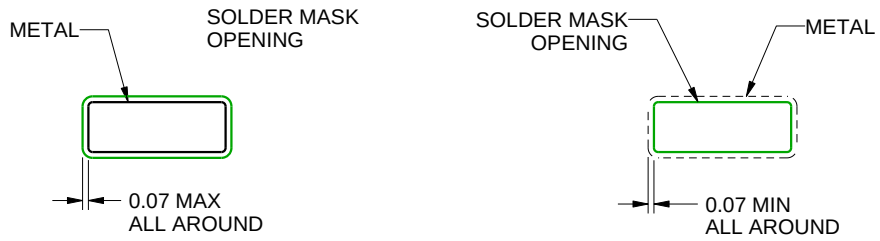
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

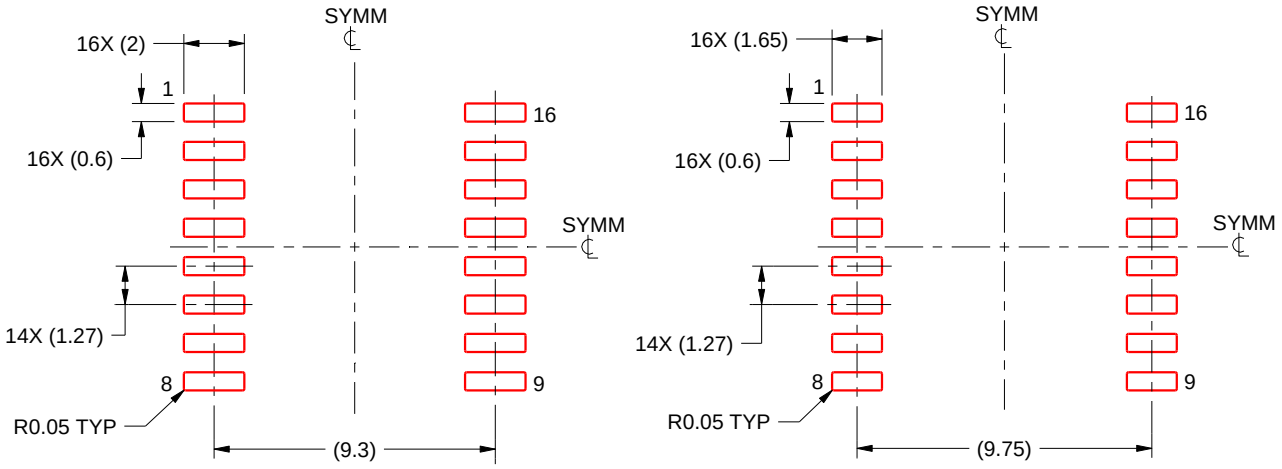
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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