**µA741 General-Purpose Operational Amplifiers**

### 1 Features
- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- No Latch-Up

### 2 Applications
- DVD Recorders and Players
- Pro Audio Mixers

### 3 Description
The µA741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 12.

The µA741C device is characterized for operation from 0°C to 70°C.

### Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>µA741CD</td>
<td>SOIC (8)</td>
<td>4.90 mm x 3.91 mm</td>
</tr>
<tr>
<td>µA741CP</td>
<td>PDIP (8)</td>
<td>9.81 mm x 6.35 mm</td>
</tr>
<tr>
<td>µA741CPS</td>
<td>SO (8)</td>
<td>6.20 mm x 5.30 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

---

**Simplified Schematic**

OFFSET N1

IN +

+     OUT

IN -

OFFSET N2
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4 Revision History

Changes from Revision F (May 2017) to Revision G .............................. Page

   • Changed supply voltage unit from "°C" to "V" in Absolute Maximum Ratings table ........................................... 5

Changes from Revision E (January 2015) to Revision F .............................. Page

   • Updated data sheet text to the latest documentation and translation standards ......................................................... 1
   • Deleted text regarding μA741M device (obsolete package) from Description section ........................................... 1
   • Added μA741CD, μA741CP, and μA741CPS devices to Device Information table .......................................................... 1
   • Deleted μA741x device from Device Information table ........................................................................................... 1
   • Updated pinout diagrams and Pin Functions tables in the Pin Configurations and Functions section ....................... 4
   • Deleted μA741M pinout drawings information from Pin Configurations and Functions section ................................ 4
   • Deleted Electrical Characteristics: μA741M table from Specifications section .......................................................... 5
   • Added operating junction temperature (T_J) and values to Absolute Maximum Ratings table ............................... 5
   • Deleted text regarding μA741M from Absolute Maximum Ratings table ................................................................. 5
   • Deleted text regarding μA741M device from Recommended Operating Conditions table ................................. 5
   • Deleted Dissipation Ratings table ......................................................................................................................... 5
   • Added Thermal Information table and values ......................................................................................................... 5
   • Deleted μA741M in Switching Characteristics table ................................................................................................ 7
   • Correct typo in Figure 1 ........................................................................................................................................... 8
   • Deleted text regarding μA741M device from Detailed Description section .............................................................. 10
   • Updated text in Overview section ............................................................................................................................ 10
   • Added 2017 copyright to Functional Block Diagram ................................................................................................ 10
   • Added caption to Figure 11 in Device Functional Modes section .................................................................................... 11
   • Changed pins 1 and 5 from "NC" to "Offset N1" and "Offset N2" in Figure 18 ........................................................................ 15
Changes from Revision D (February 2014) to Revision E

- Added Applications, Device Information table, Pin Functions table, ESD Ratings table, Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. .......................................................... 1
- Moved Typical Characteristics into Specifications section. .......................................................... 8

Changes from Revision C (January 2014) to Revision D

- Fixed Typical Characteristics graphs to remove extra lines. .......................................................... 8

Changes from Revision B (September 2000) to Revision C

- Updated document to new TI data sheet format - no specification changes. .......................................................... 1
- Deleted Ordering Information table. ......................................................................................... 1
5 Pin Configurations and Functions

uA741C D, P, or PS Package
8-Pin SOIC, PDIP, SO
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN+</td>
<td>I</td>
<td>Noninverting input</td>
</tr>
<tr>
<td>IN−</td>
<td>I</td>
<td>Inverting input</td>
</tr>
<tr>
<td>NC</td>
<td></td>
<td>No internal connection</td>
</tr>
<tr>
<td>OFFSET N1</td>
<td>I</td>
<td>External input offset voltage adjustment</td>
</tr>
<tr>
<td>OFFSET N2</td>
<td>I</td>
<td>External input offset voltage adjustment</td>
</tr>
<tr>
<td>OUT</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>VCC+</td>
<td></td>
<td>Positive supply</td>
</tr>
<tr>
<td>VCC−</td>
<td></td>
<td>Negative supply</td>
</tr>
</tbody>
</table>

NC- no internal connection

Submit Documentation Feedback
6 Specifications

6.1 Absolute Maximum Ratings

over virtual junction temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, (V_{CC})(^{(2)})</td>
<td>(\mu A741C)</td>
<td>–18</td>
<td>18</td>
</tr>
<tr>
<td>Differential input voltage, (V_D)(^{(3)})</td>
<td>(\mu A741C)</td>
<td>–15</td>
<td>15</td>
</tr>
<tr>
<td>Input voltage, (V_i) (any input) (^{(2)})(4)</td>
<td>(\mu A741C)</td>
<td>–15</td>
<td>15</td>
</tr>
<tr>
<td>Voltage between offset null (either OFFSET N1 or OFFSET N2) and (V_{CC–})</td>
<td>(\mu A741C)</td>
<td>–15</td>
<td>15</td>
</tr>
<tr>
<td>Duration of output short circuit(^{(5)})</td>
<td>Unlimited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
<td>See Thermal Information</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Case temperature for 60 seconds</td>
<td>(\mu A741C)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds</td>
<td>(\mu A741C)</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds</td>
<td>D, P, or PS package</td>
<td>(\mu A741C)</td>
<td>260</td>
</tr>
<tr>
<td>Operating junction temperature, (T_J)</td>
<td>(\mu A741C)</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>Storage temperature range, (T_{stg})</td>
<td>(\mu A741C)</td>
<td>–65</td>
<td>150</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) All voltage values, unless otherwise noted, are with respect to the midpoint between \(V_{CC+}\) and \(V_{CC–}\).

\(^{(3)}\) Differential voltages are at \(I_{IN}+\) with respect to \(I_{IN}–\).

\(^{(4)}\) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

\(^{(5)}\) The output may be shorted to ground or either power supply.

6.2 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>(V_{CC+}) Supply voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC–}) Operating free-air temperature</td>
<td>(\mu A741C)</td>
<td>0</td>
<td>70</td>
</tr>
</tbody>
</table>

\(T_{JA}\) Operating free-air temperature

<table>
<thead>
<tr>
<th>(V_{CC+})</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC–})</td>
<td>5</td>
<td>15</td>
<td>V</td>
</tr>
<tr>
<td>(T_{JA})</td>
<td>–5</td>
<td>–15</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.3 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>(\mu A741)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>129.2</td>
<td>87.4</td>
</tr>
<tr>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>73.6</td>
<td>89.3</td>
</tr>
<tr>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>72.4</td>
<td>64.4</td>
</tr>
<tr>
<td>(V_{JT}) Junction-to-top characterization parameter</td>
<td>25.9</td>
<td>49.8</td>
</tr>
<tr>
<td>(V_{JB}) Junction-to-board characterization parameter</td>
<td>71.7</td>
<td>64.1</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
### 6.4 Electrical Characteristics: μA741C

at specified virtual junction temperature, $V_{CC} = \pm 15$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IC}$  Input offset voltage</td>
<td>$V_O = 0$ 25°C</td>
<td>1</td>
<td>6</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{IO(adj)}$ Offset voltage adjust range</td>
<td>$V_O = 0$ 25°C</td>
<td>-</td>
<td>-</td>
<td>±15</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{IO}$  Input offset current</td>
<td>$V_O = 0$ 25°C</td>
<td>20</td>
<td>200</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$I_{IB}$  Input bias current</td>
<td>$V_O = 0$ 25°C</td>
<td>80</td>
<td>500</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{ICR}$ Common-mode input voltage range</td>
<td>25°C</td>
<td>±12</td>
<td>±13</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OM}$ Maximum peak output voltage swing</td>
<td>$R_L = 10$ kΩ 25°C</td>
<td>±12</td>
<td>±14</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$A_{Vd}$ Large-signal differential voltage amplification</td>
<td>$R_L = 2$ kΩ 25°C</td>
<td>20</td>
<td>200</td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td>$r_i$ Input resistance</td>
<td>25°C</td>
<td>0.3</td>
<td>2</td>
<td></td>
<td>MΩ</td>
</tr>
<tr>
<td>$C_i$ Input capacitance</td>
<td>25°C</td>
<td>1.4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CMRR Common-mode rejection ratio</td>
<td>$V_{IC} = V_{IC(min)}$ 25°C</td>
<td>70</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$k_{SVS}$ Supply voltage sensitivity ($\Delta V_{O}/\Delta V_{CC}$)</td>
<td>$V_{CC} = \pm 9$ V to ±15 V 25°C</td>
<td>30</td>
<td>150</td>
<td></td>
<td>μV/V</td>
</tr>
<tr>
<td>$I_{OS}$ Short-circuit output current</td>
<td>25°C</td>
<td>±25</td>
<td>±40</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CC}$ Supply current</td>
<td>$V_O = 0$; no load 25°C</td>
<td>1.7</td>
<td>2.8</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$P_D$ Total power dissipation</td>
<td>$V_O = 0$; no load 25°C</td>
<td>50</td>
<td>85</td>
<td></td>
<td>mW</td>
</tr>
</tbody>
</table>

(1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the μA741C is 0°C to 70°C.
(2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.
### 6.5 Electrical Characteristics: μA741Y

at specified virtual junction temperature, \( V_{CCx} = \pm 15 \text{ V}, \ T_A = 25^\circ\text{C} \) (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS (^{(2)})</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IO} ) Input offset voltage</td>
<td>( V_O = 0 )</td>
<td>1</td>
<td>5</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( \Delta V_{IO(adj)} ) Offset voltage adjust range</td>
<td>( V_O = 0 )</td>
<td>±15</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_O ) Input offset current</td>
<td>( V_O = 0 )</td>
<td>20</td>
<td>200</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>( I_{IB} ) Input bias current</td>
<td>( V_O = 0 )</td>
<td>80</td>
<td>500</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>( V_{ICR} ) Common-mode input voltage range</td>
<td></td>
<td>±12</td>
<td>±13</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{OM} ) Maximum peak output voltage swing</td>
<td>( R_L = 10 \text{ k}\Omega )</td>
<td>±12</td>
<td>±14</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_L = 2 \text{ k}\Omega )</td>
<td>±10</td>
<td>±13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( A_{VO} ) Large-signal differential voltage amplification</td>
<td>( R_L \geq 2 \text{ k}\Omega )</td>
<td>20</td>
<td>200</td>
<td>V/mV</td>
<td></td>
</tr>
<tr>
<td>( r_i ) Input resistance</td>
<td>0.3</td>
<td>2</td>
<td>MΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( r_o ) Output resistance</td>
<td>( V_O = 0; \text{ see } (1) )</td>
<td>75</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_i ) Input capacitance</td>
<td>1.4</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{CMRR} ) Common-mode rejection ratio</td>
<td>( V_{IC} = V_{CRmin} )</td>
<td>70</td>
<td>90</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>( k_{SVS} ) Supply voltage sensitivity (( \Delta V_O/\Delta V_{CC} ))</td>
<td>( V_{CC} = \pm 9 \text{ V to } \pm 15 \text{ V} )</td>
<td>30</td>
<td>150</td>
<td>µV/V</td>
<td></td>
</tr>
<tr>
<td>( I_{OS} ) Short-circuit output current</td>
<td>0.25</td>
<td>±40</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{CC} ) Supply current</td>
<td>( V_O = 0; \text{ no load} )</td>
<td>1.7</td>
<td>2.8</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( P_D ) Total power dissipation</td>
<td>( V_O = 0; \text{ no load} )</td>
<td>50</td>
<td>85</td>
<td>mW</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

\(^{(2)}\) All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

### 6.6 Switching Characteristics: μA741C

over operating free-air temperature range, \( V_{CCx} = \pm 15 \text{ V}, \ T_A = 25^\circ\text{C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_r ) Rise time</td>
<td>( V_I = 20 \text{ mV}, \ R_L = 2 \text{ k}\Omega )</td>
<td>0.3</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overshoot factor</td>
<td></td>
<td>5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{SR} ) Slew rate at unity gain</td>
<td>( V_I = 10 \text{ V}, \ R_L = 2 \text{ k}\Omega )</td>
<td>0.5</td>
<td>V/µs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 6.7 Switching Characteristics: μA741Y

over operating free-air temperature range, \( V_{CCx} = \pm 15 \text{ V}, \ T_A = 25^\circ\text{C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_r ) Rise time</td>
<td>( V_I = 20 \text{ mV}, \ R_L = 2 \text{ k}\Omega )</td>
<td>0.3</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overshoot factor</td>
<td>( C_L = 100 \text{ pF}; \text{ see } \text{ Figure 1} )</td>
<td>5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{SR} ) Slew rate at unity gain</td>
<td>( V_I = 10 \text{ V}, \ R_L = 2 \text{ k}\Omega )</td>
<td>0.5</td>
<td>V/µs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.8 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

![Input Voltage Waveform](image)

**Figure 1. Rise Time, Overshoot, and Slew Rate**

**Figure 2. Input Offset Current vs Free-Air Temperature**

**Figure 3. Input Bias Current vs Free-Air Temperature**

**Figure 4. Maximum Output Voltage vs Load Resistance**

**Figure 5. Maximum Peak Output Voltage vs Frequency**
Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

![Figure 6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage](image)

![Figure 7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency](image)

![Figure 8. Common-Mode Rejection Ratio vs Frequency](image)

![Figure 9. Output Voltage vs Elapsed Time](image)

![Figure 10. Voltage-Follower Large-Signal Pulse Response](image)
7 Detailed Description

7.1 Overview
The μA741 has been a popular operational amplifier for over four decades. Typical open loop gain is 106 dB while driving a 2000-Ω load. Short circuit tolerance, offset voltage trimming, and unity-gain stability makes the μA741 useful for many applications.

7.2 Functional Block Diagram

![Functional Block Diagram]

Component Count

<table>
<thead>
<tr>
<th>Component</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistors</td>
<td>22</td>
</tr>
<tr>
<td>Resistors</td>
<td>11</td>
</tr>
<tr>
<td>Diode</td>
<td>1</td>
</tr>
<tr>
<td>Capacitor</td>
<td>1</td>
</tr>
</tbody>
</table>

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7.3 Feature Description

7.3.1 Offset-Voltage Null Capability
The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches caused by external circuitry. See Application and Implementation for more details on design techniques.
Feature Description (continued)

7.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change an output when there is a change on the input. The µA741 device has a 0.5-V/μs slew rate. Parameters that vary significantly with operating voltages or temperature are shown in Typical Characteristics.

7.4 Device Functional Modes

The µA741 device is powered on when the power supply is connected. The device can operate as a single-supply or dual-supply operational amplifier depending on the application.

7.5 µA741Y Chip Information

When properly assembled, this chip displays characteristics similar to the µA741C device. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.

Figure 11. Bonding Pad Assignments
8 Application and Implementation

**NOTE**
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas \( \beta \), collector or emitter resistors and so forth. The input offset pins allow the designer to adjust for mismatches resulting from external circuitry. These input mismatches can be adjusted by placing resistors or a potentiometer between the inputs as shown in Figure 12. A potentiometer can fine-tune the circuit during testing or for applications which require precision offset control. For more information about designing using the input-offset pins, see *Nulling Input Offset Voltage of Operational Amplifiers*.

![Figure 12. Input Offset Voltage Null Circuit](image)

8.2 Typical Application
The voltage follower configuration of the operational amplifier is used for applications where a weak signal drives a relatively high current load. This circuit is also called a buffer amplifier or unity-gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so the resistance can provide as much current as necessary to the output load.

![Figure 13. Voltage Follower Schematic](image)
Typical Application (continued)

8.2.1 Design Requirements
- Output range from 2 V to 11.5 V
- Input range from 2 V to 11.5 V
- Resistive feedback to negative input

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by the internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ±12 V, which accommodates the input and output voltage requirements.

8.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The selected amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11.5 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail rather than ground allows the amplifier to maintain linearity for inputs below 2 V.

8.2.3 Application Curves for Output Characteristics

![Figure 14. Output Voltage vs Input Voltage](image1)

![Figure 15. Current Drawn Input of Voltage Follower (I\textsubscript{IO}) vs Input Voltage](image2)

![Figure 16. Current Drawn from Supply (I\textsubscript{CC}) vs Input Voltage](image3)
9 Power Supply Recommendations

The μA741 device is specified for operation from ±5 to ±15 V; many specifications apply from 0°C to 70°C. Typical Characteristics presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see Layout Guidelines.

CAUTION

Supply voltages larger than ±18 V can permanently damage the device (see Absolute Maximum Ratings).

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

• Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
• Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see Circuit Board Layout Techniques.
• To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
• Place the external components as close as possible to the device. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Layout Example.
• Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
• Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

Figure 17. Operational Amplifier Schematic for Noninverting Configuration
Layout Example (continued)

Run the input traces as far away from the supply lines as possible. Place components close to device and to each other to reduce parasitic errors. Only needed for dual-supply operation.

(Or GND for single supply)

Ground (GND) plane on another layer

Use low-ESR, ceramic bypass capacitor

Figure 18. Operational Amplifier Board Layout for Noninverting Configuration
11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Trademarks
All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

Tape Dimensions

A0 Dimension designed to accommodate the component width
B0 Dimension designed to accommodate the component length
K0 Dimension designed to accommodate the component thickness
W Overall width of the carrier tape
P1 Pitch between successive cavity centers

TAPE DIMENSIONS

Pocket Quadrants

Sprocket Holes

User Direction of Feed

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MS-001 variation BA.
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