CSD18501Q5A 40 V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

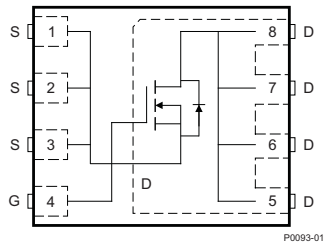
2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Battery Motor Control

3 Description

This 40 V, 2.5 mΩ, SON 5 × 6 mm NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	40		V
Q_g	Gate Charge Total (4.5 V)	20		nC
Q_{gd}	Gate Charge Gate-to-Drain	5.9		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V	3.3	mΩ
		V_{GS} = 10 V	2.5	mΩ
$V_{GS(th)}$	Threshold Voltage	1.8		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD18501Q5A	2500	13-Inch Reel	SON 5 mm × 6 mm Plastic Package	Tape and Reel
CSD18501Q5AT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

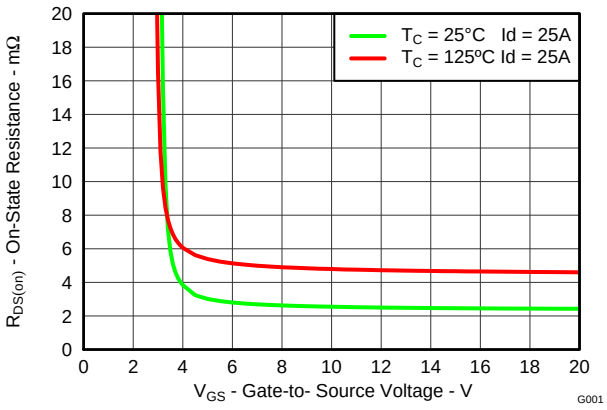
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	161	
	Continuous Drain Current (1)	22	A
I_{DM}	Pulsed Drain Current (2)	400	A
P_D	Power Dissipation(1)	3.1	W
	Power Dissipation, T_C = 25°C	150	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 68 A, L = 0.1 mH, R_G = 25 Ω	231	mJ

(1) Typical $R_{\theta JA}$ = 40°C/W on a 1-inch^2, 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.0°C/W, Pulse duration ≤100µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge

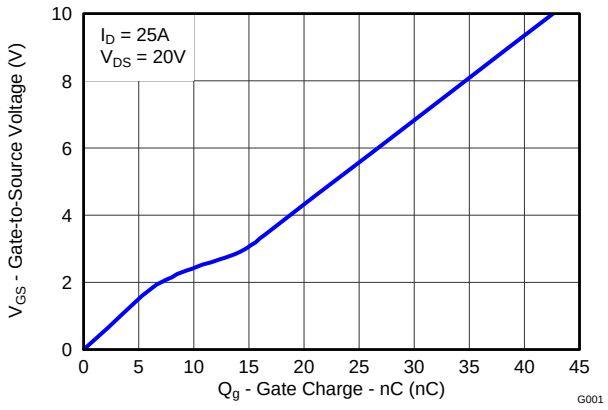


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2012) to Revision C — **Page**

- Added part number to title ... 1
- Added 7-inch reel to Ordering Information table ... 1
- Increased silicon limited continuous drain current to 161 A ... 1
- Increased pulsed drain current to 400 A ... 1
- Added line for max power dissipation with case temperature held to 25° C ... 1
- Updated pulsed current conditions ... 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve ... 4
- Updated the SOA in Figure 9 ... 6
- Added Recommended Stencil Opening ... 9

Changes from Revision A (June 2012) to Revision B — **Page**

- Changed the Transconductance TYP value From: 142 S To: 118 S. ... 3
- Changed the Turn On and Turn Off Delay Time, Rise and Fall Time Test Conditions From: I_{DS} = 25 A, R_G = 2 Ω To: I_{DS} = 25 A, R_G = 0 Ω ... 3
- Changed the Q_{rr} Reverse Recovery Charge TYP value From: 21 nC To: 70 nC ... 3

Changes from Original (June 2012) to Revision A — **Page**

- Added "T_A = 25°C" to the Product Summary table ... 1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

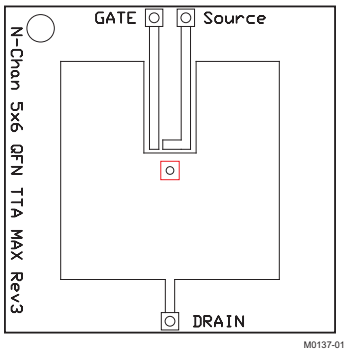
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 32 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.4	1.8	2.3	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 25 A		3.3	4.3	mΩ
		V_{GS} = 10 V, I_D = 25 A		2.5	3.2	mΩ
g_{fs}	Transconductance	V_{DS} = 20 V, I_D = 25 A		118		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz		3200	3840	pF
C_{oss}	Output Capacitance			725	870	pF
C_{rss}	Reverse Transfer Capacitance			18	23	pF
R_G	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 20 V, I_D = 25 A		20	24	nC
Q_g	Gate Charge Total (10 V)			42	50	
Q_{gd}	Gate Charge Gate-to-Drain			5.9		nC
Q_{gs}	Gate Charge Gate-to-Source			8.1		nC
$Q_{g(th)}$	Gate Charge at Vth			5.7		nC
Q_{oss}	Output Charge	V_{DS} = 20 V, V_{GS} = 0 V		48		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 20 V, V_{GS} = 10 V, I_{DS} = 25 A, R_G = 0		4.7		ns
t_r	Rise Time			10		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			3.4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{DS} = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 20 V, I_F = 25 A, di/dt = 300 A/µs		70		nC
t_{rr}	Reverse Recovery Time			40		ns

5.2 Thermal Information

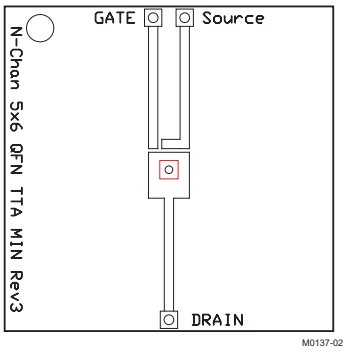
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			50	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45-cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

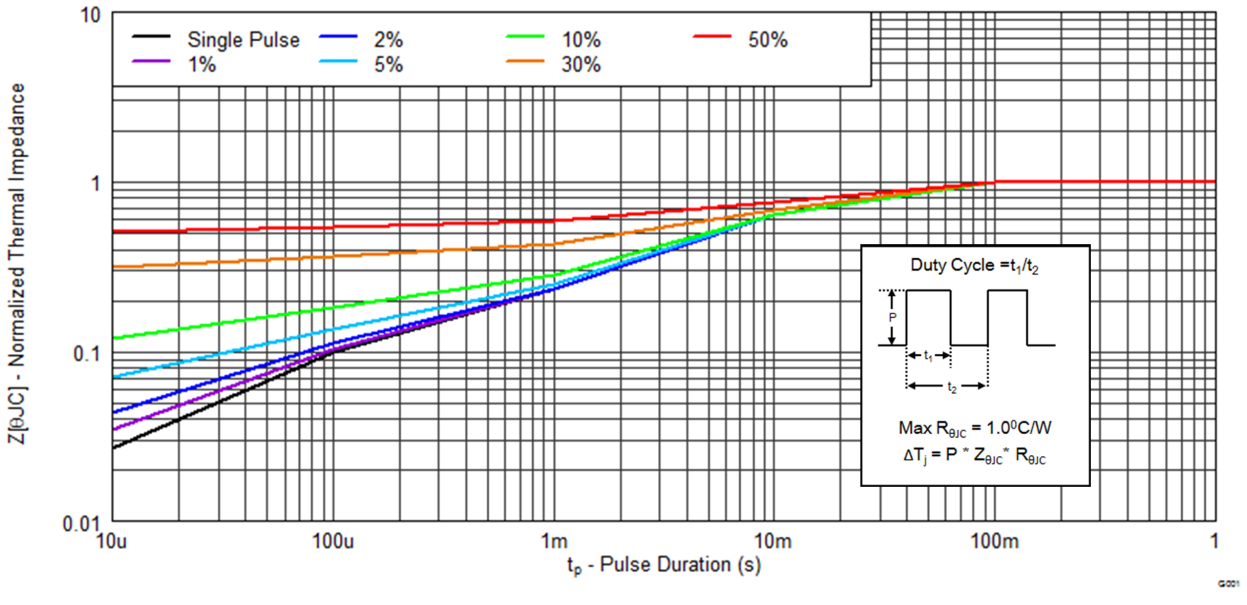


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

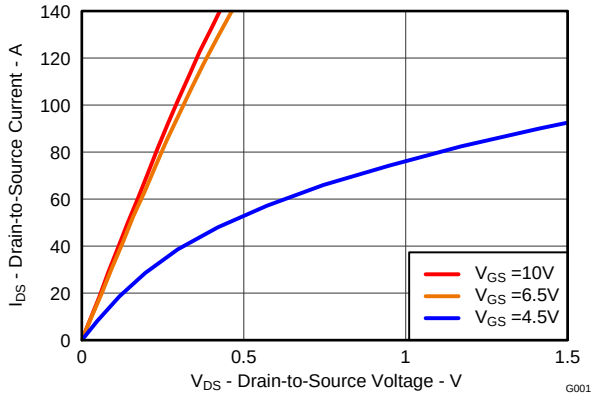


Figure 2. Saturation Characteristics

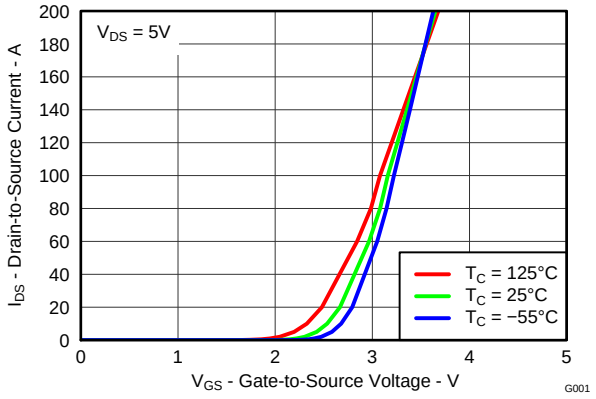


Figure 3. Transfer Characteristics

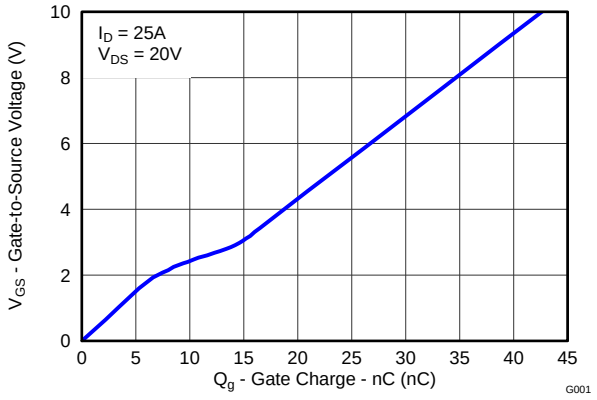


Figure 4. Gate Charge

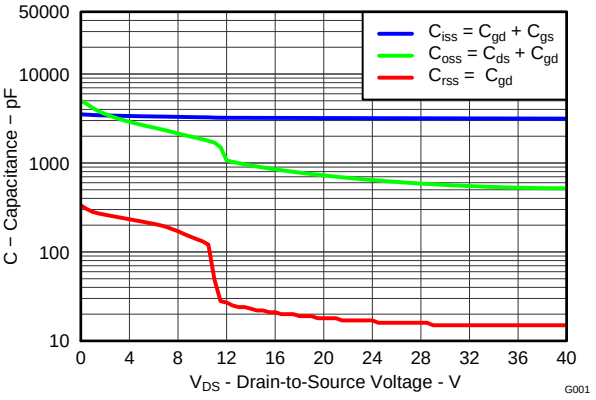


Figure 5. Capacitance

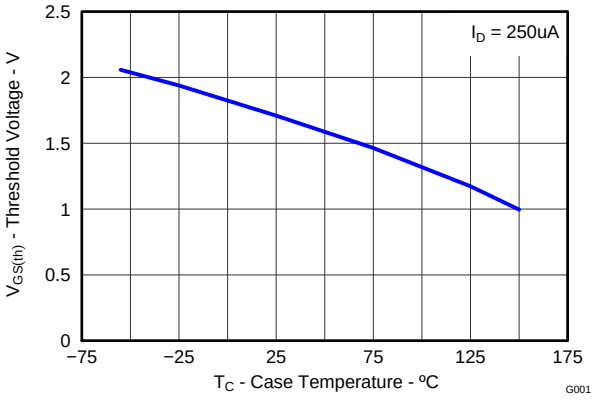


Figure 6. Threshold Voltage vs Temperature

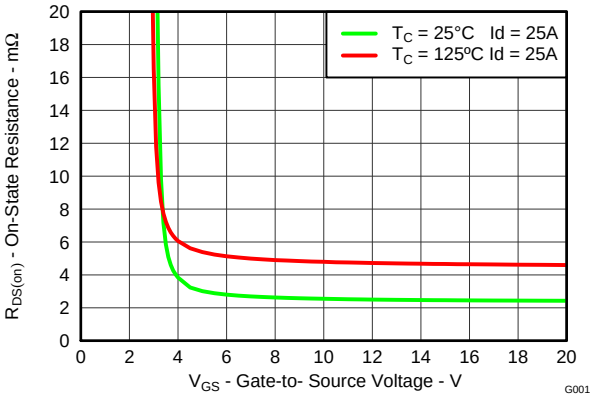


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

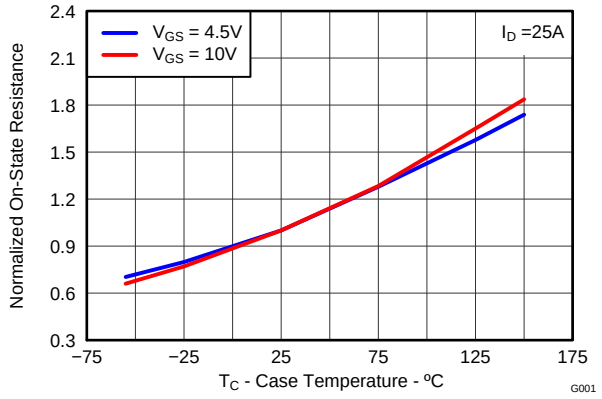


Figure 8. Normalized On-State Resistance vs Temperature

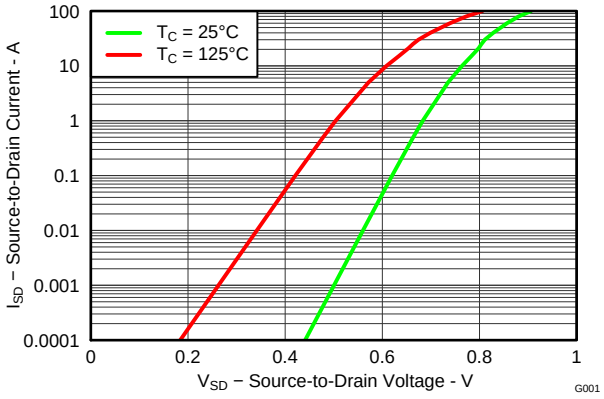


Figure 9. Typical Diode Forward Voltage

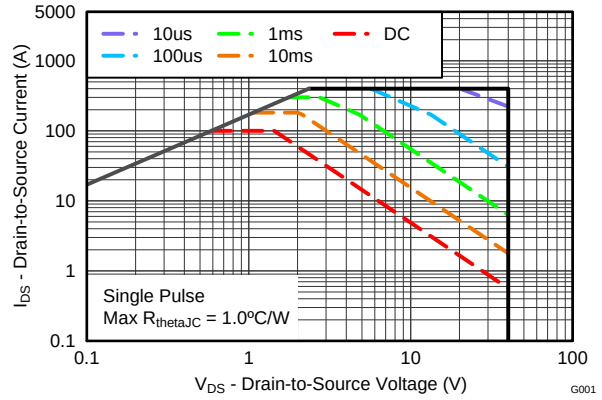


Figure 10. Maximum Safe Operating Area

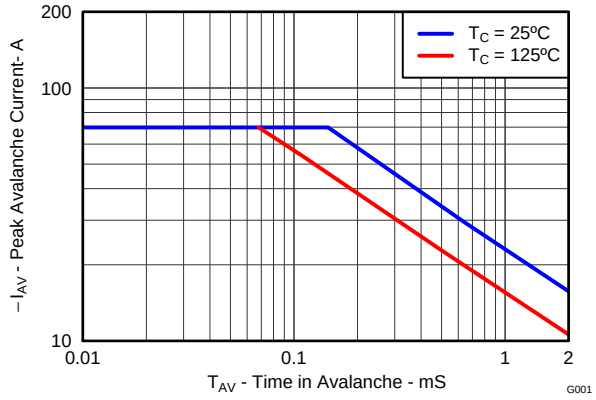


Figure 11. Single Pulse Unclamped Inductive Switching

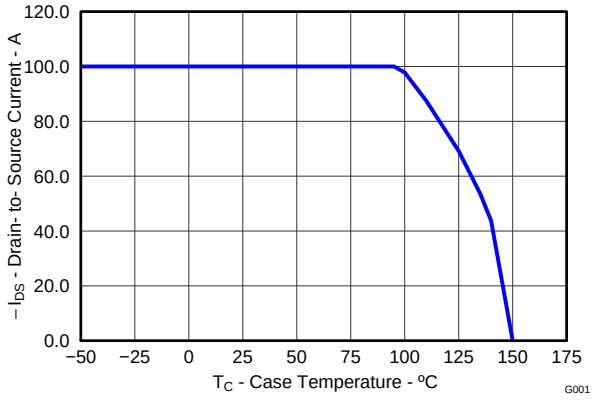


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

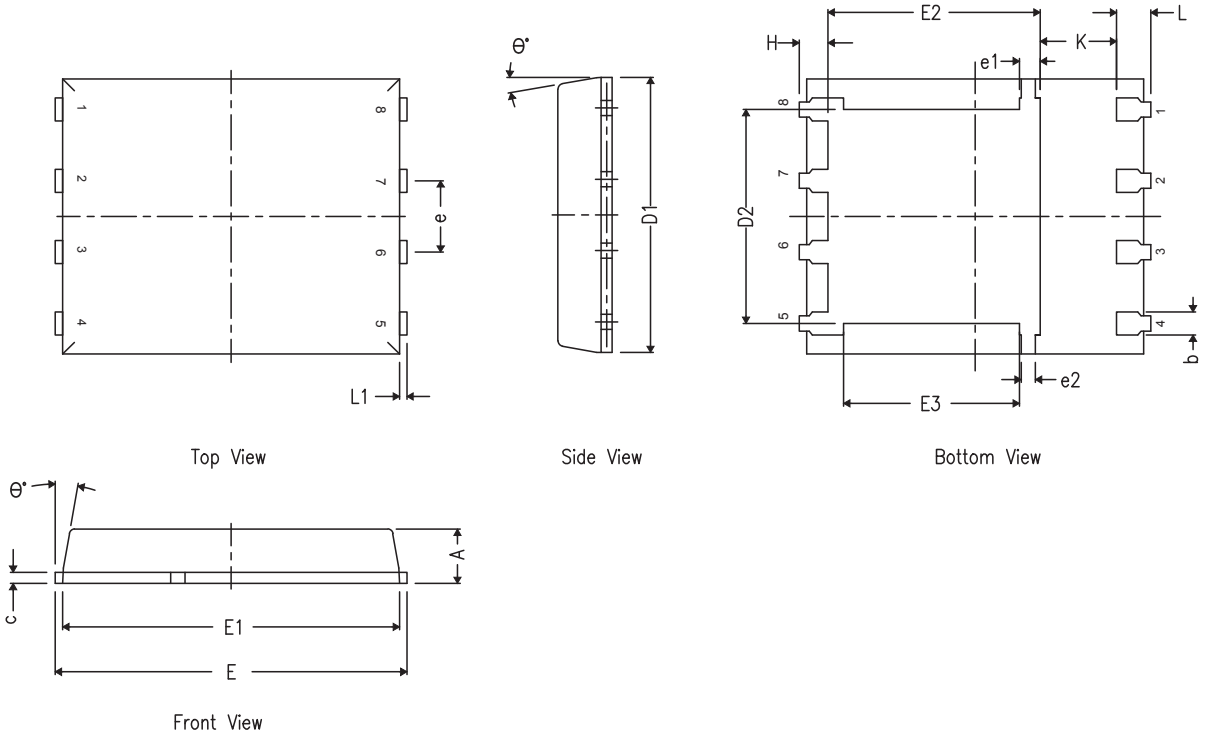
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

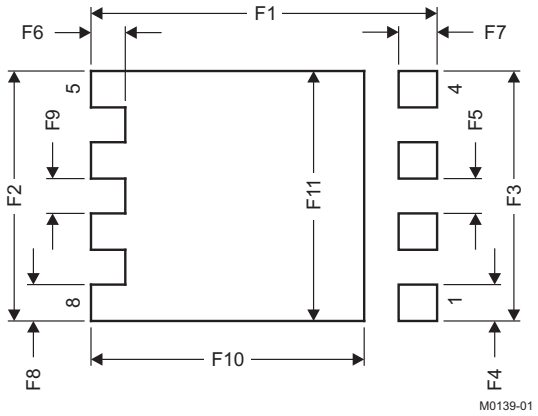
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5A Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10	–	–
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°	–	12°

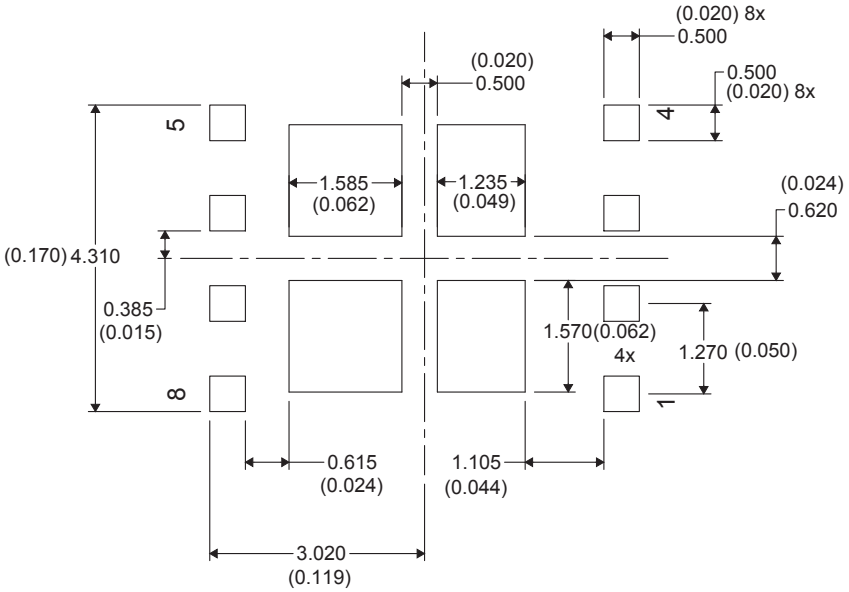
7.2 Recommended PCB Pattern



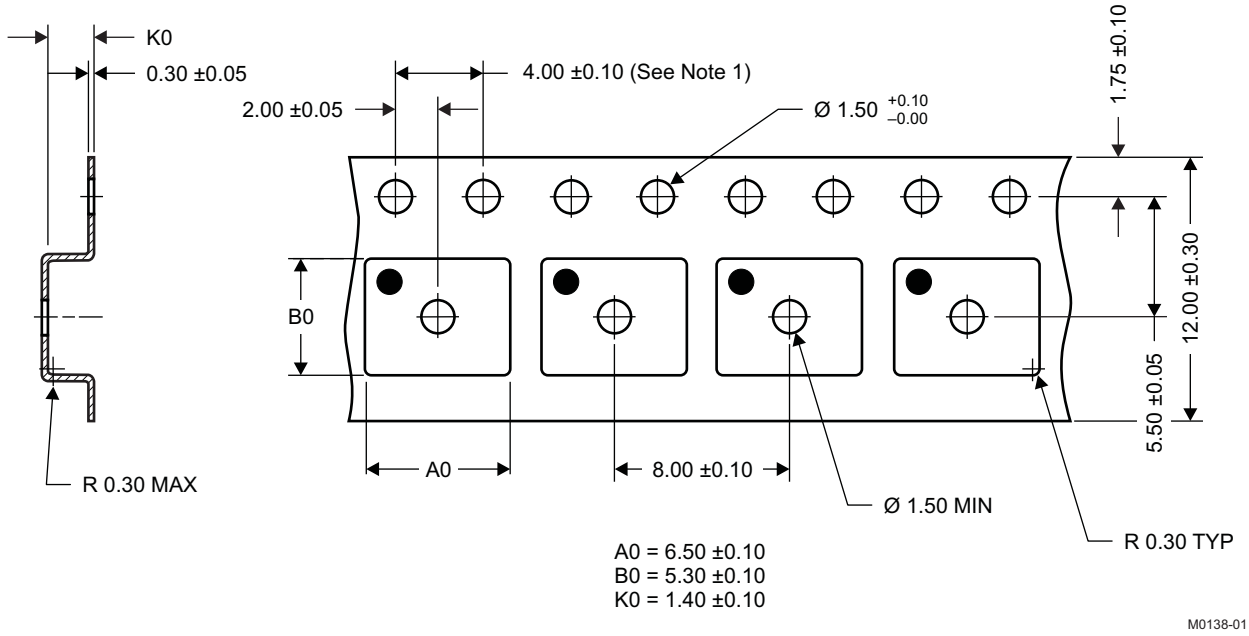
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



7.4 Q5A Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18501Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18501	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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