# Multimode (LVD/SE) SCSI 9 Line Terminator

## FEATURES

- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Built-in SPI-3 Mode Change Filter/ Delay
- Meets SCSI-1, SCSI-2, Ultra2 (SPI-2 LVD), Ultra3/Ultra160 (SPI-3) and Ultra320 (SPI-4) Standards
- Supports Active Negation
- 3pF Channel Capacitance

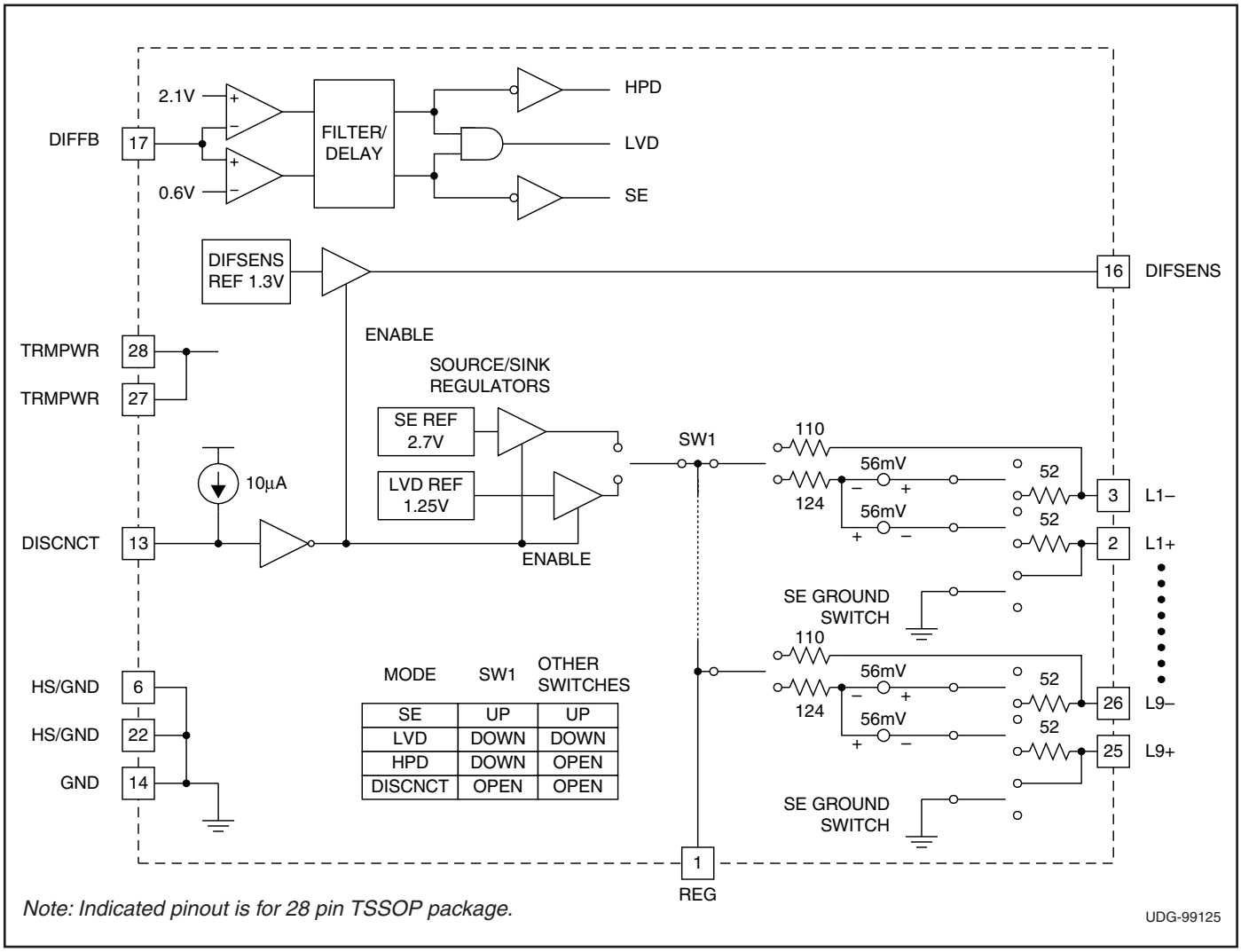
## DESCRIPTION

The UCC5672 Multi-Mode Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-3). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets.

The automatic mode select/change feature switches the terminator between Single Ended or LVD SCSI Termination, depending on the bus mode. If the bus is in High Voltage Differential Mode, the terminator lines transition into a High Impedance state.

The UCC5672 is SPI-4, SPI-3, SPI-2, and SCSI-2 compliant. This device is offered in a 28 pin TSSOP package to minimize the footprint. The UCC5672 is also available in a 36 pin MWP package.

## BLOCK DIAGRAM




*Note: Indicated pinout is for 28 pin TSSOP package.*

## ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage . . . . . 6V
Signal Line Voltage . . . . . 0V to 5V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

*All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.*

## RECOMMENDED OPERATING CONDITIONS

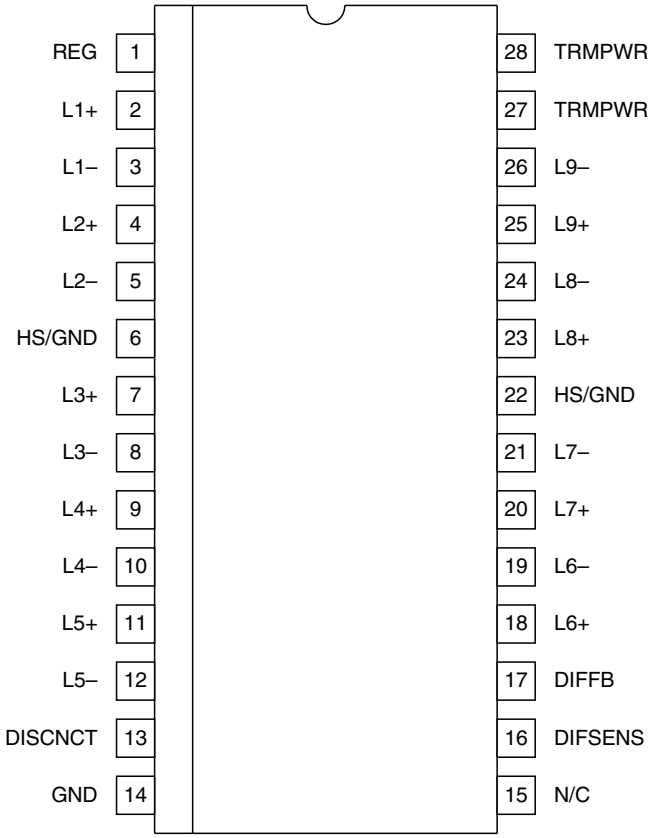
TRMPWR Voltage . . . . . 2.7V to 5.25V

## AVAILABLE OPTIONS

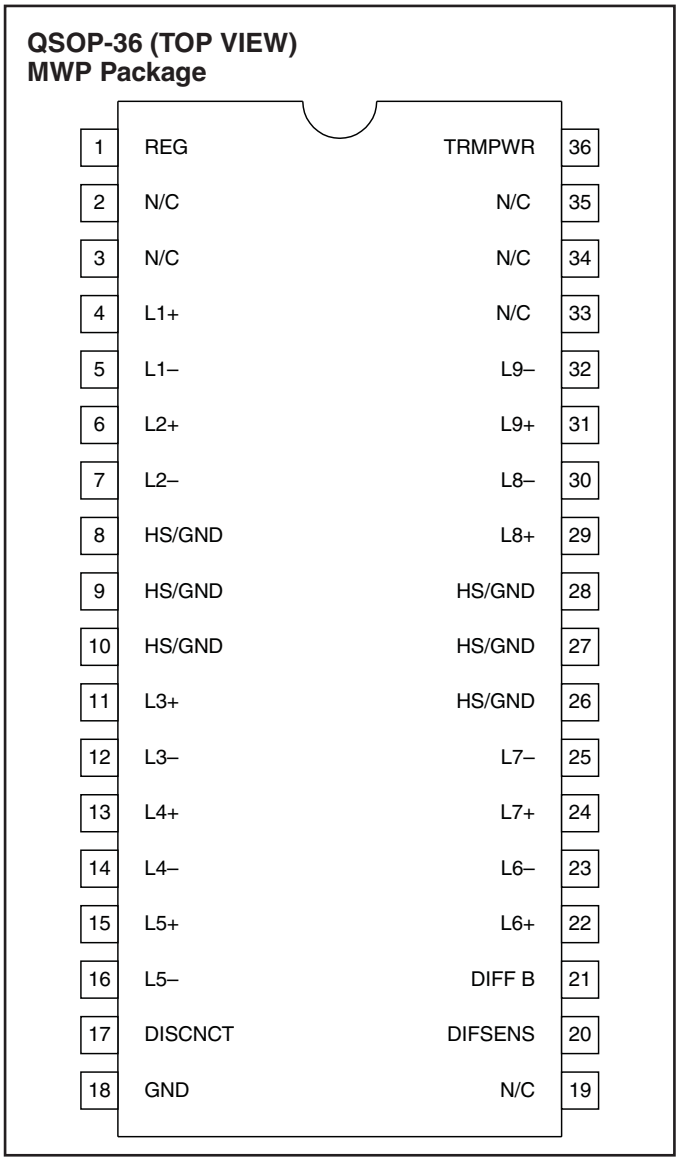
| $T_A$ | Packaged Devices |
|---|---|
| 0°C to 70°C | UCC5672MWP |
| | UCC5672PWP |

## CONNECTION DIAGRAM

**TSSOP-28 (TOP VIEW)**
**PWP Package**




**QSOP-36 (TOP VIEW)**
**MWP Package**



**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 2.7V to 5.25V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **TRMPWR Supply Current Section** | | | | | |
| TRMPWR Supply Current | LVD SCSI Mode | | 23 | 35 | mA |
| | SE Mode | | 14 | 25 | mA |
| | DISCNCT Mode | | 250 | 500 | µA |
| **Regulator Section** | | | | | |
| 1.25V Regulator Output Voltage | LVD SCSI Mode | 1.15 | 1.25 | 1.35 | V |
| 1.25V Regulator Source Current | $V_{REG}$= 0V | –225 | –420 | –800 | mA |
| 1.25V Regulator Sink Current | $V_{REG}$= 3.3V | 100 | 180 | 420 | mA |
| 2.7V Regulator Output Voltage | SE Mode | 2.5 | 2.7 | 3.0 | V |
| 2.7V Regulator Source Current | $V_{REG}$= 0V | –225 | –420 | –800 | mA |
| 2.7V Regulator Sink Current | $V_{REG}$= 3.3V | 100 | 180 | 420 | mA |
| **Diff Sense Driver (DIFSENS) Section** | | | | | |
| 1.3V DIFSENS Output Voltage | DIFSENS | 1.2 | 1.3 | 1.4 | V |
| 1.3V DIFSENS Source Current | $V_{DIFSENS}$ = 0V | –5 | | –15 | mA |
| 1.3V DIFSENS Sink Current | $V_{DIFSENS}$ = 2.75V | 50 | | 200 | µA |
| **Differential Termination Section** | | | | | |
| Differential Impedance | | 100 | 105 | 110 | Ω |
| Common Mode Impedance | (Note 2) | 110 | 150 | 165 | Ω |
| Differential Bias Voltage | | 100 | | 125 | mV |
| Common Mode Bias | | 1.15 | 1.25 | 1.35 | V |
| Output Capacitance | Single Ended Measurement to Ground (Note 1) | | | 3 | pF |
| **Single Ended Termination Section** | | | | | |
| Impedance | $Z = (VL_X - 0.2V) / IL_X$, (Note 3) | 100 | 108 | 116 | Ω |
| Termination Current | Signal Level 0.2V, All Lines Low | –20 | –23 | –25.4 | mA |
| | Signal Level 0.5V | –17 | | –22.4 | mA |
| Output Leakage | | | | 400 | nA |
| Output Capacitance | Single Ended Measurement to Ground (Note 1) | | | 3 | pF |
| Single Ended GND SE Impedance | I= 10mA | | 20 | 60 | Ω |
| **Disconnect (DISCNCT) and Diff Buffer (DIFFB) Input Section** | | | | | |
| DISCNCT Threshold | | 0.8 | | 2.0 | V |
| DISCNCT Input Current | | | –10 | –30 | µA |
| DIFFB SE to LVD SCSI Threshold | | 0.5 | | 0.7 | V |
| DIFFB LVD SCSI to HPD Threshold | | 1.9 | | 2.4 | V |
| DIFFB Input Current | | –1 | | 1 | µA |

**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 2.7V to 5.25V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Time Delay/Filter Section** | | | | | |
| Mode Change Delay | A new mode change can start any time after a previous mode change has been detected. (Note4 ) | 100 | 180 | 300 | ms |

***Note 1:*** *Guaranteed by design. Not 100% tested in production.*

***Note 2:*** $Z_{CM} = \frac{1.2V}{I_{(V_{CM}+0.6V)} - I_{(V_{CM}-0.6V)}}$*; Where VCM = Voltage measured with L+ tied to L– and zero current applied;*

***Note 3:*** *$VL_X$= Output voltage for each terminator minus output pin (L1– through L9–) with each pin unloaded.*
*$IL_X$ = Output current for each terminator minus output pin (L1– through L9–) with the minus output pin forced to 0.2V.*

***Note 4:*** *Noise on DIFFB will not cause a false mode change. The time delay is that same for a change from any mode to any other mode. Within 300ms after power is applied the mode is defined by the voltage of DIFFB.*

## PIN DESCRIPTIONS

**DIFFB:** Input pin for the comparators that select SE, LVD SCSI, or HIPD modes of operation. This pin should be decoupled with a 0.1µF capacitor to ground and then coupled to the DIFSENS pin through a 20kΩ resistor.

**DIFSENS:** Connects to the Diff Sense line of the SCSI bus. The bus mode is controlled by the voltage level on this pin.

**DISCNCT:** Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connect this pin to ground to activate the terminator or open pin to disable the terminator.

**HS/GND:** Heat sink ground pins. These should be connected to large ground area PC board traces to increase the power dissipation capability.

**GND:** Power Supply return.

**L1– thru L9–:** Termination lines. These are the active lines in SE mode and are the negative lines for LVD SCSI mode. In HIPD mode, these lines are high impedance.

**L1+ thru L9+:** Termination lines. These lines switch to ground in SE mode and are the positive lines for LVD SCSI mode. In HIPD mode, these lines are high impedance.

**REG:** Regulator bypass pin, must be connected to a 4.7µF capacitor to ground.

**TRMPWR:** 2.7V to 5.25V power input pin. Bypass near the terminators with a 4.7µF capacitor to ground.

## APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus.

The UCC5672 is used in multi-mode active termination applications, where single ended (SE) and low voltage differential (LVD) SCSI devices might coexist. The UCC5672 has both SE and LVD SCSI termination networks integrated into a single monolithic component. The correct termination network is automatically determined by the SCSI bus "DIFSENS" signal.

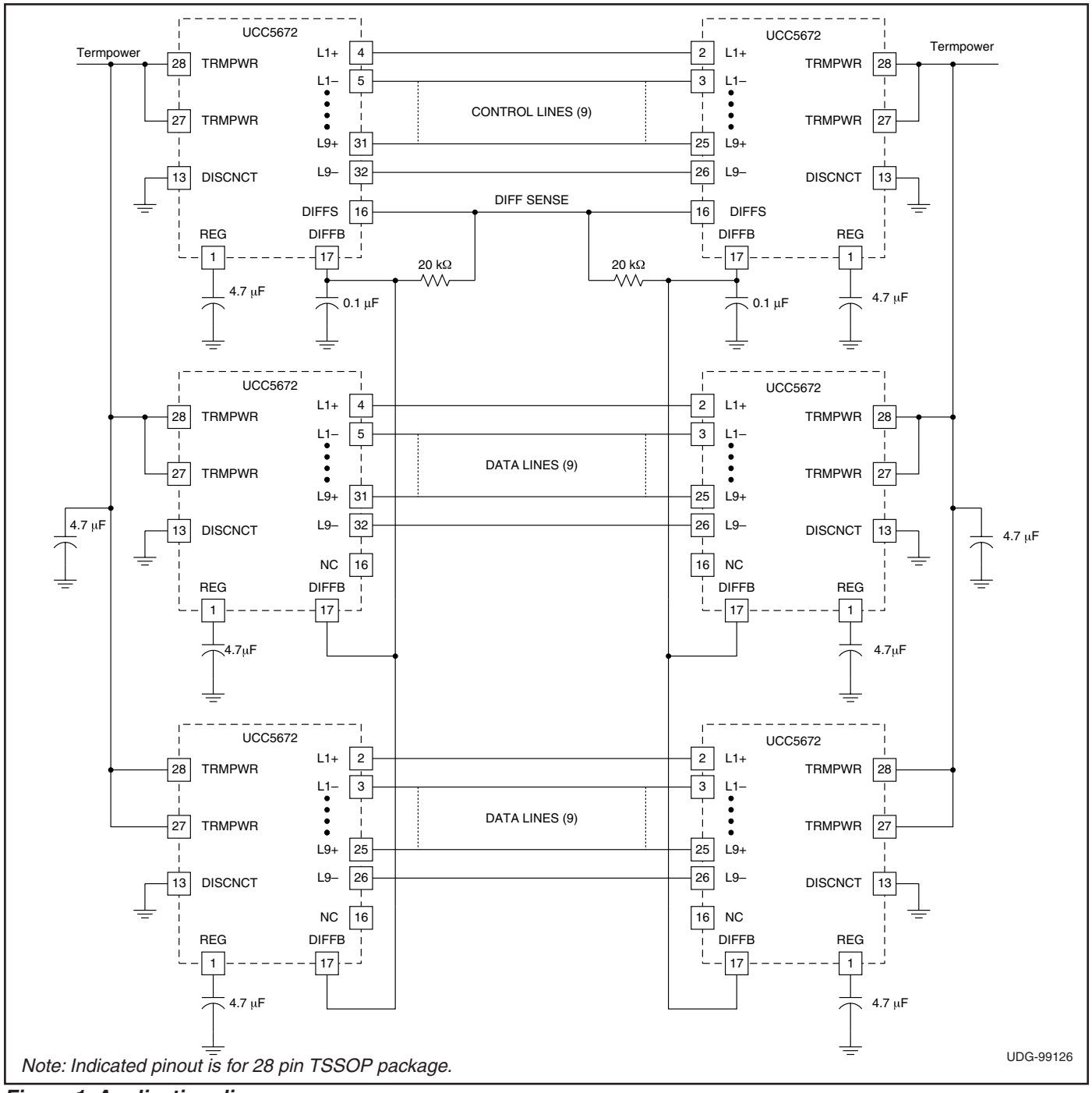
The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5672 DIFSENS drivers will try to deliver 1.3V to the DIFSENS line. If only LVD SCSI devices are present, the DIFSENS line will be successfully driven to 1.3V and the terminators will configure for LVD SCSI operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5672(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) SCSI devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

The DIFSENS line is monitored by each terminator through a 50Hz noise filter at the DIFFB input pin. A set of comparators detect and select the appropriate termi-

## APPLICATION INFORMATION (cont.)

nation for the bus as follows. If the DIFSENS signal is below 0.5V, the termination network is set for single ended. Between 0.7V and 1.9V, the termination network switches to LVD SCSI, and above 2.4V indicates HVD SCSI, causing the terminators to disconnect from the bus. These thresholds accommodate differences in ground potential that can occur with long lines.

Three UCC5672 multi-mode parts are required at each end of the bus to terminate 27 (18 data, plus 9 control) lines. Each part includes a DIFSENS driver, but only one is necessary to drive the line. The DIFFB inputs on all three parts are connected together, allowing them to share the same 50Hz noise filter. This multi-mode terminator operates in full specification down to 2.7V TRMPWR voltage. This accommodates 3.3V systems,




*Note: Indicated pinout is for 28 pin TSSOP package.*

***Figure 1. Application diagram.***

## APPLICATION INFORMATION (cont.)

with allowance for the 3.3V supply tolerance (+/- 10%), a unidirectional fusing device and cable drop. In 3.3V TRMPWR systems, the UCC3918 is recommended in place of the fuse and diode. The UCC3918's lower voltage drop allows additional margin over the fuse and diode, for the far end terminator.

Layout is critical for Ultra2, Ultra3/Ultra160 and Ultra320 systems. The SPI-2 standard for capacitance loading is 10pF maximum from each positive and negative signal line to ground, and a maximum of 5pF between the positive and negative signal lines of each pair is allowed. These maximum capacitances apply to differential bus termination circuitry that is not part of a SCSI device, (e.g. a cable terminator). If the termination circuitry is included as part of a SCSI device, (e.g., a host adaptor, disk or tape drive), then the corresponding requirements are 30pF maximum from each positive and negative signal line to ground and 15pF maximum between the positive and negative signal lines of each pair.

The SPI-2 standard for capacitance balance of each pair and balance between pairs is more stringent. The standard is 0.75pF maximum difference from the positive and negative signal lines of each pair to ground. An additional requirement is a maximum difference of 2pF when comparing pair to pair. These requirements apply to differential bus termination circuitry that is not part of a SCSI device. If the termination circuitry is included as part of a device, then the corresponding balance requirements are 2.25pF maximum difference within a pair, and 3pF from pair to pair.

Feed-throughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multi-layer power and ground plane spacing add about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes will reduce the capacitance. Similarly, opening up the power and ground planes under the connector will reduce the capacitance for through-hole connector applications. Capacitance will also be affected by components, in close proximity, above and below the circuit board.

Unitrode multi-mode terminators are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed to not effect the capacitive balance of the bus when the device is in LVD SCSI or disconnect mode.

Multi-layer boards need to adhere to the 120Ω impedance standard, including the connectors and feed-throughs. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between runs within a pair, and a minimum of 8 mil spacing to the adjacent pairs to reduce crosstalk. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems. Careful consideration must be given to the issue of heat management. A multi-mode terminator, operating in SE mode, will dissipate as much as 130mW of instantaneous power per active line with TRMPWR = 5.25V. The UCC5672 is offered in a 28 pin TSSOP. This package includes two heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. Both of the HS/GND pins need to be connected to etch area or four feed-through per pin connecting to the ground plane layer on a multi-layer board.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC5672PWP | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | UCC5672PWP | Samples |
| UCC5672PWPTR | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | UCC5672PWP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

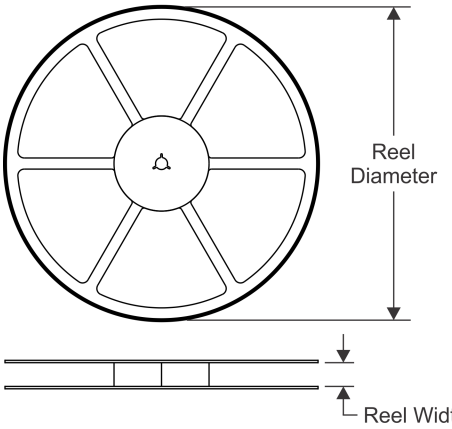
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

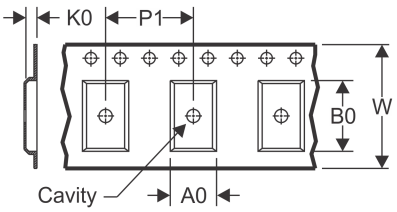
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

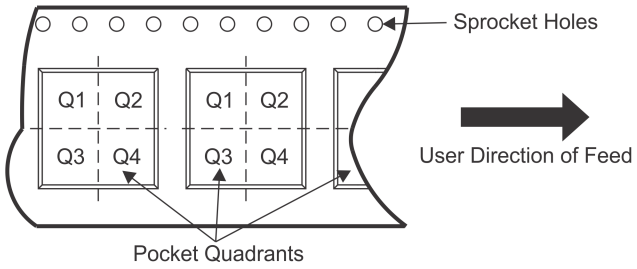



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

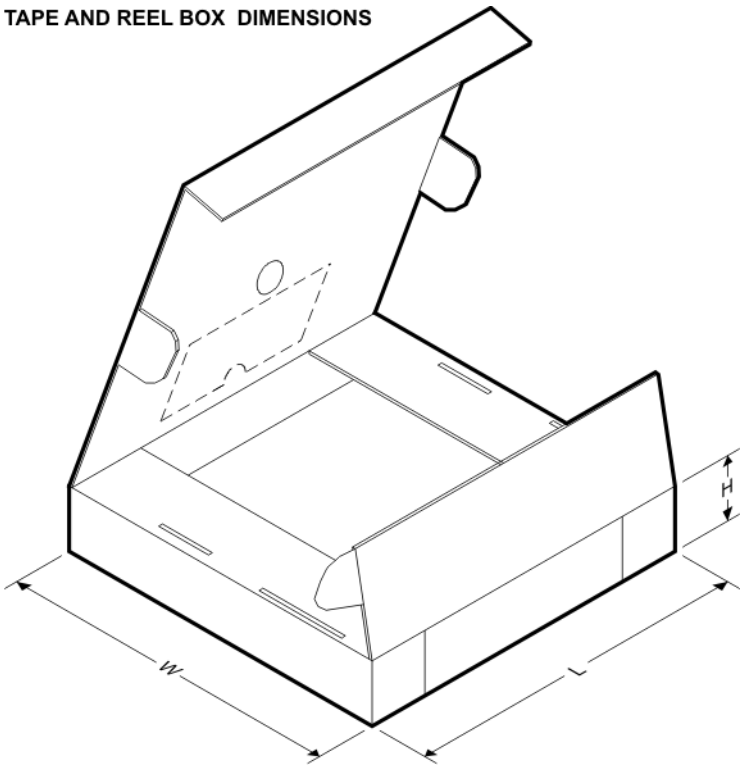
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC5672PWPTR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

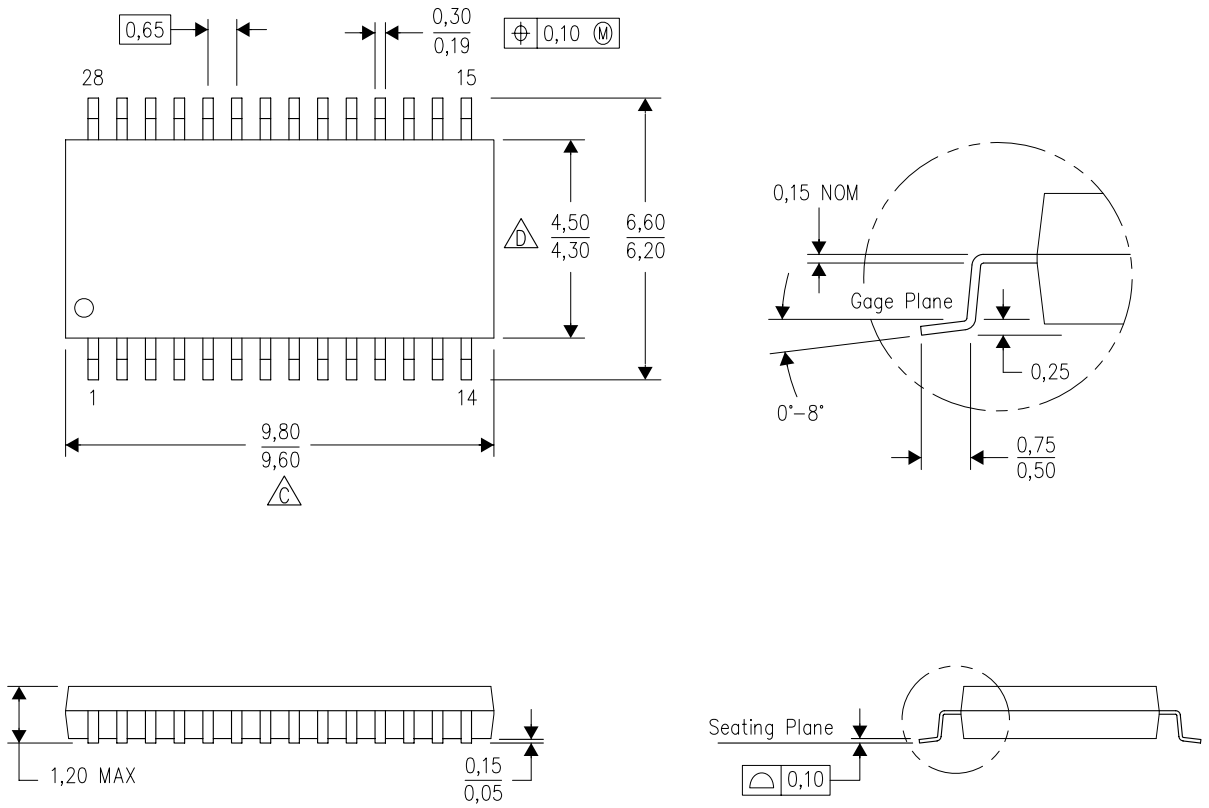
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC5672PWPTR | TSSOP | PW | 28 | 2000 | 367.0 | 367.0 | 38.0 |

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE

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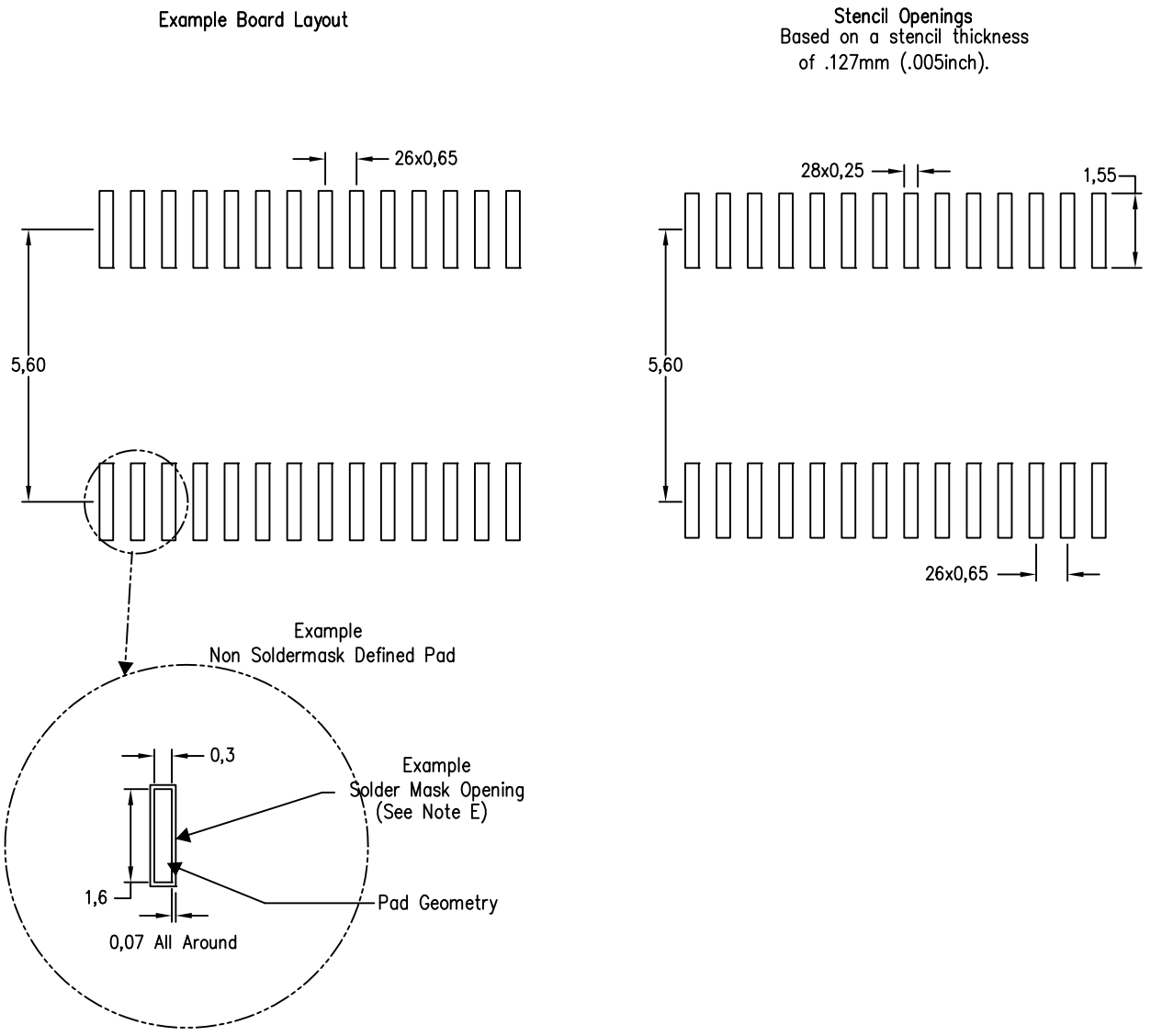
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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