TEXAS INSTRUMENTS

**DRV8880**

SLVSD18C – JUNE 2015 – REVISED AUGUST 2017

# DRV8880 2-A Stepper Motor Driver With Smart Tune

## 1 Features

- Microstepping Stepper Motor Driver
  - STEP/DIR Interface
  - Up to 1/16 Microstepping Indexer
  - Non-Circular and Standard ½ Step Modes
- 6.5- to 45-V Operating Supply Voltage Range
- Multiple Decay Modes to Support Any Motor
  - Smart tune
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Adaptive Blanking Time for Smooth Stepping
- Configurable Off-Time PWM Chopping
  - 10-, 20-, or 30-μs Off-Time
- 3.3-V, 10-mA LDO Regulator
- Low-Current Sleep Mode (28 μA)
- Small Package and Footprint
  - 28 HTSSOP (PowerPAD™)
  - 28 WQFN
- **Protection Features**
  - VM Undervoltage Lockout (UVLO2)
  - Logic Undervoltage (UVLO1)
  - Charge Pump Undervoltage (CPUV)
  - Overcurrent Protection (OCP)
    - Latched OCP Mode
    - Retry OCP Mode
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)

## 2 Applications

- Automatic Teller and Money Handling Machines
- Video Security Cameras
- Multi-Function Printers and Document Scanners
- 3D Printers
- Office Automation Machines
- Factory Automation and Robotics

## 3 Description

The DRV8880 is a bipolar stepper motor driver for industrial applications. The device has two N-channel power MOSFET H-bridge drivers and a microstepping indexer. The DRV8880 is capable of driving 2.0 A full-scale current or 1.4-A rms current (with proper PCB ground plane for thermal dissipation and at 24 V and $T_A = 25°C$).

Smart tune automatically tunes stepper motors for optimal current regulation performance and compensates for motor variation and aging effects. Additionally slow, fast, and mixed decay modes are available.

The STEP/DIR pins provide a simple control interface. The device can be configured in full-step up to 1/16- step modes. A low-power sleep mode is provided for very low quiescent current standby using a dedicated nSLEEP pin.
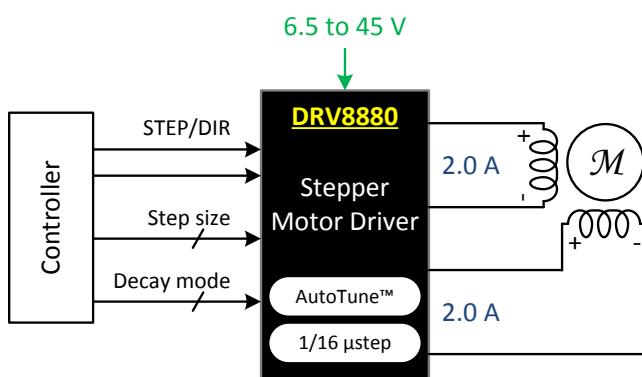
Internal protection functions are provided for undervoltage, charge pump faults, overcurrent, short-circuits, and overtemperature. Fault conditions are indicated by a nFAULT pin.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| DRV8880 | HTSSOP (28) | 9.70 mm × 4.40 mm |
| | WQFN (28) | 5.50 mm × 3.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

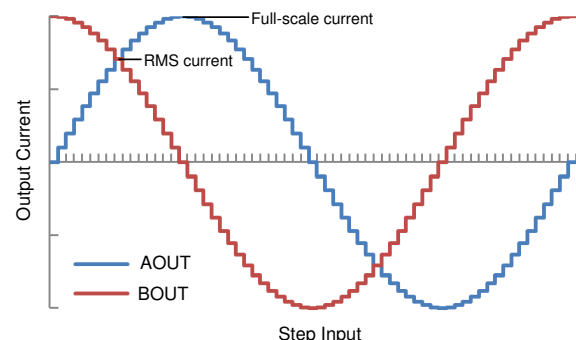**Simplified System Diagram**
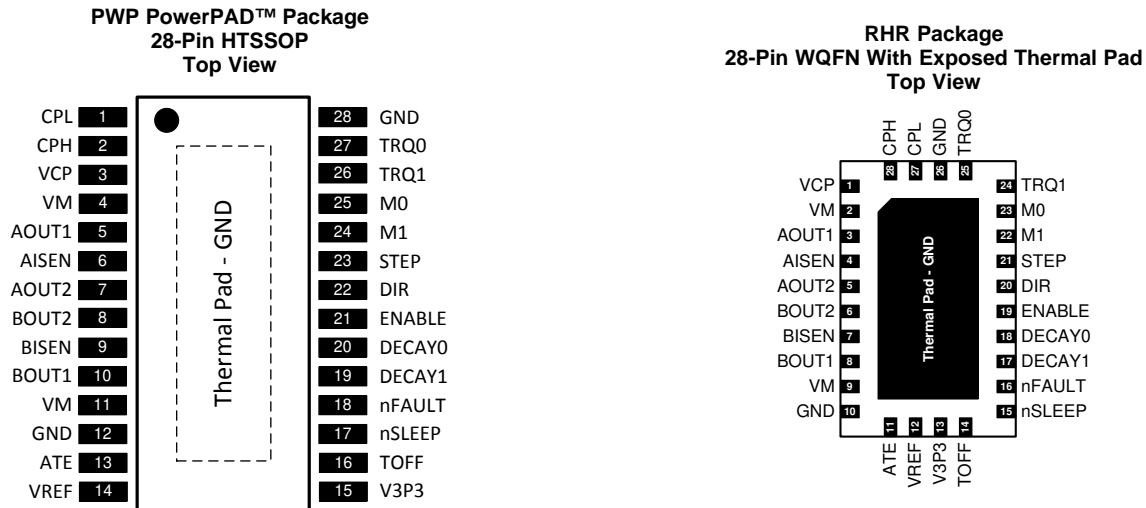


**Microstepping Current Waveform**

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# 4  Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (August 2017) to Revision C**  **Page**

- Changed the maximum value for VREF from V3P3 + 0.5 V to 4.1 V in the *Absolute Maximum Ratings* table .................... 5

**Changes from Revision A (July 2015) to Revision B**  **Page**

- Added the *Power Supplies and Input Pins* section .......................................................................................................... 27
- Added the *Receiving Notification of Documentation Updates* section ................................................................................. 37

**Changes from Original (June 2015) to Revision A**  **Page**

- Updated device status to production data ........................................................................................................................ 1
- Updated from "PowerPAD" to "thermal pad" .................................................................................................................... 4

# 5 Pin Configuration and Functions

**PWP PowerPAD™ Package**
**28-Pin HTSSOP**
**Top View**



**RHR Package**
**28-Pin WQFN With Exposed Thermal Pad**
**Top View**



**Pin Functions**

| PIN | | | TYPE | | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | PWP | RHR | | | |
| CPL | 1 | 27 | PWR | Charge pump switching pins | Connect a VM rated, 0.1-µF ceramic capacitor between CPH and CPL |
| CPH | 2 | 28 | | | |
| VCP | 3 | 1 | O | Charge pump output | Connect a 16 V, 0.47 µF ceramic capacitor to VM |
| VM | 4, 11 | 2, 9 | PWR | Power supply | Connect to motor supply voltage; bypass to GND with two 0.1 µF (for each pin) plus one bulk capacitor rated for VM |
| AOUT1 | 5 | 3 | O | Winding A output | H-bridge outputs, drives one winding of a stepper motor |
| AOUT2 | 7 | 5 | | | |
| AISEN | 6 | 4 | O | Winding A sense | Requires sense resistor to GND; value sets peak current in winding A |
| BOUT2 | 8 | 6 | O | Winding B output | H-bridge outputs, drives one winding of a stepper motor |
| BOUT1 | 10 | 8 | | | |
| BISEN | 9 | 7 | O | Winding B sense | Requires sense resistor to GND; value sets peak current in winding B |
| GND | 12, 28 | 10, 26 | PWR | Device ground | Must be connected to ground |
| ATE | 13 | 11 | I | Smart tune enable pin | Logic high enables smart tune operation; when logic low, the decay mode is set through the DECAYx pins; smart tune must be pulled high prior to power-up or coming out of sleep, or else tied to V3P3 in order to enable smart tune; internal pulldown; see *Smart Tune* |
| VREF | 14 | 12 | I | Full scale current reference input | Voltage on this pin sets the full scale chopping current. |
| V3P3 | 15 | 13 | PWR | Internal regulator | Internal supply voltage; bypass to GND with a 6.3 V, 0.47 µF ceramic capacitor; up to 10 mA external load |
| TOFF | 16 | 14 | I | Decay mode off time set | Sets the off-time during current chopping; tri-level pin |
| nSLEEP | 17 | 15 | I | Sleep mode input | Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown |
| nFAULT | 18 | 16 | O | Fault indication pin | Pulled logic low with fault condition; open-drain output requires an external pullup |
| DECAY1 | 19 | 17 | I | Decay mode setting pins | Sets the decay mode; see description section; tri-level pin |
| DECAY0 | 20 | 18 | | | |
| ENABLE | 21 | 19 | I | Enable driver input | Logic high to enable device outputs and internal indexer; logic low to disable; internal pulldown |
| DIR | 22 | 20 | I | Direction input | Logic level sets the direction of stepping; internal pulldown |

Product Folder Links: *DRV8880*

## Pin Functions (continued)

| PIN | | | TYPE | DESCRIPTION | |
|---|---|---|---|---|---|
| NAME | PWP | RHR | | | |
| STEP | 23 | 21 | I | Step input | A rising edge causes the indexer to advance one step; internal pulldown |
| M1 | 24 | 22 | I | Microstepping mode setting pins | Sets the step mode; full, 1/2, 1/4, 1/8, 1/16; tri-level pin |
| M0 | 25 | 23 | | | |
| TRQ1 | 26 | 24 | I | Torque DAC current scalar | Scales the current by 100%, 75%, 50%, or 25%; internal pulldown |
| TRQ0 | 27 | 25 | | | |
| PAD | PAD | PAD | PWR | Thermal pad | Must be connected to ground |

Product Folder Links: *DRV8880*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) [1]

|  | MIN | MAX | UNIT |
|---|---|---|---|
| Power supply voltage (VM) | −0.3 | 50 | V |
| Power supply voltage ramp rate (VM) | 0 | 2 | V/µs |
| Charge pump voltage (VCP, CPH) | −0.3 | VM + 12 | V |
| Charge pump negative switching pin (CPL) | −0.3 | VM | V |
| Internal regulator voltage (V3P3) | −0.3 | 3.8 | V |
| Internal regulator current output (V3P3) | 0 | 10 | mA |
| Control pin voltage (STEP, DIR, ENABLE, nSLEEP, nFAULT, M0, M1, DECAY0, DECAY1, TRQ0, TRQ1, ATE) | −0.3 | 7.0 | V |
| Open drain output current (nFAULT) | 0 | 10 | mA |
| Reference input pin voltage (VREF) | −0.3 | 4.1 | V |
| Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2) | −0.7 | VM + 0.7 | V |
| Continuous shunt amplifier input pin voltage (AISEN, BISEN) [2] | −0.55 | 0.55 | V |
| Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN) | Internally limited | | A |
| Operating junction temperature, $T_J$ | −40 | 150 | °C |
| Storage temperature, $T_{stg}$ | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | ±4000 | V |
|  |  | Charged-device model (CDM), per JEDEC specification JESD22-C101 [2] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| VM | Power supply voltage range | 6.5 [1] | 45 | V |
| $V_{IN}$ | Digital pin voltage range | 0 | 5.3 | V |
| VREF | Reference rms voltage range | 0.3 [2] | V3P3 | V |
| $f_{PWM}$ | Applied STEP signal | 0 | 100 [3] | kHz |
| $I_{V3P3}$ | V3P3 external load current | 0 | 10 [4] | mA |
| $I_{FS}$ | Motor full scale current | 0 | 2.0 | A |
| $I_{rms}$ | Motor rms current | 0 | 1.4 | A |
| $T_A$ | Operating ambient temperature | −40 | 125 | °C |

(1) Internal logic and indexer remain active down to $V_{UVLO2}$ (4.9 V maximum) even though the output H-bridges are disabled
(2) Operational at VREF ≈ 0 to 0.3 V, but accuracy is degraded
(3) STEP input can operate up to 1 MHz, but system bandwidth is limited by the motor load
(4) Power dissipation and thermal limits must be observed

## 6.4 Thermal Information

| THERMAL METRIC [1] | | DRV8880 | | UNIT |
|---|---|---|---|---|
| | | PWP (HTSSOP) | RHR (WQFN) | |
| | | 28 PINS | 28 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 33.1 | 37.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 16.6 | 23.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 14.4 | 8.0 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 14.2 | 7.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.3 | 1.7 | °C/W |

(1)  For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES (VM, V3P3)** | | | | | | |
| VM | VM operating voltage | | 6.5 | | 45 | V |
| $I_{VM}$ | VM operating supply current | nSLEEP high; ENABLE high; no motor load; VM = 24 V | | 8 | 18 | mA |
| $I_{VMQ}$ | VM sleep mode supply current | nSLEEP low; VM = 24 V; $T_A$ = 25°C | | 28 | | µA |
| | | nSLEEP low; VM = 24 V; $T_A$ = 125°C [1] | | | 77 | |
| $t_{SLEEP}$ | Sleep time | nSLEEP low to sleep mode | | | 100 | µs |
| $t_{WAKE}$ | Wake-up time | nSLEEP high to output transition | | | 1.5 | ms |
| $t_{ON}$ | Turn-on time | VM > $V_{UVLO2}$ to output transition | | | 1.5 | ms |
| V3P3 | LDO regulator voltage | External load 0 to 10 mA | 2.9 | 3.3 | 3.6 | V |
| **CHARGE PUMP (VCP, CPH, CPL)** | | | | | | |
| $V_{CP}$ | VCP operating voltage | VM > 12 V | | VM + 11.5 | | V |
| | | $V_{UVLO2}$ < VM < 12 V | | 2×VM − 1.5 | | |
| $f_{VCP}$ [1] | Charge pump switching frequency | VM > $V_{UVLO2}$ | 175 | | 715 | kHz |
| **LOGIC-LEVEL INPUTS (STEP, DIR, ENABLE, nSLEEP, TRQ0, TRQ1, ATE)** | | | | | | |
| $V_{IL}$ | Input logic low voltage | | 0 | | 0.6 | V |
| $V_{IH}$ | Input logic high voltage | | 1.6 | | 5.3 | V |
| $V_{HYS}$ | Input logic hysteresis | | 100 | | | mV |
| $I_{IL}$ | Input logic low current | $V_{IN}$ = 0 V | −1 | | 1 | µA |
| $I_{IH}$ | Input logic high current | $V_{IN}$ = 5.0 V | | 50 | 100 | µA |
| $R_{PD}$ | Pulldown resistance | Measured between the pin and GND | | 100 | | kΩ |
| $t_{PD}$ | Propagation delay | STEP input to current change | | 450 | | ns |
| **TRI-LEVEL INPUTS (M0, M1, DECAY0, DECAY1, TOFF)** | | | | | | |
| $V_{IL}$ | Tri-level input logic low voltage | | 0 | | 0.6 | V |
| $V_{IZ}$ | Tri-level input Hi-Z voltage | | | 1.1 | | V |
| $V_{IH}$ | Tri-level input logic high voltage | | 1.6 | | 5.3 | V |
| $V_{HYS}$ | Tri-level input hysteresis | | 100 | | | mV |
| $I_{IL}$ | Tri-level input logic low current | $V_{IN}$ = 0 V | −55 | | −35 | µA |
| $I_{IZ}$ | Tri-level input Hi-Z current | $V_{IN}$ = 1.3 V | | 15 | | µA |
| $I_{IH}$ | Tri-level input logic high current | $V_{IN}$ = 3.3 V | | 85 | | µA |
| $R_{PD}$ | Tri-level pulldown resistance | Measured between the pin and GND | | 40 | | kΩ |
| $R_{PU}$ | Tri-level pullup resistance | Measured between V3P3 and the pin | | 45 | | kΩ |

(1)  Specified by design and characterization data

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CONTROL OUTPUTS (nFAULT)** | | | | | | |
| $V_{OL}$ | Output logic low voltage | $I_O$ = 4 mA | | | 0.5 | V |
| $I_{OH}$ | Output logic high leakage | External pullup resistor to 3.3 V | −1 | | 1 | µA |
| **MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)** | | | | | | |
| $R_{DS(ON)}$ | High-side FET on resistance | VM = 24 V, I = 1 A, $T_A$ = 25°C | | 330 | | mΩ |
| | | VM = 24 V, I = 1 A, $T_A$ = 125°C [(1)] | | 400 | 440 | |
| | | VM = 6.5 V, I = 1 A, $T_A$ = 25°C | | 430 | | |
| | | VM = 6.5 V, I = 1 A, $T_A$ = 125°C [(1)] | | 500 | 560 | |
| $R_{DS(ON)}$ | Low-side FET on resistance | VM = 24 V, I = 1 A, $T_A$ = 25°C | | 300 | | mΩ |
| | | VM = 24 V, I = 1 A, $T_A$ = 125°C [(1)] | | 370 | 400 | |
| | | VM = 6.5 V, I = 1 A, $T_A$ = 25°C | | 370 | | |
| | | VM = 6.5 V, I = 1 A, $T_A$ = 125°C [(1)] | | 450 | 490 | |
| $t_{RISE}$ | Output rise time | VM = 24 V, 50 Ω load from xOUTx to GND | | 70 | | ns |
| $t_{FALL}$ | Output fall time | VM = 24 V, 50 Ω load from VM to xOUTx | | 70 | | ns |
| $t_{DEAD}$ | Output dead time [(2)] | | | 200 | | ns |
| $V_d$ | Body diode forward voltage | $I_{OUT}$ = 0.5 A | | 0.7 | 1 | V |
| **PWM CURRENT CONTROL (VREF, AISEN, BISEN)** | | | | | | |
| $V_{TRIP}$ | xISENSE trip voltage, full scale | TRQ at 100%, VREF = 3.3 V | | 500 | | mV |
| | | TRQ at 75%, VREF = 3.3 V | | 375 | | |
| | | TRQ at 50%, VREF = 3.3 V | | 250 | | |
| | | TRQ at 25%, VREF = 3.3 V | | 125 | | |
| $A_V$ | Amplifier attenuation | TRQ at 100% (TRQ0 = 0, TRQ1 = 0) | 6.25 | 6.58 | 6.91 | V/V |
| | | TRQ at 75% (TRQ0 = 1, TRQ1 = 0) | 6.2 | 6.56 | 6.92 | |
| | | TRQ at 50% (TRQ0 = 0, TRQ1 = 1) | 6.09 | 6.51 | 6.94 | |
| | | TRQ at 25% (TRQ0 = 1, TRQ1 = 1) | 5.83 | 6.38 | 6.93 | |
| $t_{OFF}$ | PWM off-time | TOFF Logic Low | | 20 | | µs |
| | | TOFF Logic High | | 30 | | |
| | | TOFF Hi-Z | | 10 | | |
| $t_{BLANK}$ | PWM blanking time | See Table 9 for details | | 1.8 | | µs |
| | | | | 1.5 | | |
| | | | | 1.2 | | |
| | | | | 0.9 | | |
| **PROTECTION CIRCUITS** | | | | | | |
| $V_{UVLO2}$ | VM undervoltage lockout | VM falling; UVLO2 report | | 5.8 | 6.4 | V |
| | | VM rising; UVLO2 recovery | | 6.1 | 6.5 | |
| $V_{UVLO1}$ | Logic undervoltage | VM falling; logic disabled | | 4.5 | 4.9 | V |
| | | VM rising; logic enabled | | 4.8 | 5 | |
| $V_{UVLO,HYS}$ | undervoltage hysteresis | Rising to falling threshold | 100 | | | mV |
| $V_{CPUV}$ | Charge pump undervoltage | VCP falling; CPUV report | | VM + 1.8 | | V |
| | | VCP rising; CPUV recovery | | VM + 1.9 | | |
| $V_{CPUV,HYS}$ | CP undervoltage hysteresis | Rising to falling threshold | 50 | | | mV |
| $I_{OCP}$ | Overcurrent protection trip level | Current through any FET | 2.5 | 3.6 | | A |
| $V_{OCP}$ | Sense pin overcurrent trip level | Voltage at AISEN or BISEN | 0.9 | 1.25 | | V |
| $t_{OCP}$ | Overcurrent deglitch time | | | 2 | | µs |

(2)   Specified by design and characterization data

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{RETRY}$ | Overcurrent retry time | | 0.5 | | 2 | ms |
| $T_{TSD}$ (2) | Thermal shutdown temperature | Die temperature $T_J$ | 150 | | | °C |
| $T_{HYS}$ (2) | Thermal shutdown hysteresis | Die temperature $T_J$ | | 35 | | °C |

## 6.6 Indexer Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $f_{STEP}$ | Step frequency | | 1 (1) | MHz |
| 2 | $t_{WH(STEP)}$ | Pulse duration, STEP high | 470 | | ns |
| 3 | $t_{WL(STEP)}$ | Pulse duration, STEP low | 470 | | ns |
| 4 | $t_{SU(DIR, Mx)}$ | Setup time, DIR or Mx to STEP rising | 200 | | ns |
| 5 | $t_{H(DIR, Mx)}$ | Hold time, DIR or Mx to STEP rising | 200 | | ns |

(1) STEP input can operate up to 1 MHz, but system bandwidth is limited by the motor load



**Figure 1. Timing Diagram**

Product Folder Links: *DRV8880*
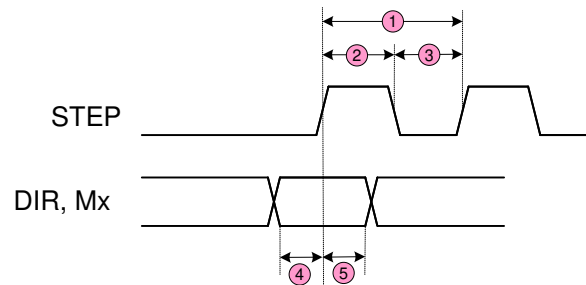
## 6.7 Typical Characteristics

Over recommended operating conditions (unless otherwise noted)
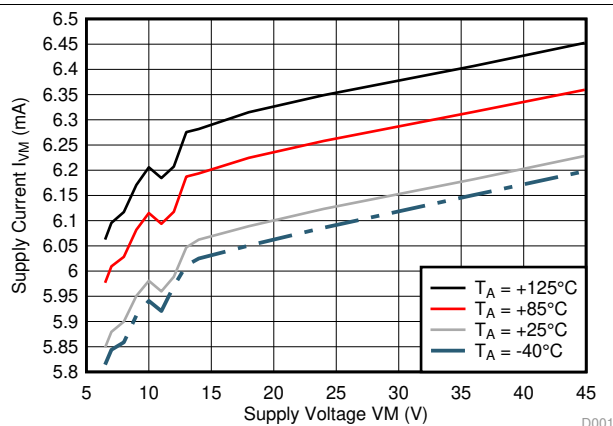


**Figure 2. Supply Current over VM**
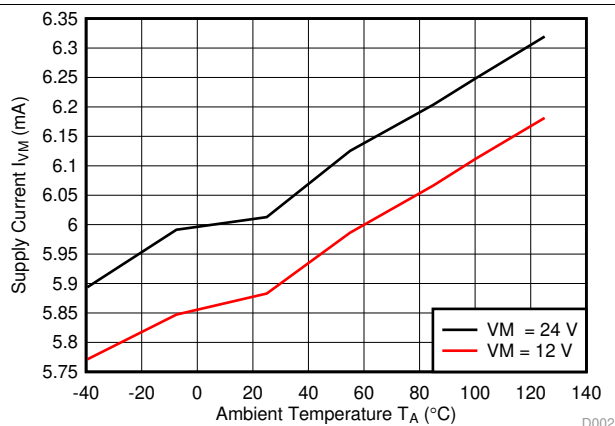


**Figure 3. Supply Current over Temperature**
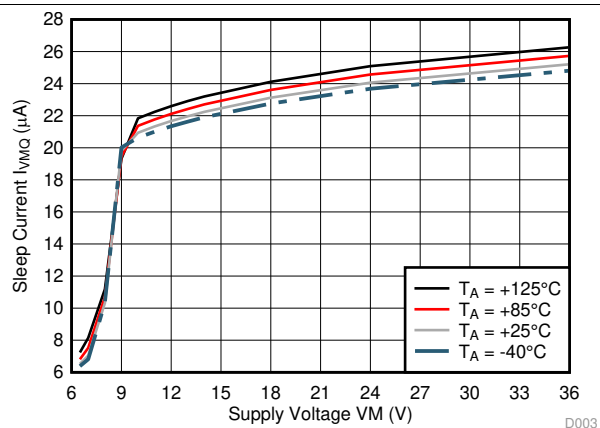


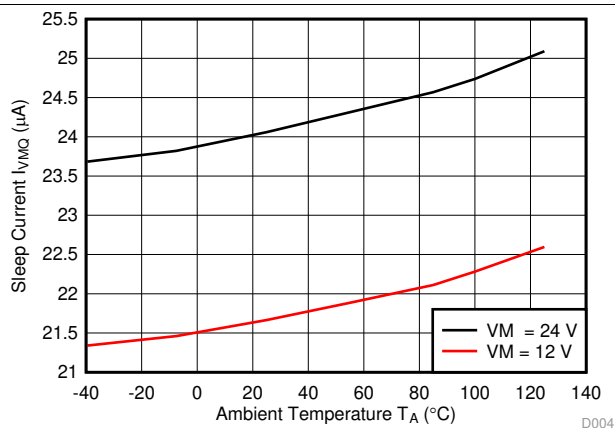**Figure 4. Sleep Current over VM**
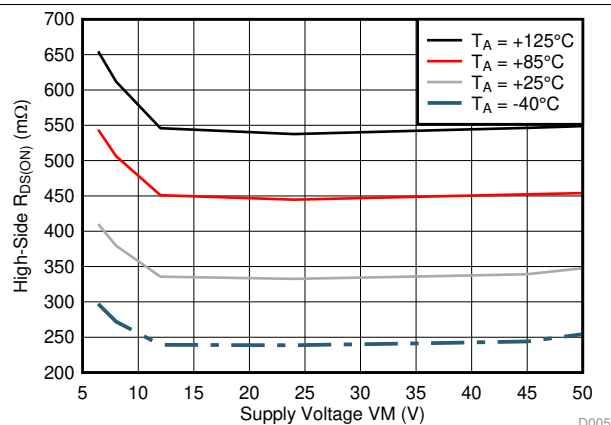


**Figure 5. Sleep Current over Temperature**
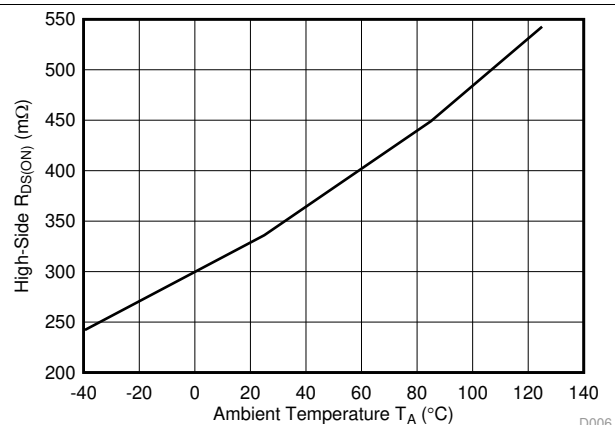


**Figure 6. High-Side R$_{DS(ON)}$ over VM**



**Figure 7. High-Side R$_{DS(ON)}$ over Temperature (VM = 12 V)**

## Typical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted)
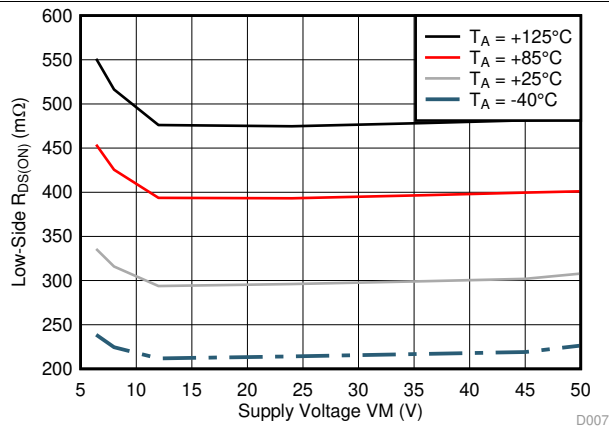


**Figure 8. Low-Side R_DS(ON) over VM**
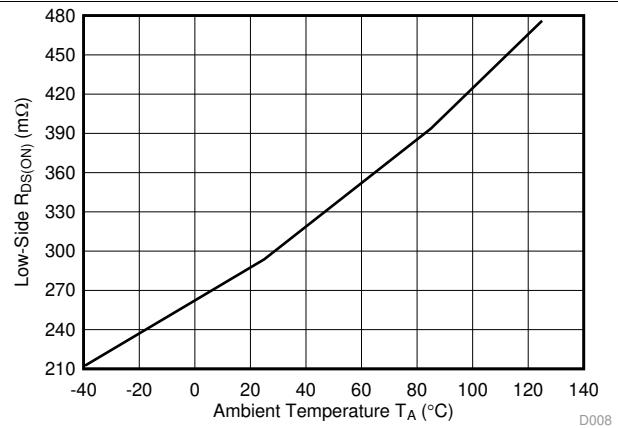

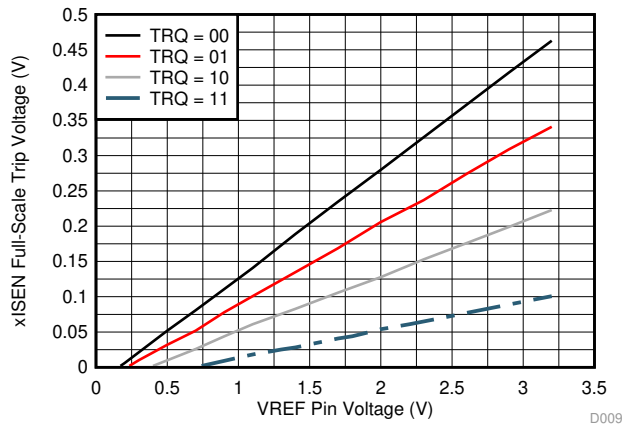
**Figure 9. Low-Side R_DS(ON) over Temperature (VM = 12 V)**



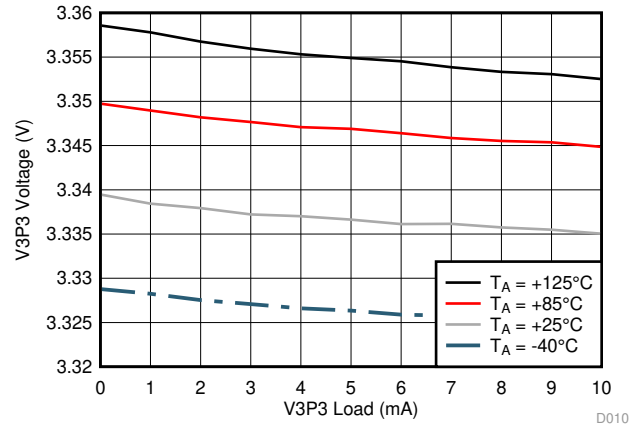**Figure 10. xISEN Full-Scale Trip Voltage over VREF Input**



**Figure 11. V3P3 Regulator over Load (VM = 24 V)**

Product Folder Links: *DRV8880*

# 7 Detailed Description

## 7.1 Overview

The DRV8880 is an integrated motor driver solution for bipolar stepper motors. The device integrates two NMOS H-bridges, current regulation circuitry, and a microstepping indexer. The DRV8880 can be powered with a supply voltage between 6.5 and 45 V, and is capable of providing an output current up to 2.5 A peak current, 2.0 A full-scale current, or 1.4 A rms current. Actual operable full-scale and rms current will depend on ambient temperature, supply voltage, and PCB ground plane size. Between VM = 6.4 V and VM = 4.9 V the H-bridge outputs are shut down, but the internal logic remains active in order to prevent missed steps.

A simple STEP/DIR interface allows easy interfacing to the controller circuit. The internal indexer is able to execute high-accuracy microstepping without requiring the processor to control the current level. The indexer is capable of full step and half step as well as microstepping to 1/4, 1/8, and 1/16. In addition to the standard half stepping mode, a non-circular 1/2-stepping mode is available for increased torque output at higher motor rpm.

The current regulation is highly configurable, with several decay modes of operation. The decay mode can be selected as a fixed slow, slow/mixed, mixed, slow/fast, or fast decay. The slow/mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. Similarly, the slow/fast decay mode uses slow decay on increasing steps and fast decay on decreasing steps.

In addition, an smart tune mode can be used which automatically adjusts the decay setting to minimize current ripple while still reacting quickly to step changes. This feature greatly simplifies stepper driver integration into a motor drive system.

The PWM off-time, $t_{OFF}$, can be adjusted to 10, 20, or 30 µs.

An adaptive blanking time feature automatically scales the minimum drive time with output current. This helps alleviate zero-crossing distortion by limiting the drive time at low-current steps.

A torque DAC feature allows the controller to scale the output current without needing to scale the analog reference voltage input VREF. The torque DAC is accessed using digital input pins. This allows the controller to save power by decreasing the current consumption when not required.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

## 7.2 Functional Block Diagram
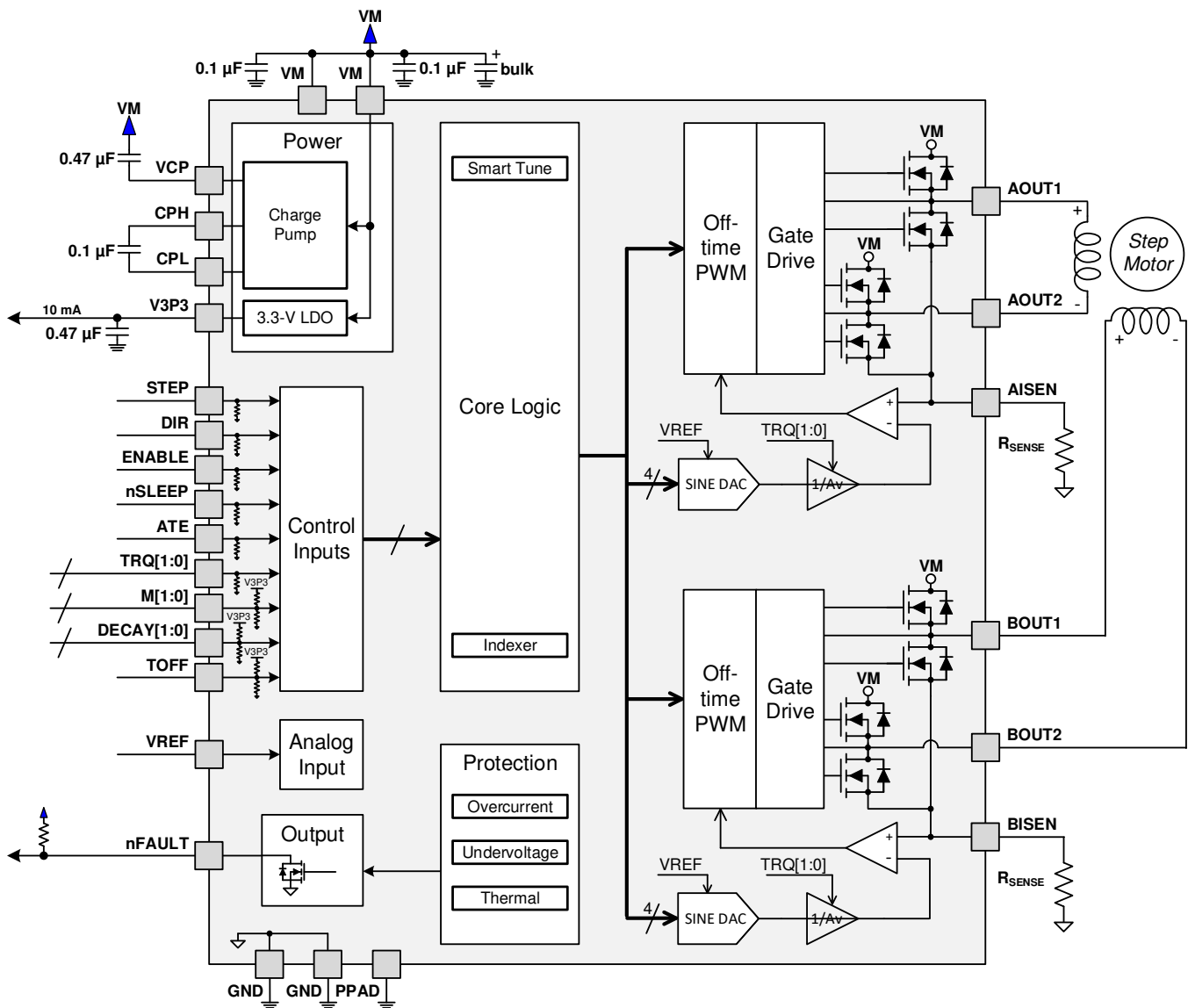
## 7.3 Feature Description

Table 1 lists the recommended values of the external components.

**Table 1. External Components**

| COMPONENT | PIN 1 | PIN 2 | RECOMMENDED |
|---|---|---|---|
| $C_{VM1}$ | VM | GND | 0.1-µF ceramic capacitor rated for VM per VM pin |
| $C_{VM1}$ | VM | GND | Bulk electrolytic capacitor rated for VM, recommended value is 100 µF, see Bulk Capacitance Sizing |
| $C_{VCP}$ | VCP | VM | 16-V, 0.47-µF ceramic capacitor |
| $C_{SW}$ | CPH | CPL | 0.1-µF X7R capacitor rated for VM |
| $C_{V3P3}$ | V3P3 | GND | 6.3-V, 0.47-µF ceramic capacitor |
| $R_{nFAULT}$ | $V_{MCU}$ [(1)] | nFAULT | > 5 kΩ pullup |
| $R_{AISEN}$ | AISEN | GND | Sense resistor, see Sense Resistor |
| $R_{BISEN}$ | BISEN | GND | |

(1)  $V_{MCU}$ is not a pin on the DRV8880, but a supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to V3P3

### 7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, rms, and full-scale.

#### 7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold $I_{OCP}$. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of $I_{OCP}$ specifies the peak current rating of the stepper motor driver. For the DRV8880, the peak current rating is 2.5 A per bridge.

#### 7.3.1.2 RMS Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The real operating rms current may be higher or lower depending on heatsinking and ambient temperature. For the DRV8880, the rms current rating is 1.4 A per bridge.

#### 7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Since the sineusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the IC. The full-scale current rating is approximately $\sqrt{2} \times I_{rms}$. The full-scale current is set by VREF, the sense resistor, and Torque DAC when configuring the DRV8880 , see Current Regulation for details. For the DRV8880, the full-scale current rating is 2.0 A per bridge.
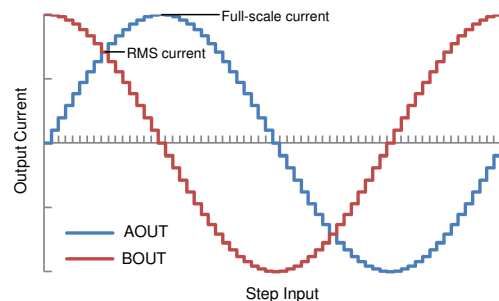


**Figure 12.  Full-Scale and rms Current**

### 7.3.2 PWM Motor Drivers

The DRV8880 contains drivers for two full H-bridges. A block diagram of the circuitry is shown in Figure 13.
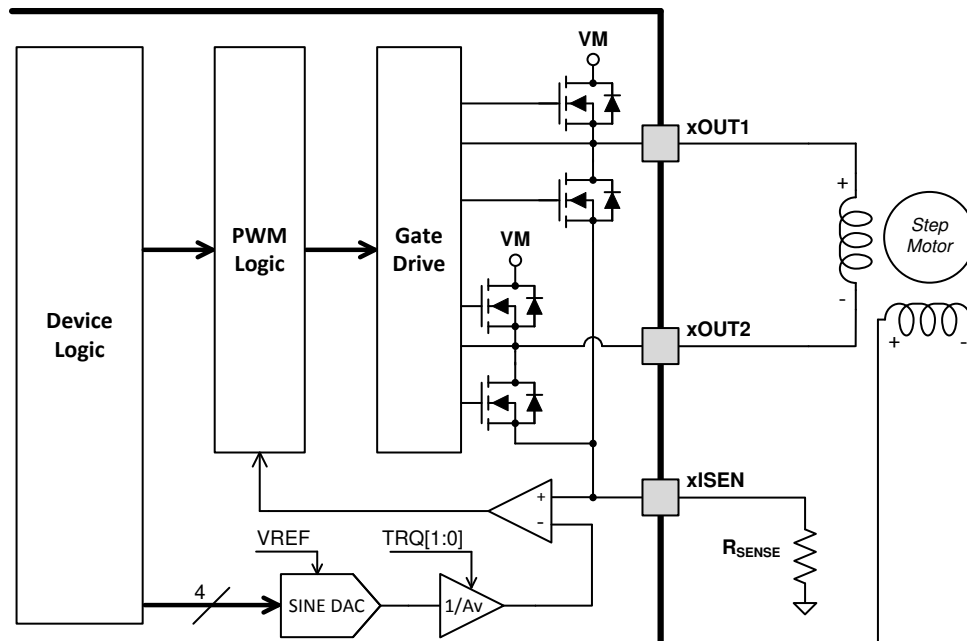


**Figure 13. PWM Motor Driver Block Diagram**

### 7.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8880 allows a number of different stepping configurations. The Mx pins are used to configure the stepping format as shown in Table 2.

**Table 2. Microstepping Settings**

| M1 | M0 | STEP MODE |
|----|----|-----------|
| 0 | 0 | Full step (2-phase excitation) with 71% current |
| 0 | 1 | Non-circular 1/2 step |
| 1 | 0 | 1/2 step |
| 1 | 1 | 1/4 step |
| 0 | Z | 1/8 step |
| 1 | Z | 1/16 step |
| Z | 0 | Reserved |
| Z | 1 | Reserved |
| Z | Z | Reserved |

Table 3 shows the relative current and step directions for full-step through 1/16-step operation. The AOUT current is the sine of the electrical angle; BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from xOUT1 to xOUT2 while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table. The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

Note that if the step mode is changed while stepping, the indexer will advance to the next valid state for the new MODE setting at the rising edge of STEP.

The home state is an electrical angle of 45°. This state is entered after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode. This is shown in Table 3 with the highlighted row.

### Table 3. Microstepping Relative Current Per Step

| FULL STEP | 1/2 STEP | 1/4 STEP | 1/8 STEP | 1/16 STEP | ELECTRICAL ANGLE (°) | AOUT CURRENT (% full-scale) | BOUT CURRENT (% full-scale) |
|---|---|---|---|---|---|---|---|
| | 1 | 1 | 1 | 1 | 0.000° | 0% | 100% |
| | | | | 2 | 5.625° | 10% | 100% |
| | | | 2 | 3 | 11.250° | 20% | 98% |
| | | | | 4 | 16.875° | 29% | 96% |
| | | 2 | 3 | 5 | 22.500° | 38% | 92% |
| | | | | 6 | 28.125° | 47% | 88% |
| | | | 4 | 7 | 33.750° | 56% | 83% |
| | | | | 8 | 39.375° | 63% | 77% |
| 1 | 2 | 3 | 5 | 9 | 45.000° | 71% | 71% |
| | | | | 10 | 50.625° | 77% | 63% |
| | | | 6 | 11 | 56.250° | 83% | 56% |
| | | | | 12 | 61.875° | 88% | 47% |
| | | 4 | 7 | 13 | 67.500° | 92% | 38% |
| | | | | 14 | 73.125° | 96% | 29% |
| | | | 8 | 15 | 78.750° | 98% | 20% |
| | | | | 16 | 84.375° | 100% | 10% |
| | 3 | 5 | 9 | 17 | 90.000° | 100% | 0% |
| | | | | 18 | 95.625° | 100% | −10% |
| | | | 10 | 19 | 101.250° | 98% | −20% |
| | | | | 20 | 106.875° | 96% | −29% |
| | | 6 | 11 | 21 | 112.500° | 92% | −38% |
| | | | | 22 | 118.125° | 88% | −47% |
| | | | 12 | 23 | 123.750° | 83% | −56% |
| | | | | 24 | 129.375° | 77% | −63% |
| 2 | 4 | 7 | 13 | 25 | 135.000° | 71% | −71% |
| | | | | 26 | 140.625° | 63% | −77% |
| | | | 14 | 27 | 146.250° | 56% | −83% |
| | | | | 28 | 151.875° | 47% | −88% |
| | | 8 | 15 | 29 | 157.500° | 38% | −92% |
| | | | | 30 | 163.125° | 29% | −96% |
| | | | 16 | 31 | 168.750° | 20% | −98% |
| | | | | 32 | 174.375° | 10% | −100% |
| | 5 | 9 | 17 | 33 | 180.000° | 0% | −100% |
| | | | | 34 | 185.625° | −10% | −100% |
| | | | 18 | 35 | 191.250° | −20% | −98% |
| | | | | 36 | 196.875° | −29% | −96% |
| | | 10 | 19 | 37 | 202.500° | −38% | −92% |
| | | | | 38 | 208.125° | −47% | −88% |
| | | | 20 | 39 | 213.750° | −56% | −83% |
| | | | | 40 | 219.375° | −63% | −77% |
| 3 | 6 | 11 | 21 | 41 | 225.000° | −71% | −71% |
| | | | | 42 | 230.625° | −77% | −63% |
| | | | 22 | 43 | 236.250° | −83% | −56% |
| | | | | 44 | 241.875° | −88% | −47% |
| | | 12 | 23 | 45 | 247.500° | −92% | −38% |
| | | | | 46 | 253.125° | −96% | −29% |
| | | | 24 | 47 | 258.750° | −98% | −20% |

Product Folder Links: *DRV8880*

**Table 3. Microstepping Relative Current Per Step (continued)**

| FULL STEP | 1/2 STEP | 1/4 STEP | 1/8 STEP | 1/16 STEP | ELECTRICAL ANGLE (°) | AOUT CURRENT (% full-scale) | BOUT CURRENT (% full-scale) |
|---|---|---|---|---|---|---|---|
| | | | | 48 | 264.375° | −100% | −10% |
| | 7 | 13 | 25 | 49 | 270.000° | −100% | 0% |
| | | | | 50 | 275.625° | −100% | 10% |
| | | | 26 | 51 | 281.250° | −98% | 20% |
| | | | | 52 | 286.875° | −96% | 29% |
| | | 14 | 27 | 53 | 292.500° | −92% | 38% |
| | | | | 54 | 298.125° | −88% | 47% |
| | | | 28 | 55 | 303.750° | −83% | 56% |
| | | | | 56 | 309.375° | −77% | 63% |
| 4 | 8 | 15 | 29 | 57 | 315.000° | −71% | 71% |
| | | | | 58 | 320.625° | −63% | 77% |
| | | | 30 | 59 | 326.250° | −56% | 83% |
| | | | | 60 | 331.875° | −47% | 88% |
| | | 16 | 31 | 61 | 337.500° | −38% | 92% |
| | | | | 62 | 343.125° | −29% | 96% |
| | | | 32 | 63 | 348.750° | −20% | 98% |
| | | | | 64 | 354.375° | −10% | 100% |
| | 1 | 1 | 1 | 1 | 360.000° | 0% | 100% |

Non-circular 1/2–step operation is shown in Table 4. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor rpm.

**Table 4. Non-Circular 1/2-Stepping Current**

| NON-CIRCULAR 1/2 STEP | ELECTRICAL ANGLE (°) | AOUT CURRENT (% FULL-SCALE) | BOUT CURRENT (% FULL-SCALE) |
|---|---|---|---|
| 1 | 0° | 0 | 100 |
| 2 | 45° | 100 | 100 |
| 3 | 90° | 100 | 0 |
| 4 | 135° | 100 | -100 |
| 5 | 180° | 0 | -100 |
| 6 | 225° | −100 | -100 |
| 7 | 270° | −100 | 0 |
| 8 | 315° | −100 | 100 |

Product Folder Links: *DRV8880*

### 7.3.4 Current Regulation

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. After the current hits the current chopping threshold, the bridge enters a decay mode for a fixed period of time to decrease the current, which is configurable between 10 and 30 µs through the tri-level input TOFF. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

**Table 5. Off-Time Settings**

| TOFF | OFF-TIME $t_{OFF}$ |
|------|-----------|
| 0 | 20 µs |
| 1 | 30 µs |
| Z | 10 µs |

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pin with a reference voltage. To generate the reference voltage for the current chopping comparator, the output of a sine lookup table is applied to a sine-weighted DAC, whose full-scale output voltage is set by VREF. This voltage is attenuated by a factor of Av. In addition, the TRQx pins further scale the reference.
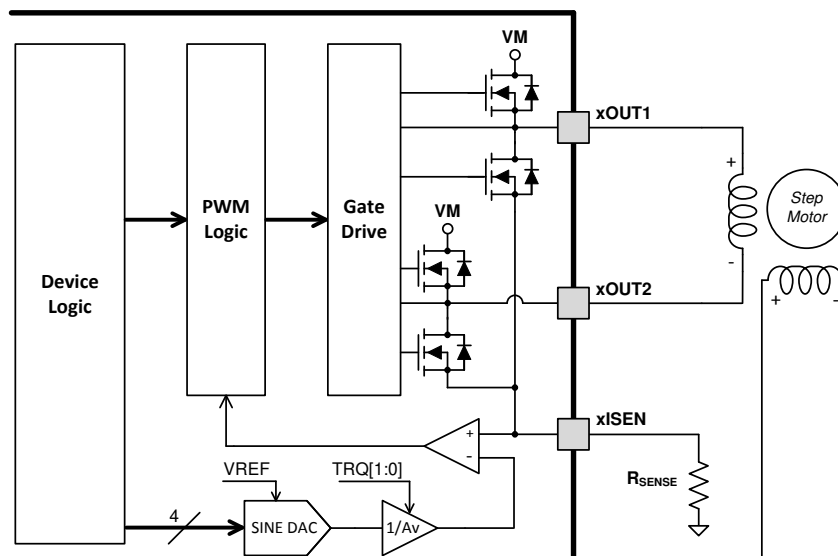


**Figure 14.  Current Regulation Block Diagram**

The full-scale (100%) chopping current is calculated as follows:

$$I_{FS} \ (A) = \frac{VREF \ (V) \times TRQ \ (\%)}{A_V \times R_{SENSE} \ (\Omega)} = \frac{VREF \ (V) \times TRQ \ (\%)}{6.6 \times R_{SENSE} \ (\Omega)} \tag{1}$$

The TRQx pins are the inputs to a Torque DAC used to scale the output current. The current scalar value for different inputs is shown below.

**Table 6. Torque DAC Settings**

| TRQ1 | TRQ0 | CURRENT SCALAR (TRQ) | EFFECTIVE ATTENUATION |
|------|------|----------------------|-----------------------|
| 1 | 1 | 25% | 26.4 V/V |
| 1 | 0 | 50% | 13.2 V/V |
| 0 | 1 | 75% | 8.8 V/V |
| 0 | 0 | 100% | 6.6 V/V |

Table 7 gives the xISEN trip voltage at a given DAC code and TRQ[1:0] setting for 1/16 step mode. In this table, VREF = 3.3 V.

**Table 7. xISEN Trip Voltages over Torque DAC and Microsteps**

| 1/16 STEP (SINE DAC CODE) | TORQUE DAC TRQ[1:0] SETTING | | | |
|---|---|---|---|---|
| | 00 – 100% | 01 – 75% | 10 – 50% | 11 – 25% |
| 16 | 500.0 mV | 375.0 mV | 250.0 mV | 125.0 mV |
| 15 | 490.0 mV | 367.5 mV | 245.0 mV | 122.5 mV |
| 14 | 480.0 mV | 360.0 mV | 240.0 mV | 120.0 mV |
| 13 | 460.0 mV | 345.0 mV | 230.0 mV | 115.0 mV |
| 12 | 440.0 mV | 330.0 mV | 220.0 mV | 110.0 mV |
| 11 | 415.0 mV | 311.3 mV | 207.5 mV | 103.8 mV |
| 10 | 385.0 mV | 288.8 mV | 192.5 mV | 96.3 mV |
| 9 | 355.0 mV | 266.3 mV | 177.5 mV | 88.8 mV |
| 8 | 315.0 mV | 236.3 mV | 157.5 mV | 78.8 mV |
| 7 | 280.0 mV | 210.0 mV | 140.0 mV | 70.0 mV |
| 6 | 235.0 mV | 176.3 mV | 117.5 mV | 58.8 mV |
| 5 | 190.0 mV | 142.5 mV | 95.0 mV | 47.5 mV |
| 4 | 145.0 mV | 108.8 mV | 72.5 mV | 36.3 mV |
| 3 | 100.0 mV | 75.0 mV | 50.0 mV | 25.0 mV |
| 2 | 50.0 mV | 37.5 mV | 25.0 mV | 12.5 mV |
| 1 | 0.0 mV | 0.0 mV | 0.0 mV | 0.0 mV |

Product Folder Links: *DRV8880*

### 7.3.5 Decay Modes

A fixed decay mode is selected by setting the tri-level DECAYx pins as shown in Table 8. Please note that if the ATE pin is logic high, the DECAYx pins are ignored and smart tune is used.

**Table 8. Decay Mode Settings**

| DECAY1 | DECAY0 | INCREASING STEPS | DECREASING STEPS |
|--------|--------|------------------|------------------|
| 0 | 0 | Slow Decay | Slow Decay |
| 0 | 1 | Slow Decay | Mixed Decay: 2 $t_{BLANK}$ |
| 1 | 0 | Slow Decay | Mixed Decay: 30% Fast |
| 1 | 1 | Mixed Decay: 30% Fast | Mixed Decay: 30% Fast |
| 0 | Z | Slow Decay | Mixed Decay: 60% Fast |
| 1 | Z | Slow Decay | Fast Decay |
| Z | 0 | Mixed Decay: 1 $t_{BLANK}$ | Mixed Decay: 30% Fast |
| Z | 1 | Mixed Decay: 60% Fast | Mixed Decay: 60% Fast |
| Z | Z | Fast Decay | Fast Decay |

Increasing and decreasing current are defined in the chart below. For the Slow/Mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step mode, the increasing step decay mode is always used.
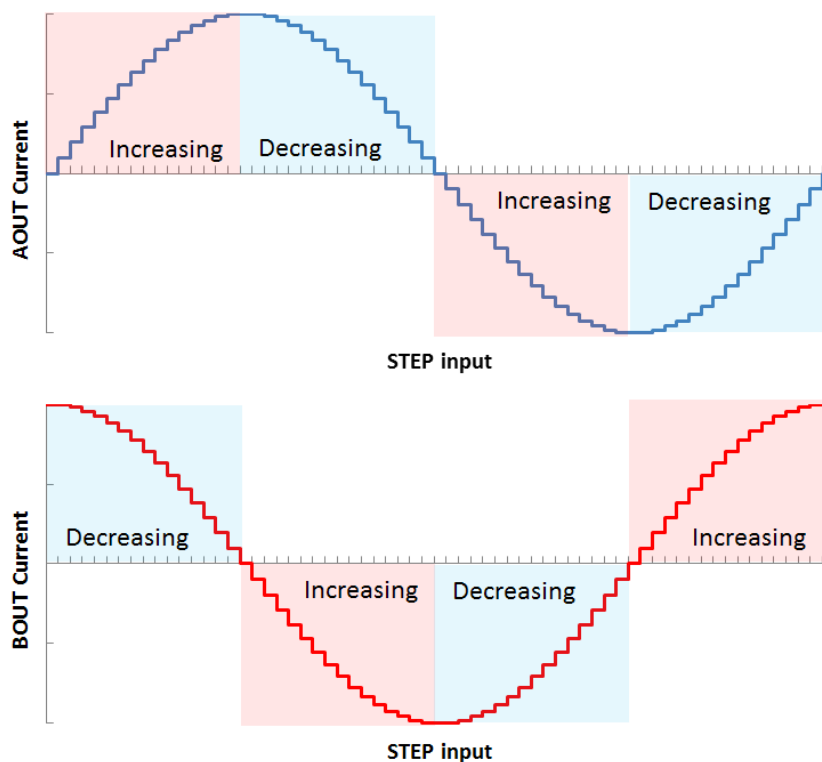


**Figure 15. Definition of Increasing and Decreasing Steps**

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### 7.3.5.1 Mode 1: Slow Decay for Increasing and Decreasing Current
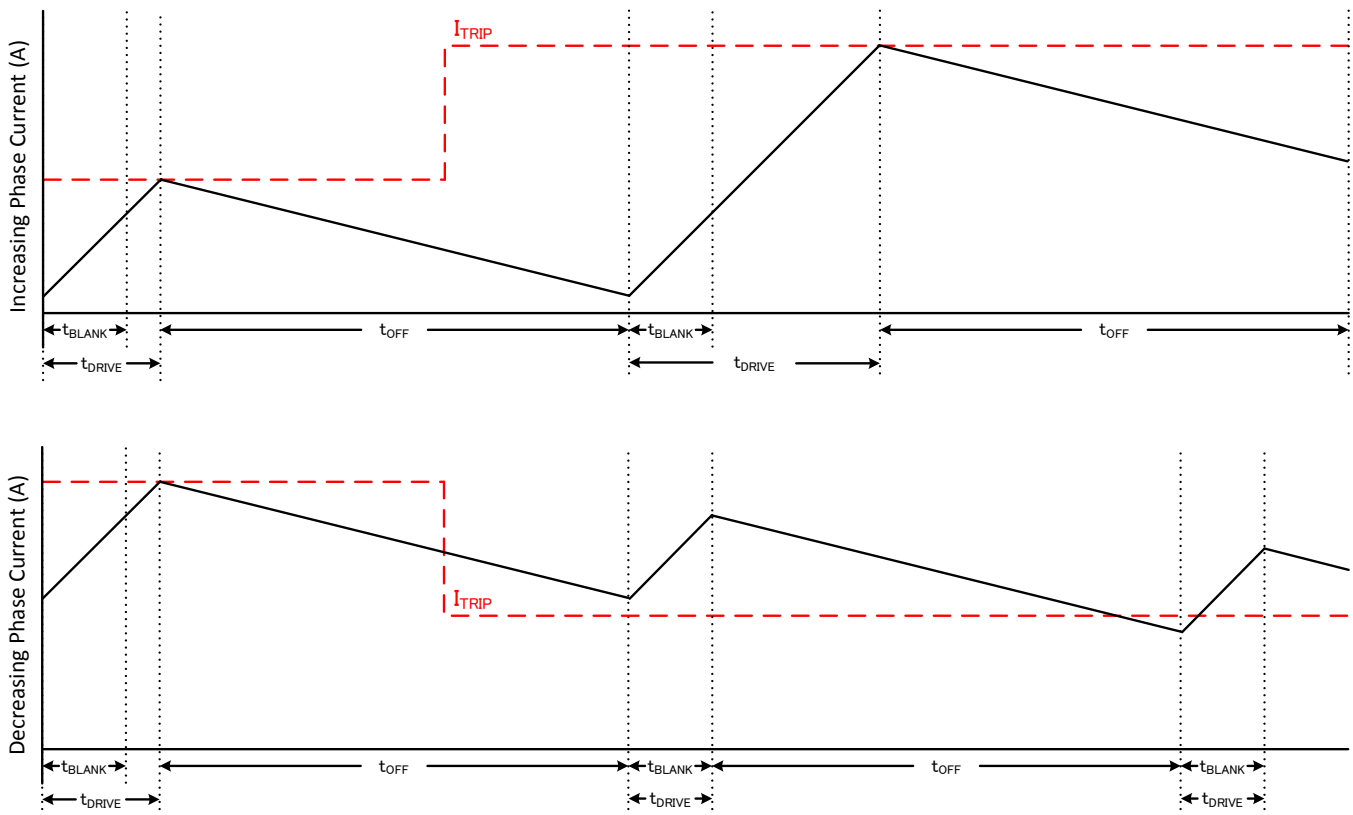


**Figure 16. Slow/Slow Decay Mode**

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given $t_{OFF}$. However on decreasing current steps, slow decay will take a long time to settle to the new ITRIP level because the current decreases very slowly.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and may require a large off-time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

### 7.3.5.2  Mode 2: Slow Decay for Increasing Current, Mixed Decay for Decreasing current
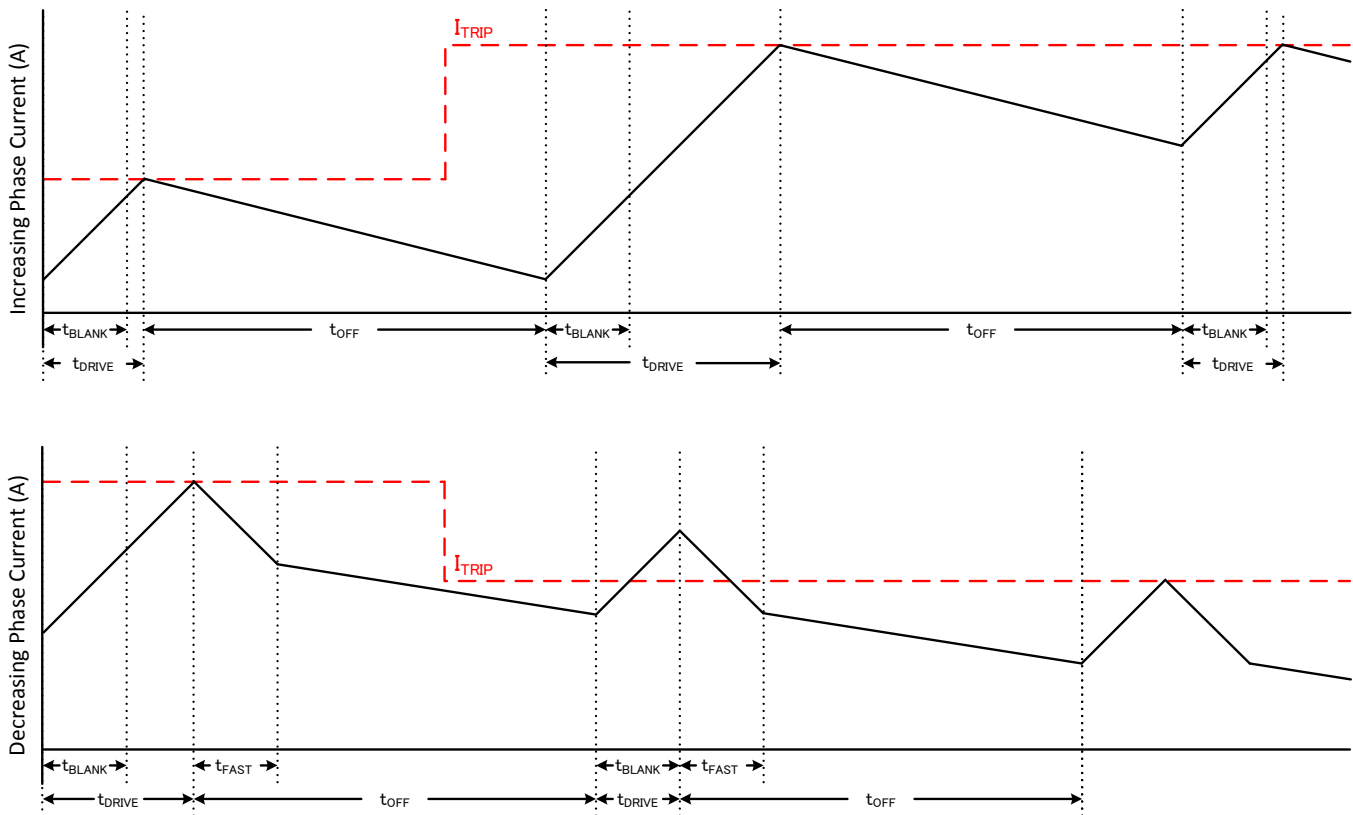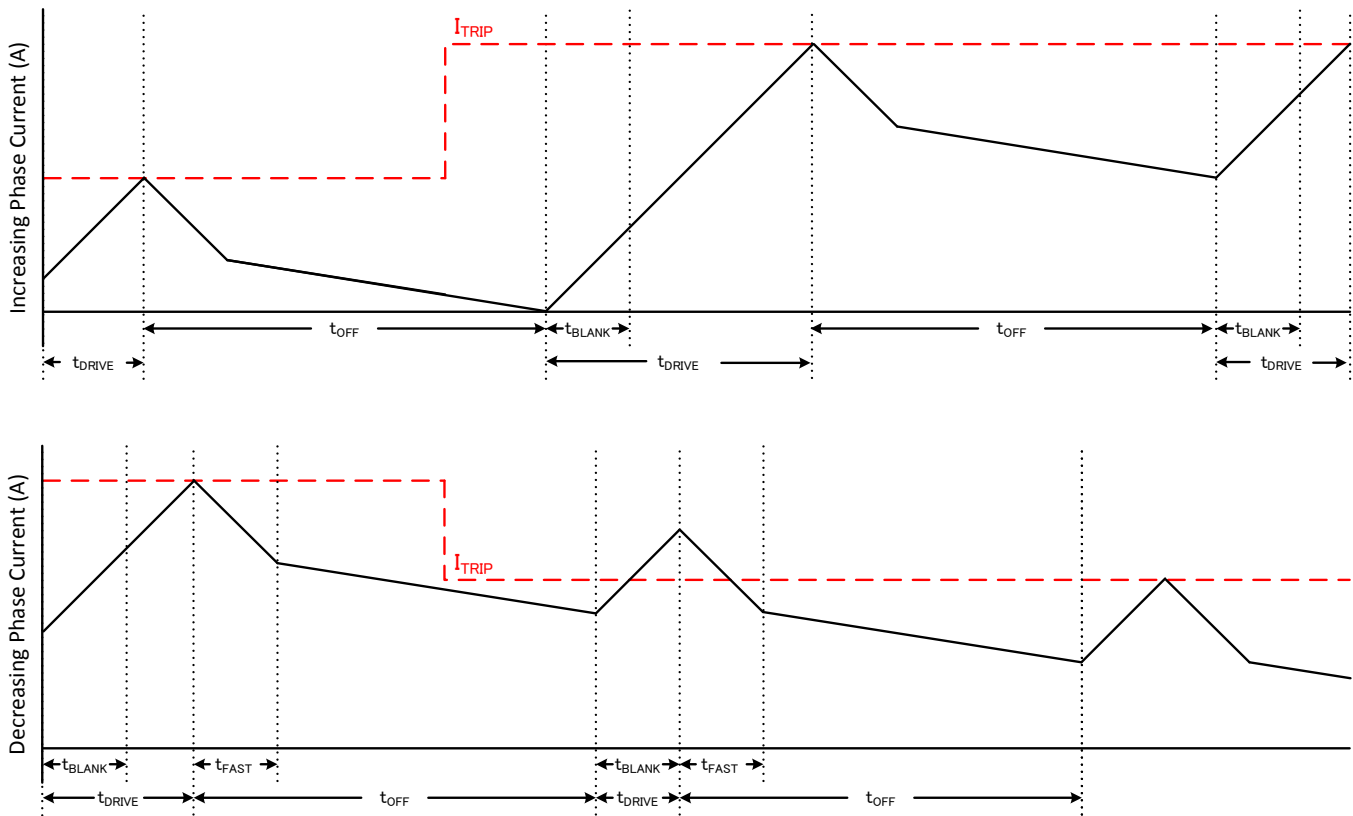


**Figure 17.  Slow/Mixed Decay Mode**

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of $t_{OFF}$. In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, since for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay will settle to the new $I_{TRIP}$ level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and may require a large off-time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

### 7.3.5.3 Mode 3: Mixed Decay for Increasing and Decreasing Current



**Figure 18. Mixed/Mixed Decay Mode**

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of $t_{OFF}$. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay will settle to the new $I_{TRIP}$ level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing/decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

### 7.3.5.4  Mode 4: Slow Decay for Increasing Current, Fast Decay for Decreasing current
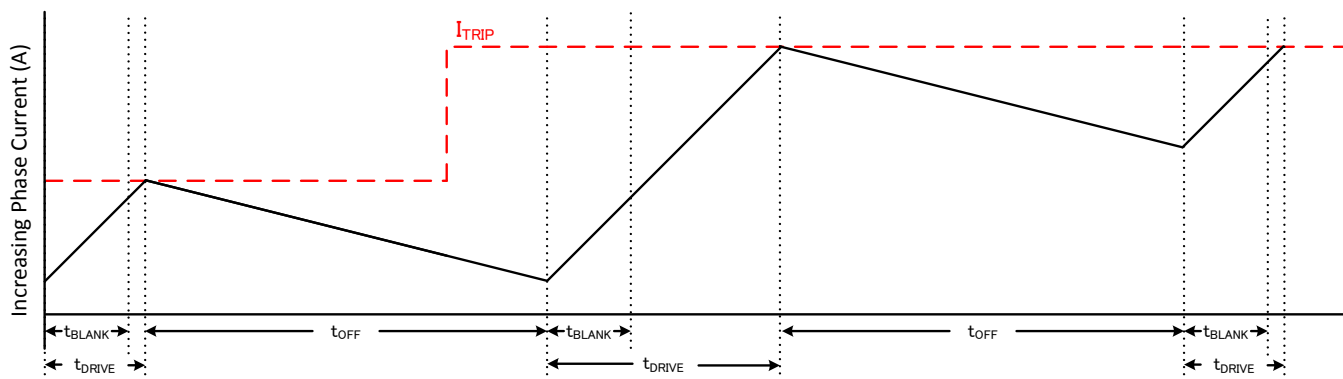


Please note that these graphs are not the same scale; $t_{OFF}$ is the same
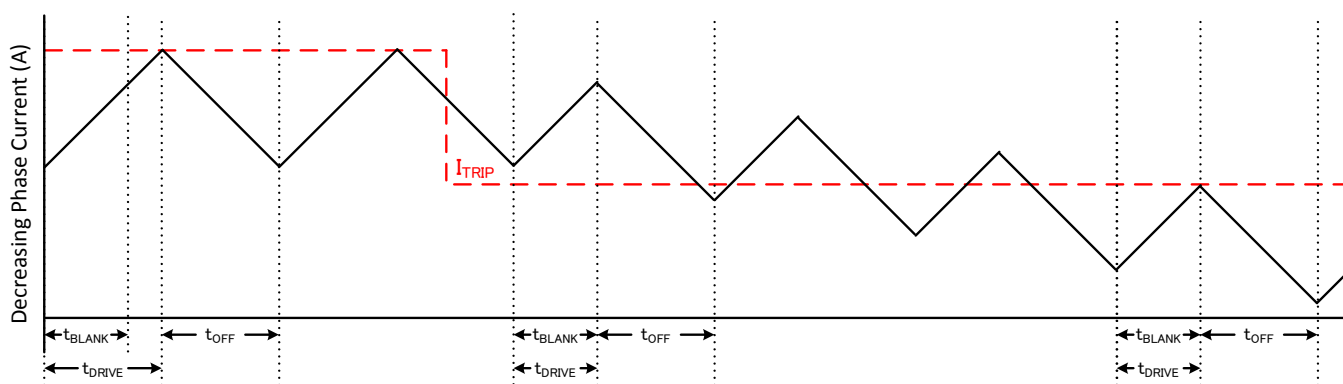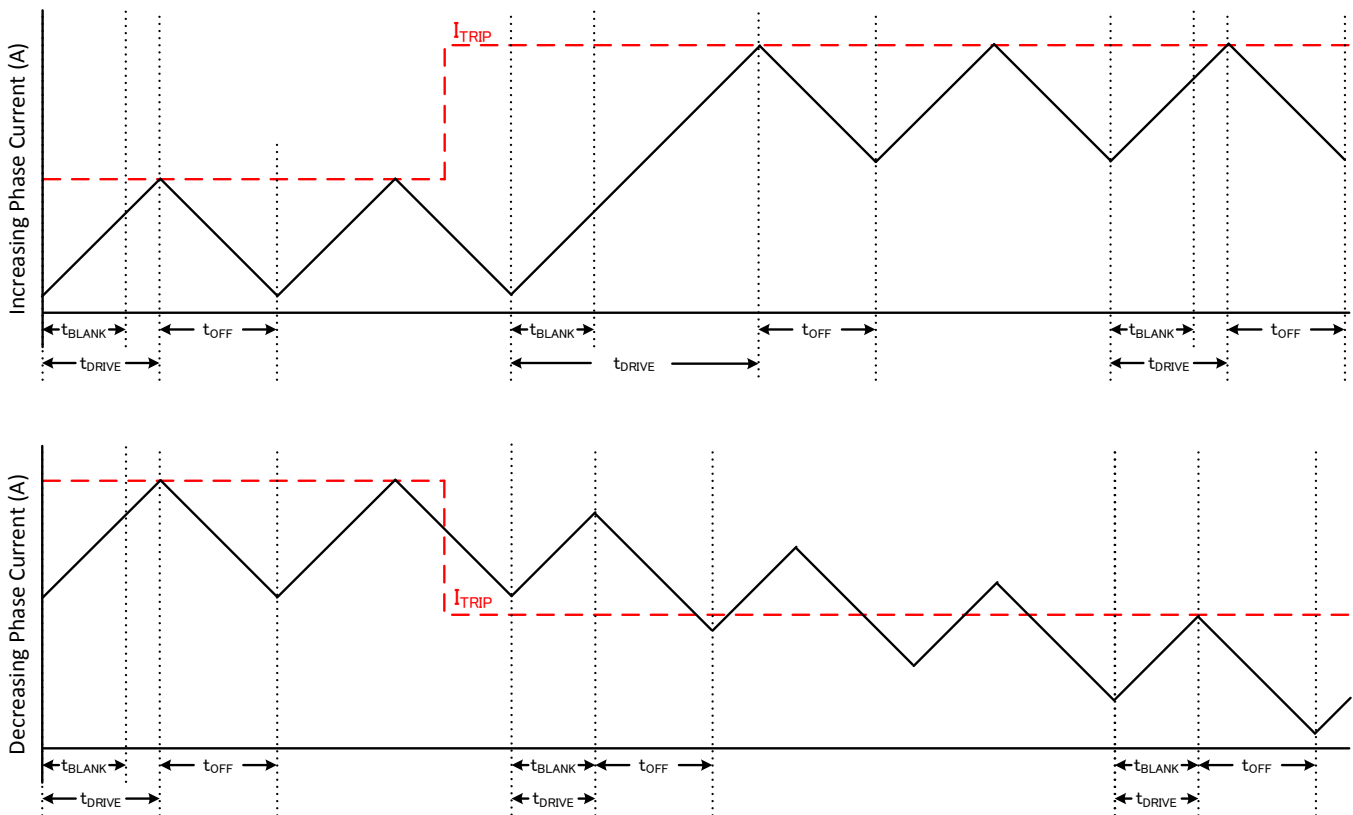


**Figure 19. Slow/Fast Decay Mode**

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction. In this mode, fast decay only occurs during decreasing current. Slow decay is used for increasing current.

Fast decay exhibits the highest current ripple of the decay modes for a given $t_{OFF}$. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

Product Folder Links: *DRV8880*

### 7.3.5.5 Mode 5: Fast Decay for Increasing and Decreasing Current



**Figure 20. Fast/Fast Decay Mode**

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction.

Fast decay exhibits the highest current ripple of the decay modes for a given $t_{OFF}$. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

### 7.3.6 Smart Tune

To enable the smart tune mode, pull the ATE pin logic high. Ensure the DECAYx pins are logic low. The smart tune mode is registered internally when exiting from sleep mode or the power-up sequence. The ATE pin can be shorted to V3P3 to pull it logic high for this purpose.

Smart tune greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle in order to prevent regulation loss. If there is a long drive time to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle in order to operate with less ripple and more efficiently. On falling steps, smart tune will automatically switch to fast decay in order to reach the next step quickly.

Smart tune will automatically adjust the decay scheme based on operating factors like:
• Motor winding resistance and inductance
• Motor aging effects
• Motor dynamic speed and load
• Motor supply voltage variation
• Motor back-EMF difference on rising and falling steps
• Step transitions
• Low-current vs. high-current dI/dt

### 7.3.7 Adaptive Blanking Time

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a period of time before enabling the current sense circuitry. Note that the blanking time also sets the minimum drive time of the PWM.

The blanking time is automatically scaled so that the drive time is reduced at lower current steps.

The time $t_{BLANK}$ is determined by the sine DAC code and the torque DAC setting. The timing information for $t_{BLANK}$ is given in Table 9.

**Table 9. Adaptive Blanking Time Settings over Torque DAC and Microsteps**

| SINE DAC CODE | TORQUE DAC TRQ[1:0] SETTING | | | |
|---|---|---|---|---|
| | 00 – 100% | 01 – 75% | 10 – 50% | 11 – 25% |
| 16 | 1.80 µs | 1.50 µs | 1.50 µs | 1.20 µs |
| 15 | 1.80 µs | 1.50 µs | 1.50 µs | 1.20 µs |
| 14 | 1.80 µs | 1.50 µs | 1.50 µs | 1.20 µs |
| 13 | 1.80 µs | 1.50 µs | 1.50 µs | 1.20 µs |
| 12 | 1.80 µs | 1.50 µs | 1.50 µs | 1.20 µs |
| 11 | 1.80 µs | 1.50 µs | 1.50 µs | 1.20 µs |
| 10 | 1.80 µs | 1.50 µs | 1.50 µs | 1.20 µs |
| 9 | 1.80 µs | 1.50 µs | 1.50 µs | 1.20 µs |
| 8 | 1.50 µs | 1.50 µs | 1.20 µs | 0.90 µs |
| 7 | 1.50 µs | 1.50 µs | 1.20 µs | 0.90 µs |
| 6 | 1.50 µs | 1.50 µs | 1.20 µs | 0.90 µs |
| 5 | 1.50 µs | 1.50 µs | 1.20 µs | 0.90 µs |
| 4 | 1.20 µs | 1.20 µs | 0.90 µs | 0.90 µs |
| 3 | 1.20 µs | 1.20 µs | 0.90 µs | 0.90 µs |
| 2 | 0.90 µs | 0.90 µs | 0.90 µs | 0.90 µs |
| 1 | 0.90 µs | 0.90 µs | 0.90 µs | 0.90 µs |

Product Folder Links: *DRV8880*

### 7.3.8 Charge Pump

A charge pump is integrated in order to supply a high-side NMOS gate drive voltage. The charge pump requires a capacitor between the VM and VCP pins. Additionally a low-ESR ceramic capacitor is required between pins CPH and CPL.
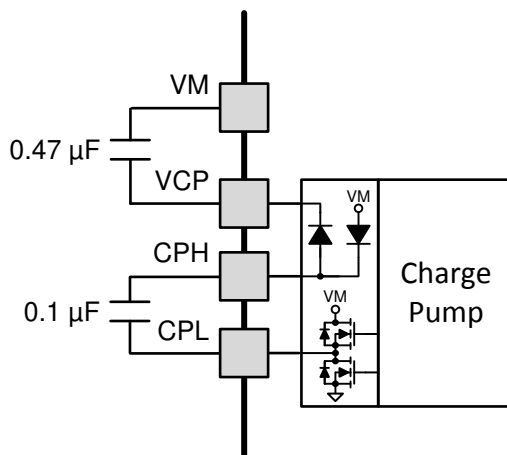


**Figure 21. Charge Pump Diagram**

### 7.3.9 LDO Voltage Regulator

An LDO regulator is integrated into the DRV8880. It can be used to provide the supply voltage for low-current devices. For proper operation, bypass V3P3 to GND using a ceramic capacitor.

The V3P3 output is nominally 3.3 V. When the V3P3 LDO current load exceeds 10 mA, the LDO will behave like a constant current source. The output voltage will drop significantly with currents greater than 10 mA.
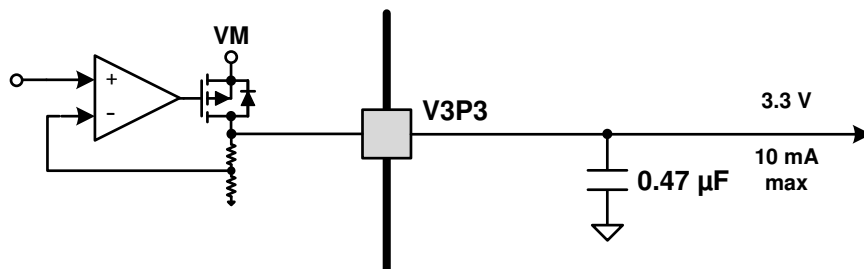


**Figure 22. LDO Diagram**

If a digital input needs to be tied permanently high (that is, M or TOFF), it is preferable to tie the input to V3P3 instead of an external regulator. This will save power when VM is not applied or in sleep mode: V3P3 is disabled and current will not be flowing through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 100 kΩ, and tri-level inputs have a typical pulldown of 40 kΩ.

Product Folder Links: *DRV8880*

### 7.3.10 Logic and Tri-Level Pin Diagrams

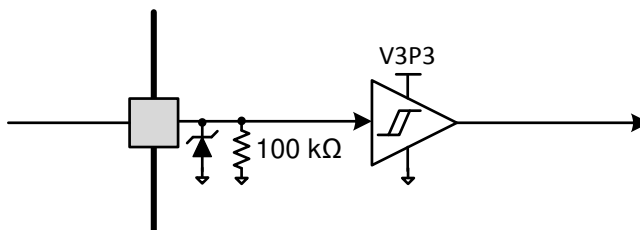The diagram below gives the input structure for logic-level pins STEP, DIR, ENABLE, nSLEEP, TRQ0, TRQ1, and ATE:



**Figure 23. Logic-level Input Pin Diagram**

Tri-level logic pins TOFF, M0, M1, DECAY0, and DECAY1 have the following structure:
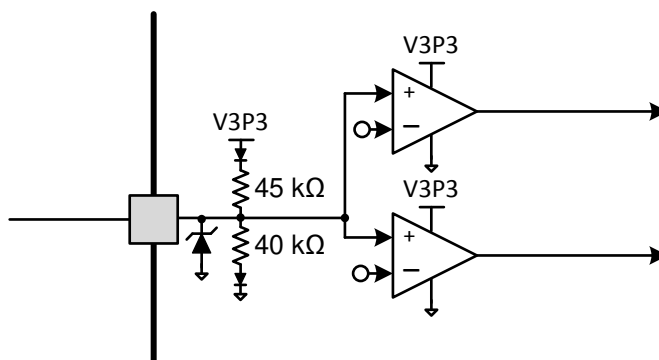


**Figure 24. Tri-level Input Pin Diagram**

### 7.3.11 Power Supplies and Input Pins

The control pins and reference input pin can be driven within the recommended operating conditions without the VM power supply present, or when the device is in sleep mode.

Each control pin has a weak pulldown resistor to ground. TI recommends setting the inputs to a logic low when in sleep mode to minimize current through the pulldown resistors.

### 7.3.12 Protection Circuits

The DRV8880 is fully protected against undervoltage, charge pump undervoltage, overcurrent, and overtemperature events.

### 7.3.13 VM UVLO (UVLO2)

If at any time the voltage on the VM pin falls below the VM undervoltage lockout threshold voltage ($V_{UVLO2}$), all FETs in the H-bridge will be disabled, the charge pump will be disabled, and the nFAULT pin will be driven low. Operation will resume when VM rises above the UVLO2 threshold. The nFAULT pin will be released after operation has resumed.

The indexer position is not reset by this fault even though the output drivers are disabled. The indexer position is maintained and internal logic remains active until VM falls below the logic undervoltage threshold ($V_{UVLO1}$).

### 7.3.14 Logic Undervoltage (UVLO1)

If at any time the voltage on the VM pin falls below the logic undervoltage threshold voltage ($V_{UVLO1}$), the internal logic is reset, and the V3P3 regulator is disabled. Operation will resume when VM rises above the UVLO1 threshold. The nFAULT pin is logic low during this state since it is pulled low upon encountering VM undervoltage. Decreasing VM below this undervoltage threshold will reset the indexer position.

### 7.3.15 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the charge pump undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Operation will resume when VCP rises above the CPUV threshold. The nFAULT pin will be released after operation has resumed.

### 7.3.16 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume. The nFAULT pin will be released after operation has resumed.

### 7.3.17 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than $t_{OCP}$, all FETs in the H-bridge will be disabled and nFAULT will be driven low. In addition to this FET current limit, an overcurrent condition is also detected if the voltage at xISEN exceeds $V_{OCP}$.

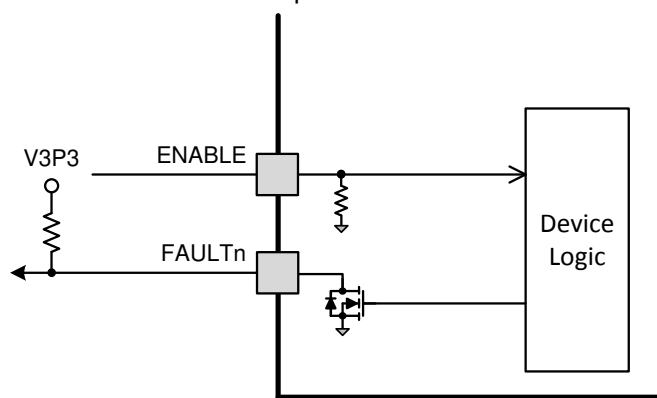The overcurrent fault response can be set to either latched mode or retry mode:
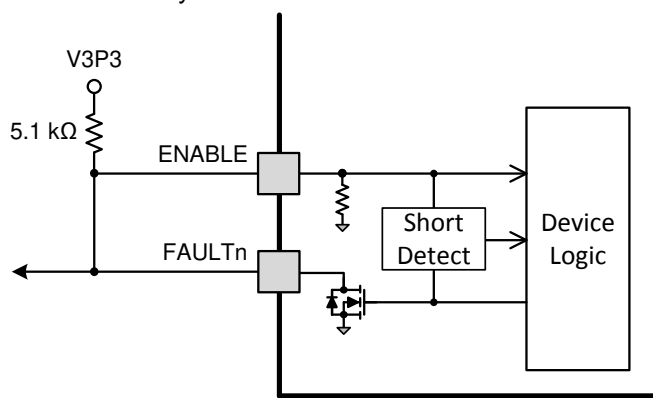


**Figure 25. Latched OCP Mode**

**Figure 26. Retry OCP Mode**

In latched mode, operation will resume after the ENABLE pin is brought logic low for at least 1 μs to reset the output driver. The nFAULT pin will be released after ENABLE is returned logic high. Removing and re-applying VM or toggling nSLEEP will also reset the latched fault.

Product Folder Links: *DRV8880*

In retry mode, the driver will be re-enabled after the OCP retry period ($t_{RETRY}$) has passed. nFAULT becomes high again after the retry time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes and nFAULT remains deasserted.

A microcontroller can retain control of the ENABLE pin while in retry mode if it is operated like an open-drain output. Many microcontrollers support this. When the DRV8880 is operating normally, configure the MCU GPIO as an input. In this state, the MCU can detect whenever nFAULT is pulled low. In order to disable the DRV8880 output, configure the GPIO output state as low, and then configure the GPIO as an output.

Alternatively, a logic-level FET may be used to create an open drain external to the MCU. In this case, an additional MCU GPIO may be required in order to monitor the nFAULT pin.
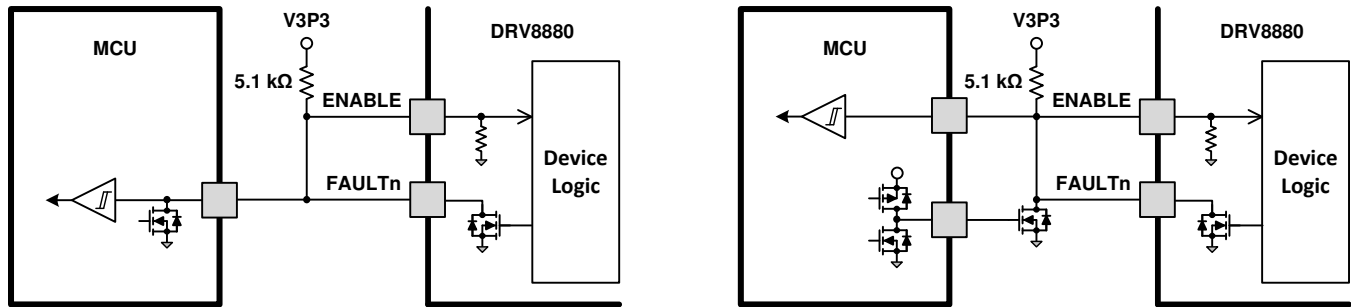


**Figure 27. Methods For Operating in Retry Mode**

**Table 10. Fault Condition Summary**

| FAULT | CONDITION | ERROR REPORT | H-BRIDGE | CHARGE PUMP | INDEXER | V3P3 | RECOVERY |
|---|---|---|---|---|---|---|---|
| VM undervoltage (UVLO2) | VM < $V_{UVLO2}$ (max 6.4 V) | nFAULT | Disabled | Disabled | Operating | Operating | VM > $V_{UVLO2}$ (max 6.5 V) |
| Logic undervoltage (UVLO1) | VM < $V_{UVLO2}$ (max 4.9 V) | None | Disabled | Disabled | Disabled | Operating | VM > $V_{UVLO2}$ (max 4.8 V) |
| VCP undervoltage (CPUV) | VCP < $V_{CPUV}$ (typ VM + 1.8 V) | nFAULT | Disabled | Operating | Operating | Operating | VCP > $V_{CPUV}$ (typ VM + 1.9 V) |
| Thermal Shutdown (TSD) | $T_J$ > $T_{TSD}$ (min 150°C) | nFAULT | Disabled | Operating | Operating | Operating | $T_J$ < $T_{TSD}$ - $T_{HYS}$ ($T_{HYS}$ typ 35°C) |
| Overcurrent (OCP) | $I_{OUT}$ > $I_{OCP}$ (min 2.5 A) $V_{xISEN}$ > $V_{OCP}$ (min 0.9 V) | nFAULT | Disabled | Operating | Operating | Operating | ENABLE -or- $t_{RETRY}$ |

## 7.4 Device Functional Modes

The DRV8880 internal logic, indexer, and charge pump are operating unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled, the H-bridge FETs are disabled Hi-Z, and the V3P3 regulator is disabled. $t_{SLEEP}$ must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8880 is brought out of sleep mode automatically if nSLEEP is brought logic high. $t_{WAKE}$ must elapse before the outputs change state after wake-up.

If the ENABLE pin is brought logic low, the H-bridge outputs are disabled, but the charge pump and internal logic will remian active. A rising edge on STEP will advance the indexer, but the outputs will not change state until ENABLE brought logic high.

When VM falls below the VM undervoltage lockout threshold $V_{UVLO2}$, the output driver and charge pump are disabled, but the internal logic and V3P3 remain active. In this mode, STEP inputs will advance the indexer, but the outputs will remain disabled. If VM falls below the logic undervoltage threshold $V_{UVLO1}$, the internal logic is reset and the indexer will lose position.

**Table 11. Functional Modes Summary**

| CONDITION | | H-BRIDGE | CHARGE PUMP | INDEXER | V3P3 |
|---|---|---|---|---|---|
| Operating | 6.5 V < VM < 45 V nSLEEP pin = 1 ENABLE pin = 1 | Operating | Operating | Operating | Operating |
| Disabled | 6.5 V < VM < 45 V nSLEEP pin = 1 ENABLE pin = 0 | Disabled | Operating | Operating | Operating |
| Sleep mode | 5.0 V < VM < 45 V nSLEEP pin = 0 | Disabled | Disabled | Disabled | Disabled |
| Fault encountered | VM undervoltage (UVLO2) | Disabled | Disabled | Operating | Operating |
| | Logic undervoltage (UVLO1) | Disabled | Disabled | Disabled | Operating |
| | VCP undervoltage (CPUV) | Disabled | Operating | Operating | Operating |
| | Thermal shutdown (TSD) | Disabled | Operating | Operating | Operating |
| | Overcurrent (OCP) | Disabled | Operating | Operating | Operating |

Product Folder Links: *DRV8880*

# 8 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The DRV8880 is used in stepper control.

## 8.2 Typical Application

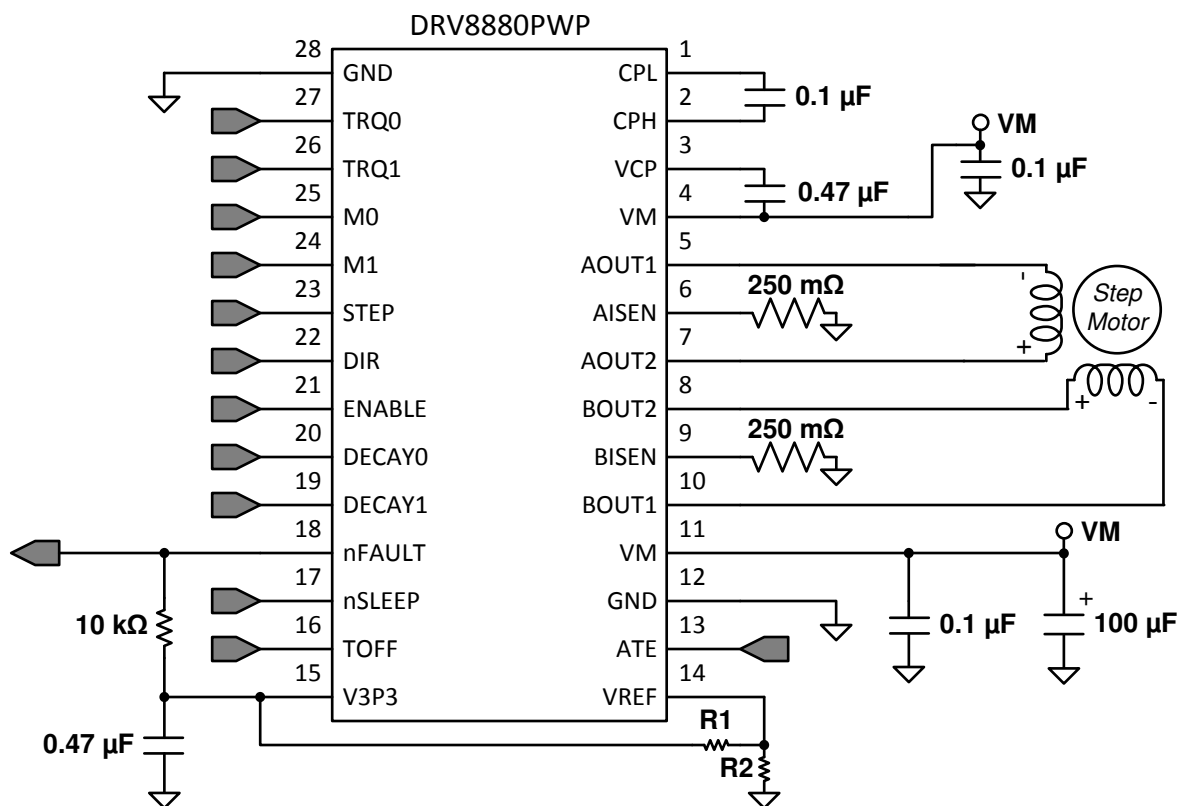The following design procedure can be used to configure the DRV8880.



**Figure 28. Typical Application Schematic**

### 8.2.1 Design Requirements

Table 12 gives design input parameters for system design.

**Table 12. Design Parameters**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Supply voltage | VM | 24 V |
| Motor winding resistance | $R_L$ | 0.8 Ω/phase |
| Motor winding inductance | $L_L$ | 1.4 mH/phase |
| Motor full step angle | $\theta_{step}$ | 1.8°/step |
| Target microstepping level | $n_m$ | 1/8 step |
| Target motor speed | v | 120 rpm |

**Table 12. Design Parameters (continued)**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Target full-scale current | $I_{FS}$ | 1.5 A |

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8880 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency $f_{step}$ must be applied to the STEP pin.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level ($n_m$), and motor full step angle ($\theta_{step}$),

$$f_{step}\ (steps\,/\,s) = \frac{v\ (rpm) \times 360\ (°\,/\,rot)}{\theta_{step}\ (°\,/\,step) \times n_m\ (steps\,/\,microstep) \times 60\ (s\,/\,min)} \tag{2}$$

$\theta_{step}$ can be found in the stepper motor data sheet or written on the motor itself.

For the DRV8880, the microstepping level is set by the Mx pins and can be any of the settings in the table below. Higher microstepping will mean a smother motor motion and less audible noise, but will increase switching losses and require a higher $f_{step}$ to achieve the same motor speed.

**Table 13. Microstepping Indexer Settings**

| M1 | M0 | STEP MODE |
|---|---|---|
| 0 | 0 | Full step (2-phase excitation) with 71% current |
| 0 | 1 | Non-circular 1/2 step |
| 1 | 0 | 1/2 step |
| 1 | 1 | 1/4 step |
| 0 | Z | 1/8 step |
| 1 | Z | 1/16 step |

**Example:** Target 120 rpm at 1/8 microstep mode. The motor is 1.8°/step

$$f_{step}\ (steps\,/\,s) = \frac{120\ rpm \times 360°\,/\,rot}{1.8°\,/\,step \times 1/\,8\ steps\,/\,microstep \times 60\ s\,/\,min} = 3.2\ kHz \tag{3}$$

#### 8.2.2.2 Current Regulation

In a stepper motor, the full-scale current ($I_{FS}$) is the maximum current driven through either winding. This quantity will depend on the TRQ pins, the VREF analog voltage, and the sense resistor value ($R_{SENSE}$). During stepping, $I_{FS}$ defines the current chopping threshold ($I_{TRIP}$) for the maximum current step.

$$I_{FS}\ (A) = \frac{VREF\ (V) \times TRQ\ (\%)}{A_v \times R_{SENSE}\ (\Omega)} = \frac{VREF\ (V) \times TRQ\ (\%)}{6.6 \times R_{SENSE}\ (\Omega)} \tag{4}$$

TRQ is a DAC used to scale the output current. The current scalar value for different inputs is shown below.

**Table 14. Torque DAC Settings**

| TRQ1 | TRQ0 | CURRENT SCALAR (TRQ) |
|---|---|---|
| 1 | 1 | 25% |
| 1 | 0 | 50% |
| 0 | 1 | 75% |
| 0 | 0 | 100% |

**Example:** If the desired full-scale current is 1.5 A

    Set $R_{SENSE}$ = 100 mΩ, assume TRQ = 100%.

    VREF would have to be 0.99 V.

    Create a resistor divider from V3P3 (3.3 V) to set VREF ≈ 0.99 V.

    Set R2 = 10 kΩ, set R1 = 22 kΩ

Note that $I_{FS}$ must also follow the equation below in order to avoid saturating the motor. VM is the motor supply voltage, and $R_L$ is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega) + R_{SENSE}\ (\Omega)}$$

(5)

### 8.2.2.3  Decay Modes

The DRV8880 supports several different decay modes: slow decay, fast decay, mixed decay, and smart tune. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold ($I_{TRIP}$), the DRV8880 will place the winding in one of the decay modes for $t_{OFF}$. After $t_{OFF}$, a new drive phase starts. For fixed decay modes (slow, fast, and mixed), the best setting can be determined by operating the motor and choosing the best setting.

### 8.2.2.4  Sense Resistor

For optimal performance, it is important for the sense resistor to be:
- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{rms}^2 \times R$. For example, if the rms motor current is 1.4A and a 250 mΩ sense resistor is used, the resistor will dissipate 1.4 $A^2 \times 0.25\ \Omega$ = 0.49 W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.
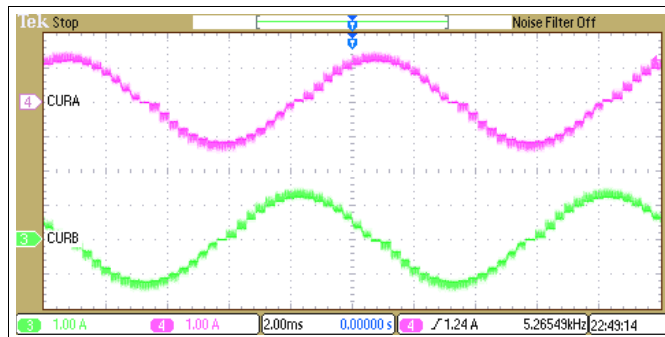
## 8.2.3 Application Curves



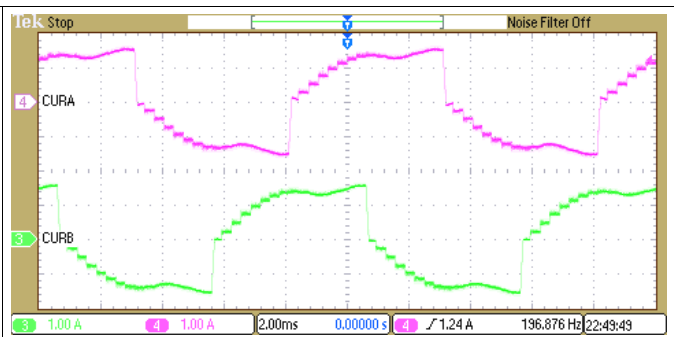**Figure 29. Mixed Decay 30% Fast on Increasing and Decreasing Steps**



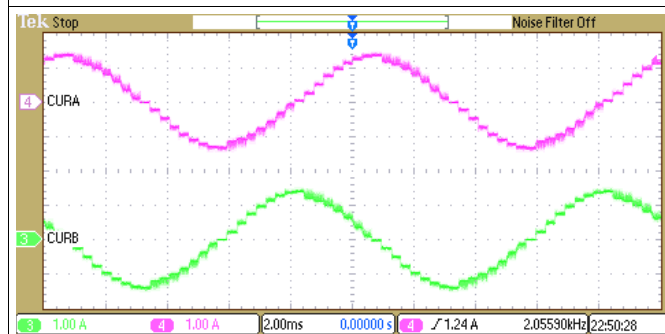**Figure 30. Slow Decay on Increasing and Decreasing Steps**



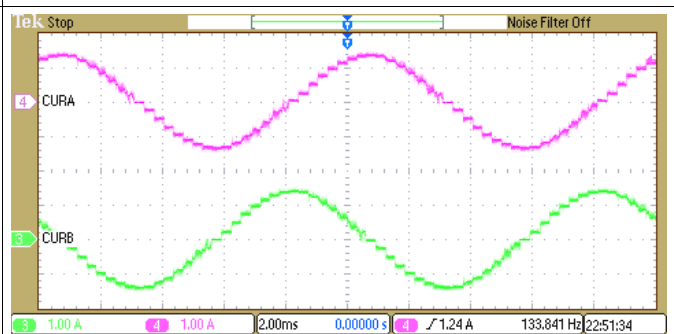**Figure 31. Slow Decay on Increasing and Mixed Decay 30% Fast on Decreasing Steps**
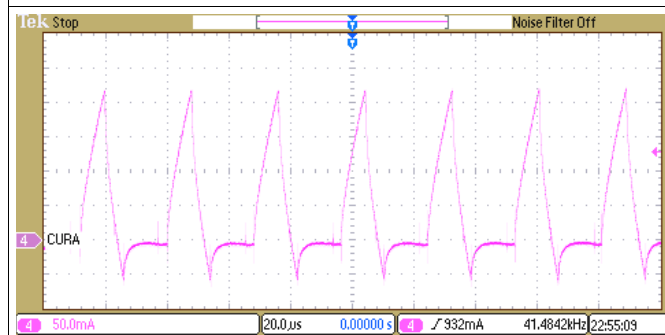


**Figure 32. Smart Tune**



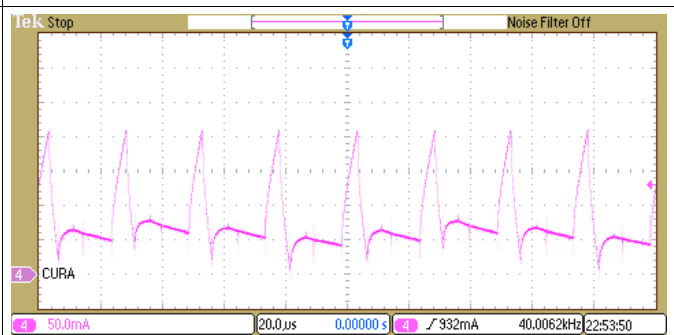**Figure 33. Mixed Decay 30% Fast on Increasing and Decreasing Steps**



**Figure 34. Smart Tune**

Product Folder Links: _DRV8880_

# 9 Power Supply Recommendations

The DRV8880 is designed to operate from an input voltage supply (VM) range between 6.5 V and 45 V. The device has an absolute maximum rating of 50 V. A 0.1-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8880 as possible. In addition, a bulk capacitor must be included on VM.

## 9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:
- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.
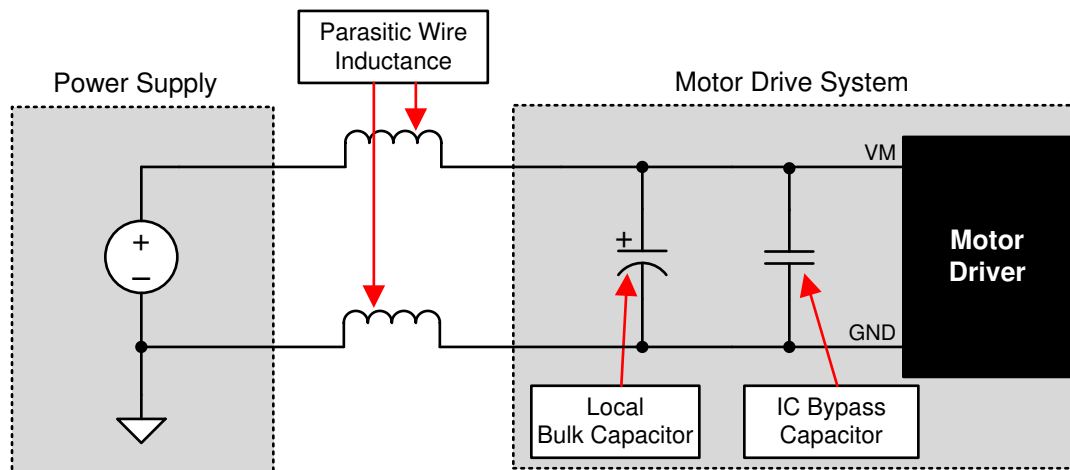


**Figure 35. Setup of Motor Drive System With External Power Supply**

## 10 Layout

### 10.1 Layout Guidelines

Each VM terminal must be bypassed to GND using a low-ESR ceramic bypass capacitors with recommended values of 0.1 μF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.1 μF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.47 μF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

The current sense resistors should be placed as close as possible to the device pins in order to minimize trace inductance between the pin and resistor.
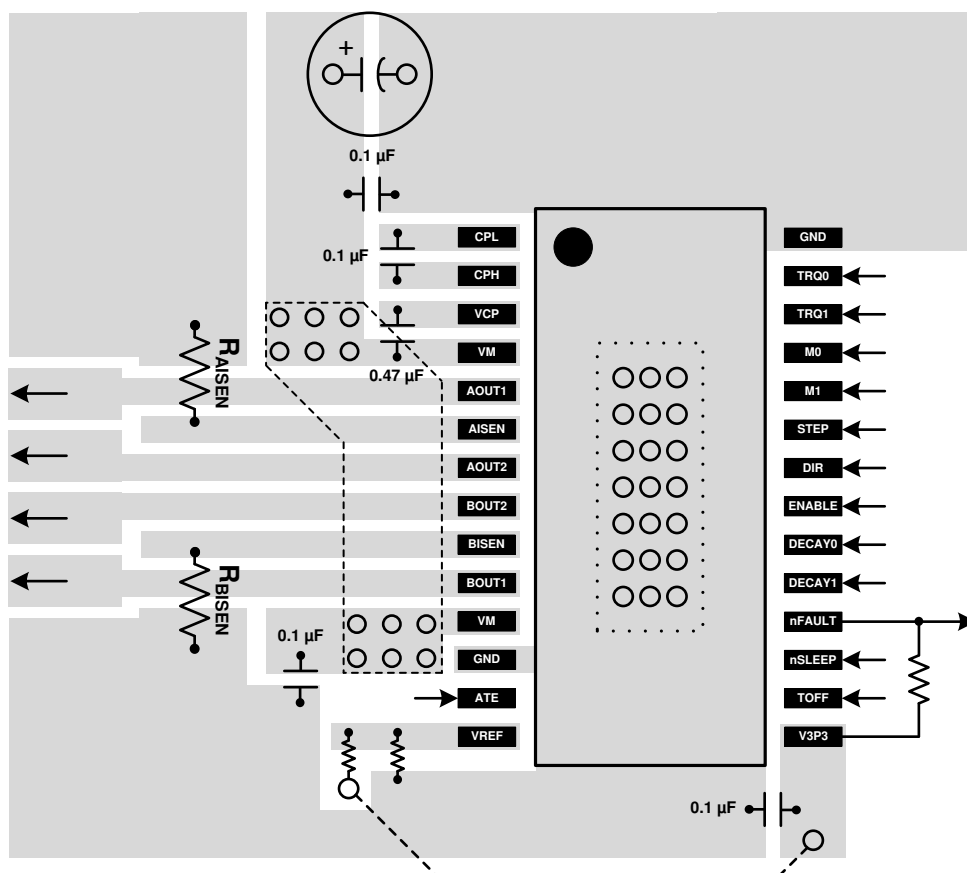
### 10.2 Layout Example



**Figure 36. Layout Recommendation**

Product Folder Links: *DRV8880*

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DRV8880PWP | Obsolete | Production | HTSSOP (PWP) \| 28 | - | - | Call TI | Call TI | -40 to 125 | DRV8880 |
| DRV8880PWPR | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV8880 |
| DRV8880PWPR.A | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV8880 |
| DRV8880PWPR.B | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV8880 |
| DRV8880PWPRG4 | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV8880 |
| DRV8880PWPRG4.A | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV8880 |
| DRV8880PWPRG4.B | Active | Production | HTSSOP (PWP) \| 28 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | DRV8880 |
| DRV8880RHRR | Active | Production | WQFN (RHR) \| 28 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | DRV8880 |
| DRV8880RHRR.A | Active | Production | WQFN (RHR) \| 28 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | DRV8880 |
| DRV8880RHRR.B | Active | Production | WQFN (RHR) \| 28 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | DRV8880 |
| DRV8880RHRT | Obsolete | Production | WQFN (RHR) \| 28 | - | - | Call TI | Call TI | -40 to 125 | DRV8880 |

**(1)** **Status:** For more details on status, see our product life cycle.

**(2)** **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3)** **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4)** **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5)** **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
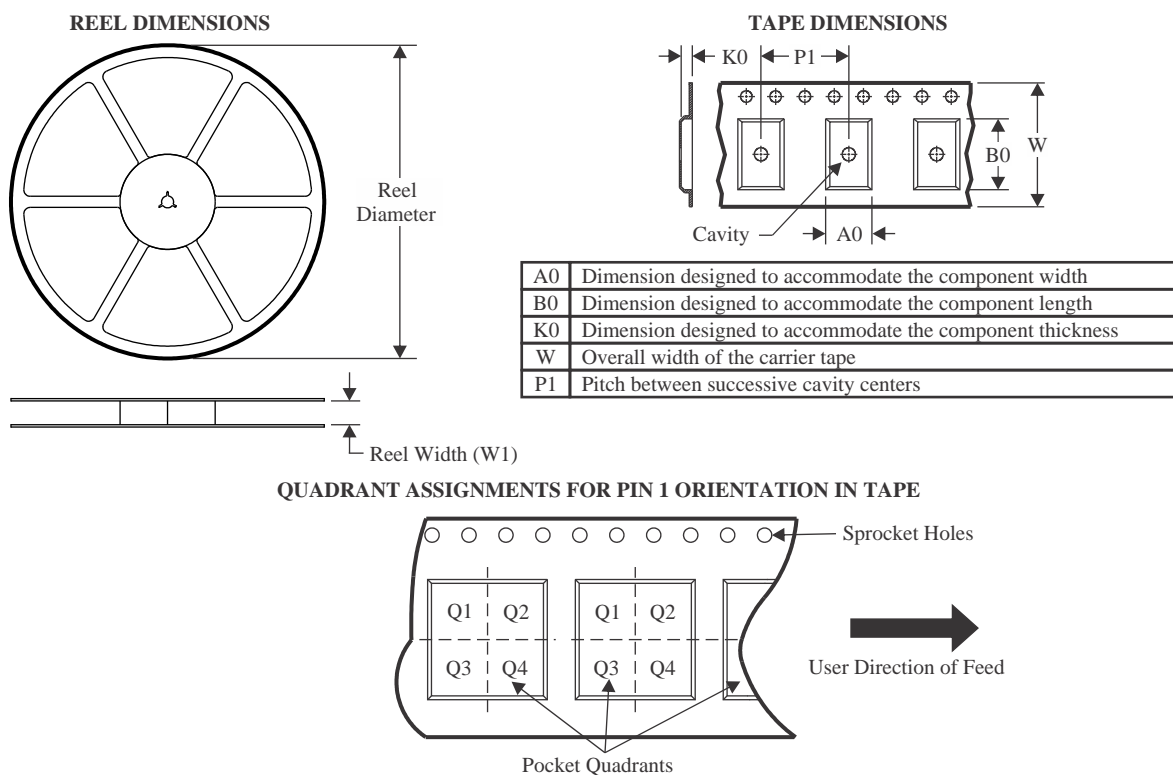
**(6)** **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8880PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| DRV8880PWPRG4 | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| DRV8880RHRR | WQFN | RHR | 28 | 3000 | 330.0 | 12.4 | 3.8 | 5.8 | 1.2 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**
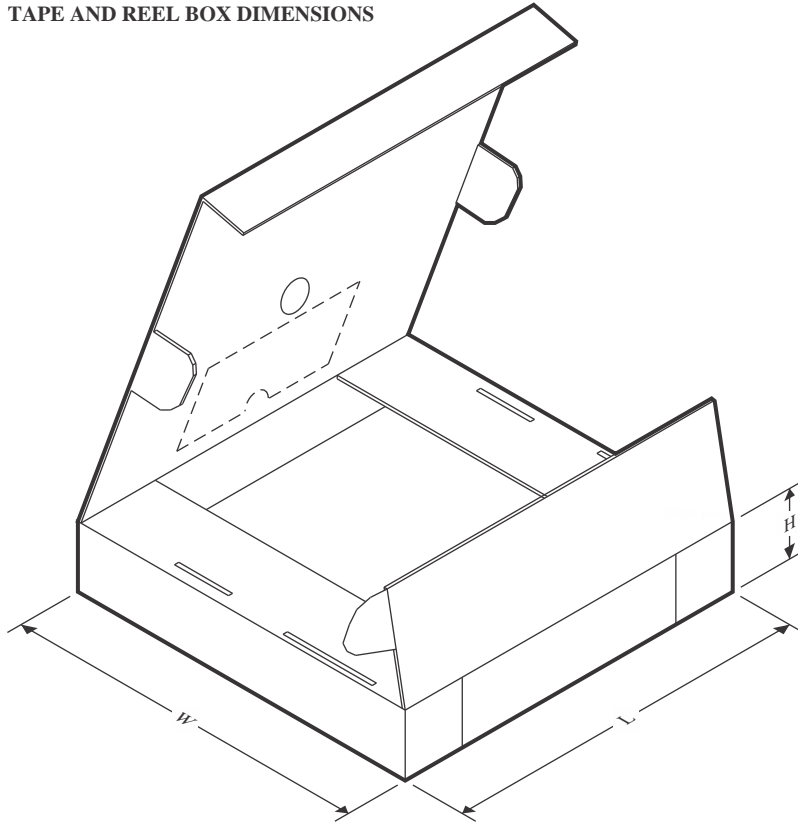


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8880PWPR | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| DRV8880PWPRG4 | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| DRV8880RHRR | WQFN | RHR | 28 | 3000 | 346.0 | 346.0 | 33.0 |

**RHR 28**

**3.5 x 5.5, 0.5 mm pitch**
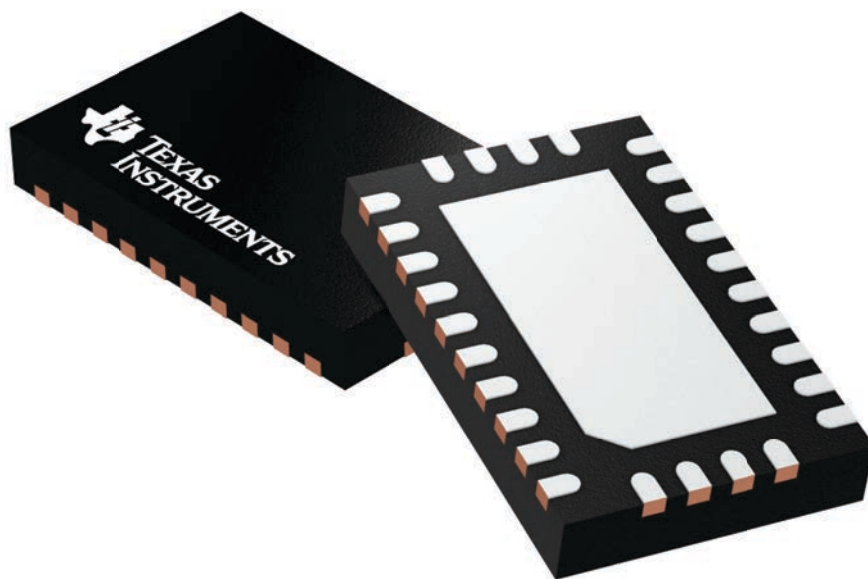
Images above are just a representation of the package family, actual package may vary.
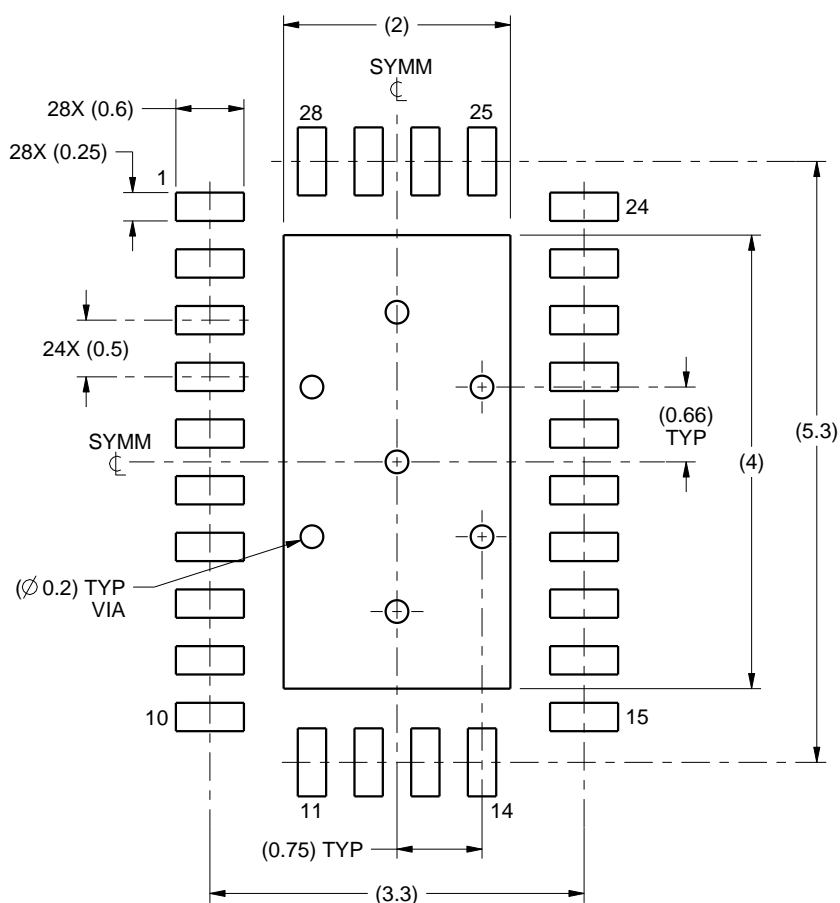Refer to the product data sheet for package details.

4210249/B

A

3.6
3.4

B

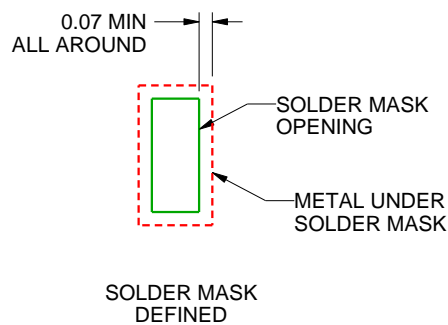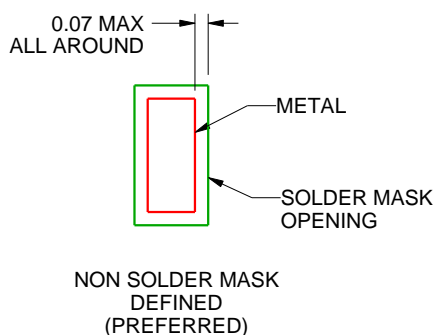PIN 1 INDEX AREA

5.6
5.4

0.5
0.3

0.3
0.2

DETAIL
OPTIONAL TERMINAL
TYPICAL

0.8 MAX

C

⌒ 0.08

SEATING PLANE

0.05
0.00

2±0.1

2X 1.5

24X 0.5

11        14

EXPOSED
THERMAL PAD

10

15

2X
4.5

4±0.1

SEE TERMINAL
DETAIL

1

24

PIN 1 ID
(OPTIONAL)

28        25

28X 0.3
0.2

28X 0.5
0.3

⊕ | 0.1 Ⓜ | C | AⓈ | BⓈ
0.05 Ⓜ

(0.2) TYP

4219075/A    11/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**TEXAS INSTRUMENTS**
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**LAND PATTERN EXAMPLE**
SCALE:15X

(2) SYMM

28X (0.6)

28X (0.25)

24X (0.5)

SYMM

(∅ 0.2) TYP VIA

(0.66) TYP

(5.3)

(4)

(0.75) TYP

(3.3)

**SOLDER MASK DETAILS**

0.07 MAX ALL AROUND

METAL

SOLDER MASK OPENING

NON SOLDER MASK DEFINED (PREFERRED)

0.07 MIN ALL AROUND

SOLDER MASK OPENING

METAL UNDER SOLDER MASK

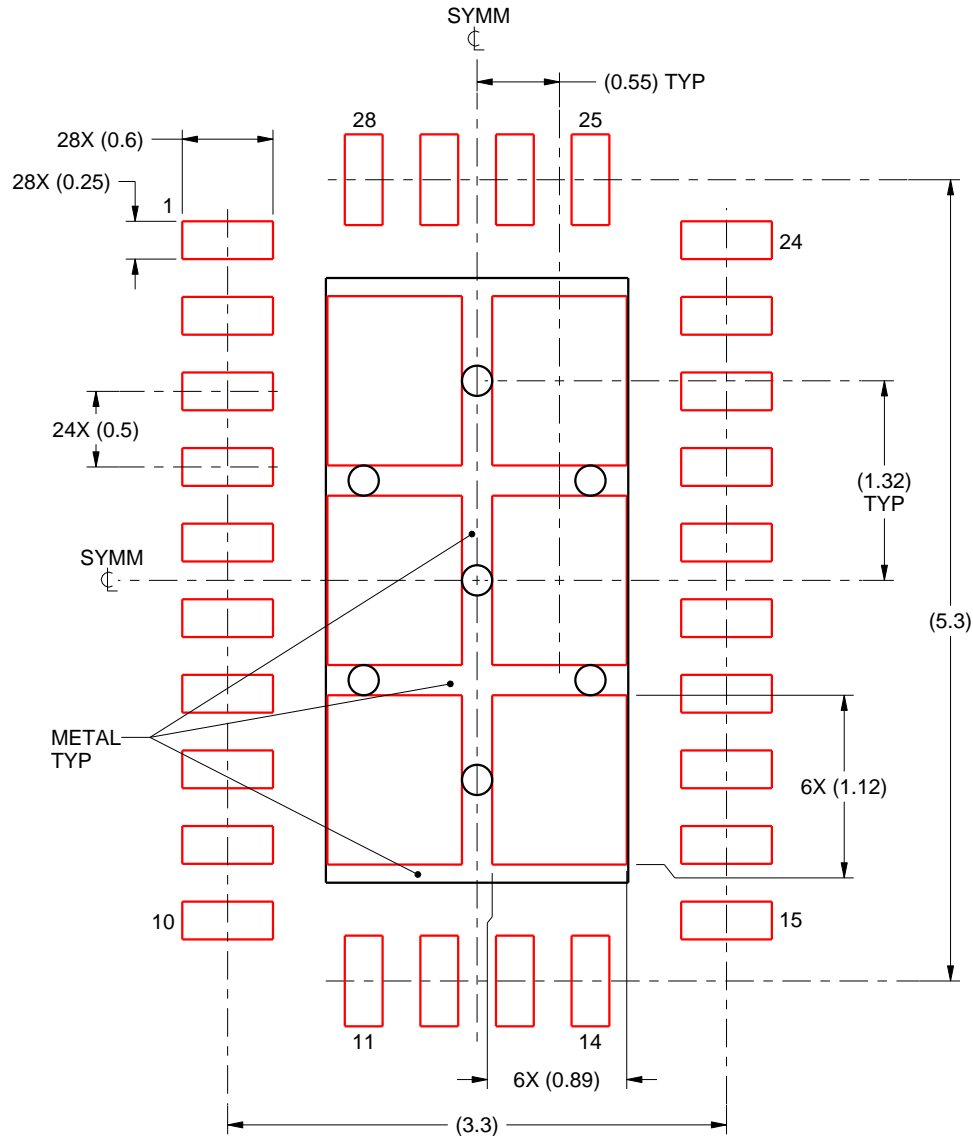SOLDER MASK DEFINED

4219075/A   11/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

SYMM

(0.55) TYP

28

25

28X (0.6)

28X (0.25)

1

24

24X (0.5)

(1.32)
TYP

SYMM

(5.3)

METAL
TYP

6X (1.12)

10

15

11

14

6X (0.89)

(3.3)

## SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219075/A   11/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PWP 28**
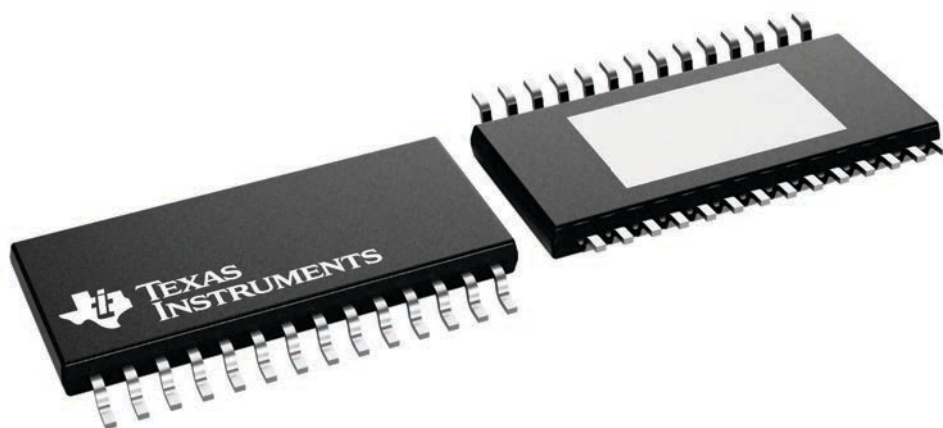
PowerPAD™ TSSOP - 1.2 mm max height

**4.4 x 9.7, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

6.6
6.2 TYP

A

PIN 1 INDEX
AREA

1

28

26X 0.65

C

0.1 C

SEATING
PLANE

2X
8.45

9.8
9.6
NOTE 3

14

B

15

4.5
4.3

28X 0.30
0.19

⊕ 0.1Ⓜ C A B

SEE DETAIL A

(0.15) TYP

2X 0.95 MAX
NOTE 5

14

15

2X 0.2 MAX
NOTE 5

5.18
4.48

THERMAL
PAD

0.25

GAGE PLANE

1.2 MAX

1

28

3.1
2.4

0°-8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4223582/A   03/2017

PowerPAD is a trademark of Texas Instruments.
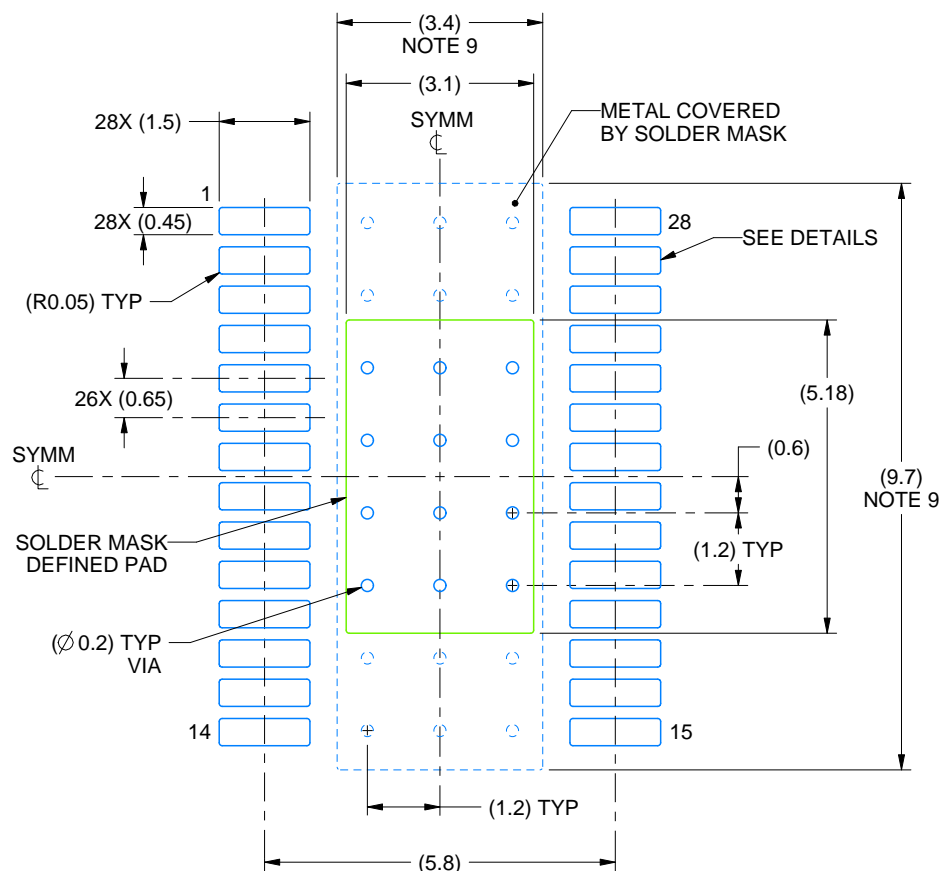
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
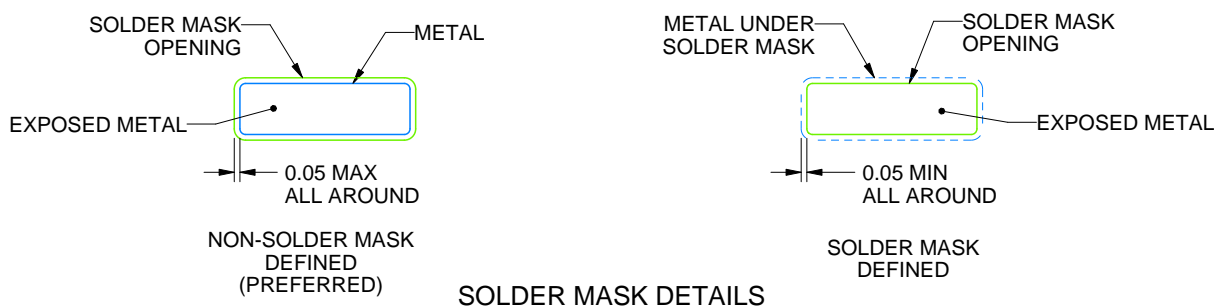5. Features may differ or may not be present.

# PWP0028C

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

SOLDER MASK OPENING
METAL
EXPOSED METAL
0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER SOLDER MASK
SOLDER MASK OPENING
EXPOSED METAL
0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4223582/A   03/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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## PWP0028C
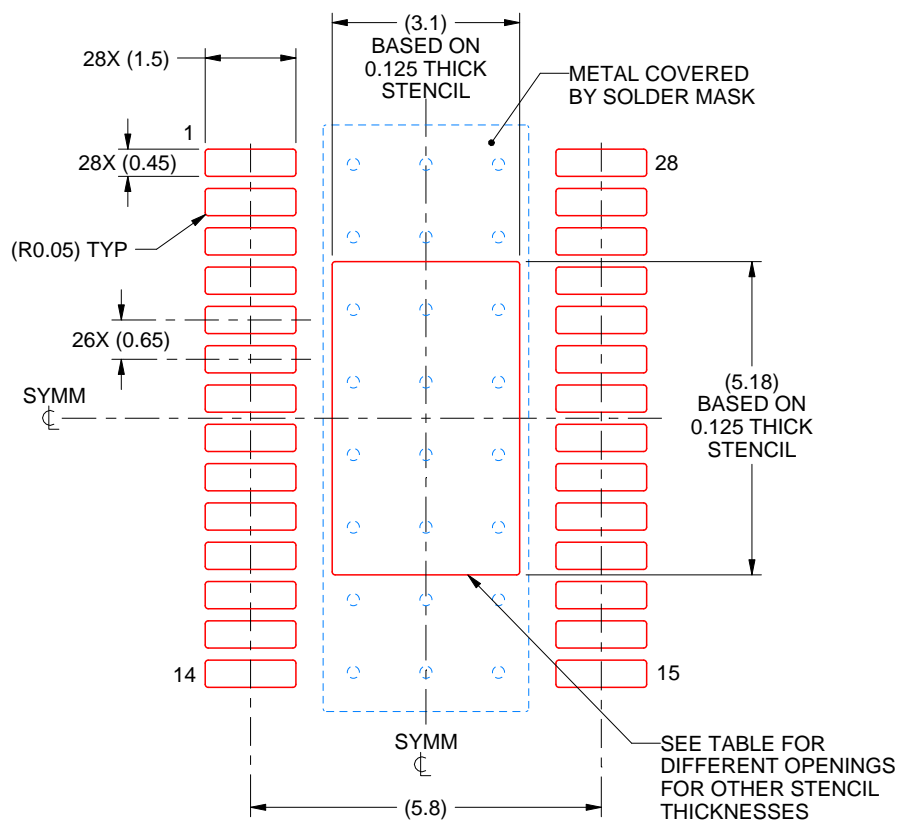
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.47 X 5.79 |
| 0.125 | 3.10 X 5.18 (SHOWN) |
| 0.15 | 2.83 X 4.73 |
| 0.175 | 2.62 X 4.38 |

4223582/A   03/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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